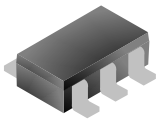
CURRENT MODE PWM＋PFM CONTROLLER

DESCRIPTION

The SD4873A is a current mode PWM+PFM controller IC for high performance, low standby power offline flyback converter application.

Large startup resistor could be used in the startup circuit to minimize the standby current because of low startup current. The frequency reducing function makes it can operate in Burst Mode to reduce switching loss and improve efficiency. Excellent EMI performance is achieved with frequency shuffling technique and soft switching control at the totem pole gate driver output. The built-in soft start-up function reduces device's stress to avoid transformer saturation. The cycle-by-cycle peak current limit and high-/low-voltage limit peak current compensation keeps the consistency of output power in high voltage and low voltage conditions.

The SD4873A offers complete protection functions including internal and settable over-voltage protections for V_{DD}, leading edge blanking, cycle-by-cycle peak current limit, output over-voltage protection, over-load protection, internal and settable over- temperature protection, etc.



SOT-23-6L

APPLICATIONS

- Battery Chargers
- Adapters
- Set-Top Box Power Supplies

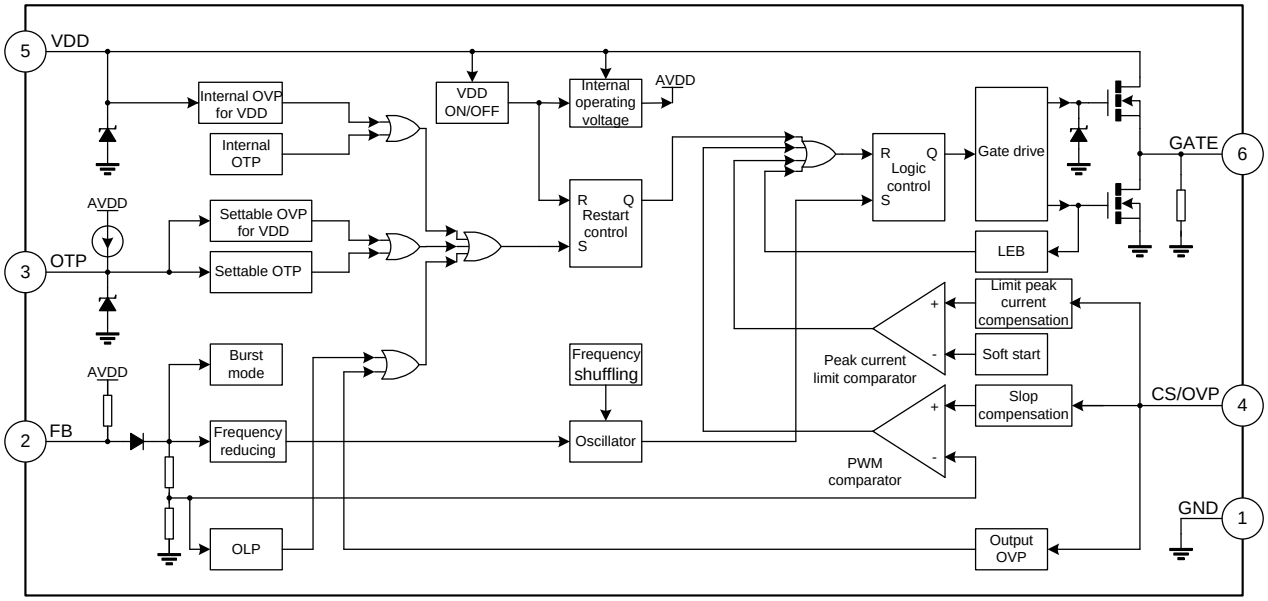
FEATURES

- Low startup current
- Frequency reducing
- Burst mode
- Frequency shuffling
- Totem pole gate driver output with soft switch control
- Soft Start
- Cycle-by-cycle peak current limiting
- High-/low-voltage limit peak current compensation
- Internal and settable over-voltage protections for V_{DD}
- Leading edge blanking
- Output over-voltage protection
- Over-load protection
- Internal and settable over-temperature protections

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SD4873ATR	SOT-23-6L	873A	Halogen free	Tape & Reel

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Rating	Unit
VDD Supply Voltage	VDD	30	V
FB Input Voltage	VFB	-0.3~6	V
CS/OVP Input Voltage	VCS	-0.3~6	V
OTP Input Voltage	VOTP	-0.3~6	V
Junction Temperature Range	T_j	-20~150	°C
Lead Temperature	T_L	260	°C
Storage Temperature Range	T_{stg}	-55~150	°C

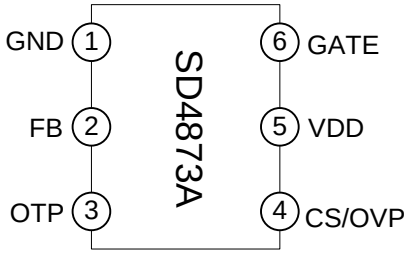
ELECTRICAL CHARACTERISTICS (Unless otherwise specified, VDD=18V, Tam_b=25°C)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
VDD Pin						
Startup Current	I_{ST}	VDD=13.5V,VFB=0V	--	1	15	μA
Operation Current	I_{DD}	VDD=18V,VFB=3V	--	1	--	mA
Start up Voltage	VDD_{START}		14.5	15.5	16.5	V
Shut down Voltage	VDD_{SHUT}		6.5	7.5	8.5	V
Internal VDD OVP Threshold	VDD_{OVP1}		--	27.3	--	V
VDD Clamp Voltage	VDD_{CLAMP}	I_{DD} =10mA	--	30	--	V
Operating Frequency						
Oscillation Frequency	f_{OSC}		57	65	73	KHz
Max. Duty Cycle	D_{MAX}	VFB =3V, VCS/OVP=0V	--	80	--	%

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Frequency Shuffling Range	Δf_{OSC_JITTER}		-4	--	4	%
Frequency Reducing Threshold	VFB_{FD_START}		--	2	--	V
Oscillation Frequency in Burst Mode	f_{OSC_BURST}		--	23	--	KHz
The Threshold Enter Burst Mode	VFB_{BURST_ENTER}		--	1.1	--	V
The Threshold Exit Burst Mode	VFB_{BURST_EXIT}		--	1.2	--	V
FB pin						
FB Input Impedance	ZFB_{IN}		--	11.5	--	KΩ
FB Open Loop Voltage	VFB_{OPEN}		--	5	--	V
FB Short Circuit Current	IFB_{SHORT}	VFB=0V	--	150	--	uA
Detection Threshold for OLP	VFB_{OLP_DET}		--	3.75	--	V
Delay Time for Overload Protection	td_{OLP}		--	90	--	ms
PWM Gain	AV_{FB_CS}	$\Delta V_{FB}/\Delta V_{CS}$	--	2	--	V/V
OTP Pin						
OTP Output Current	$IOTP_{OUT}$		--	100	--	uA
Detection Threshold for Settable OTP	V_{OTP2_DET}		--	1.0	--	V
Delay time for Settable OTP	td_{OTP2}		16	--	32	Cycles
Internal OTP Threshold	T_{OTP1}		--	150	--	°C
Hysteresis Temperature of Internal OTP	T_{OTP1_HYS}		--	25	--	°C
Detection Threshold for VDD Settable OTP	VDD_{OVP2_DET}		--	4.25	--	V
CS/OVP						
CS Current Limit initial Point	VCS_{LIMIT0}	Duty cycle D=0	--	0.7	--	V
CS Clamp Point	VCS_{CLAMP}		--	1	--	V
LEB Time	t_{LEB}		--	400	--	ns
Soft Start Time	t_{ss}		--	4	--	ms
Detection Threshold for Output OVP	VCS_{OVP_DET}		--	0.4	--	V
Delay Time for Output OVP	td_{OVP}		4	--	5	Cycles
Gate Driver						
Output Low Level	$VGATE_{OL}$	I_O=-20mA	--	0.15	0.8	V
Output High Level	$VGATE_{OH}$	I_O=20mA	13.8	15	--	V
Output Clamp Voltage Level	$VGATE_{OH\_CLAMP}$	VDD=25V	--	17	--	V

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rising Time	t_r	C_L=1nF	--	200	--	ns
Output Falling Time	t_f	C_L=1nF	--	80	--	ns

PIN CONFIGURATION



PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	GND	--	Ground.
2	FB	I	Feedback input pin.
3	OTP	I/O	Dual function pin. Either for OTP detection or for settable VDD OVP detection
4	CS/OVP	I	Switch current sense input and output OVP detection pin.
5	V_{DD}	--	Power supply pin.
6	GATE	O	Gate driver output pin.

FUNCTION DESCRIPTIONS

The SD4873A is a current mode PWM+PFM controller, which features low startup current, frequency reducing, frequency shuffling, soft switching control at the totem pole gate driver output, soft start, cycle-by-cycle peak current limit, and high-/low-voltage limit peak current compensation. It offers complete protection functions including internal and settable over-voltage protections for V_{DD}, leading edge blanking, output over-voltage protection, over-load protection, internal and settable over- temperature protection, etc. The detailed functions are as follows:

Startup Control

The startup current of SD4873A is very low so that IC could start up quickly. A large startup resistor can be used in startup circuit to minimize standby power loss yet provides reliable startup in application.

Frequency Reducing Control

The SD4873A controls the switching frequency f through detecting the FB voltage, their relationship is shown in the following diagram. At general load condition, the switching frequency f is fixed at 65KHz, i.e., the system works in PWM mode; at light load condition, f drops from 65KHz, and the system works in PFM mode; at no-load condition, f drops to 23KHz, and the system works in Burst mode.

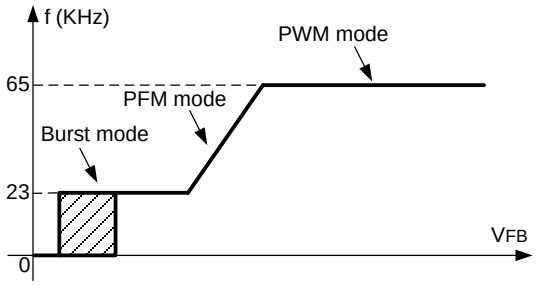


Figure 1. Frequency reducing curve

Burst Mode

At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss.

The SD4873A enters Burst mode through frequency reducing at light condition or no load condition, i.e., when the output voltage is lower than desired value, the MOSFET begins to works, meanwhile the switching frequency drops to reduce the switching times, otherwise the MOSFET is always cutoff for low switching loss and high efficiency, the waveform is shown as follows:

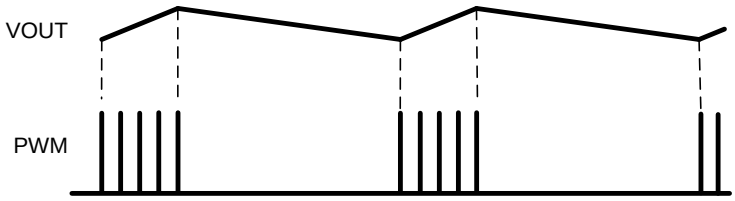


Figure 2. Burst mode waveforms

Frequency Shuffling Control

Frequency shuffling is used in SD4873A to improve EMI performance.

The oscillation frequency is modulated randomly so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and the system design can be easier. The entire application system design can become simpler.

Totem Pole Gate Driver Output with Soft Switch Control

GATE pin is connected to external MOSFET's gate for switch control. Weak gate drive ability results in more switch loss of MOSFET while strong gate drive ability causes EMI problem.

A good tradeoff is achieved through the totem pole gate drive design with appropriate output ability and dead time control.

Besides that, the output high voltage of GATE is clamped at 17V to protect the external MOSFET.

Soft Start

The SD4873A features an internal 4ms soft start function, which limits the max. peak current at DRAIN of MOSFET for small stress to avoid transformer saturation.

Cycle-by-cycle Peak Current Limit

In every cycle, the peak current is determined by the comparing point of comparator, this value will not exceed the peak current limit value to make sure that the current flowing through MOSFET is lower than rated current. When the current reaches the peak current, the output power cannot rise, thereby the maximum output power is limited.

High-/low-voltage limit peak current compensation

The SD4873A uses patented curve compensation mode, which greatly improves the peak current compensation and ensures the consistency of output power in high-/low-voltage condition.

Internal and Settable VDD Over-voltage Protection

When VDD is higher than VDD OVP threshold (27.3V), the circuit enters into over-voltage protection status, the MOSFET is off, and the system restarts automatically.
When OTP pin of SD4873A is used for VDD OVP detection, the settable VDD OVP is available, and then a Zener diode is needed between OTP and VDD pins. If OTP pin voltage exceeds detection threshold (4.25V) for settable VDD OVP, the circuit enters into over-voltage protection status, and the MOSFET is off, and the system restarts automatically.

Leading Edge Blanking

At the moment of MOSFET turned on, the current spike due to snubber diode reverse recovery should be chopped off for it will cause error judgment of PWM comparator. And this is available through internal LEB (Leading Edge Blanking) circuit. So that the external RC filter circuit on CS/OVP input is no longer required.
During the blanking period, the PWM comparator and peak current limit comparator are disabled and MOSFET keeps on state. The minimum on time of MOSFET is just LEB time. The waveform is shown as follows:

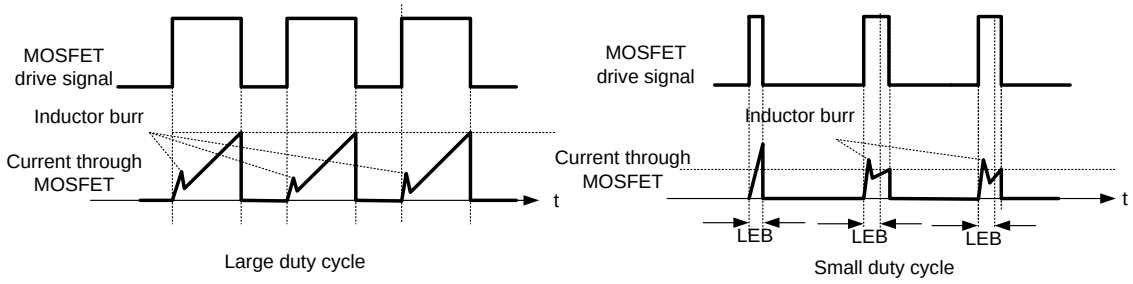


Figure 3. LEB waveforms at different duty cycle conditions

Output Over-voltage Protection

CS/OVP pin of SD4873A is used for switching current sensing during switch on state while is used for output voltage detection during switch off state and primary side freewheeling period. When it is used for the latter function, if CS/OVP pin voltage exceeds the detection threshold 0.4V for output OVP and lasts for 4～5 switching periods, the system enters output over-voltage protection state, MOSFET is cut off, and the system restarts automatically, the waveforms are shown as follows:

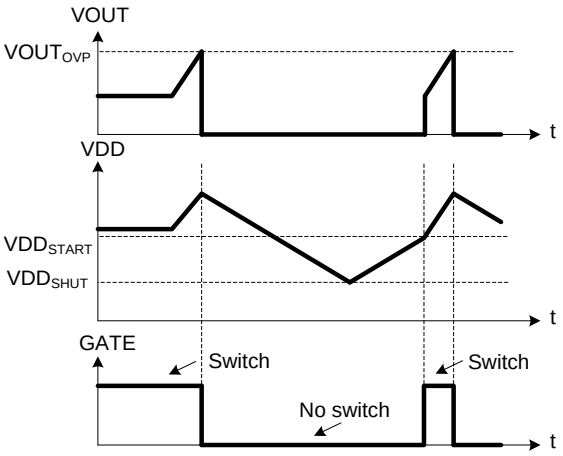


Figure 4. Output OVP waveforms

Over-load Protection

When FB input voltage is higher than the detection threshold (3.75V) for OLP and lasts for OLP delay time (90ms), the circuit enters into over-load protection status, the MOSFET is off, and the system restarts automatically, the waveforms are shown as follows:

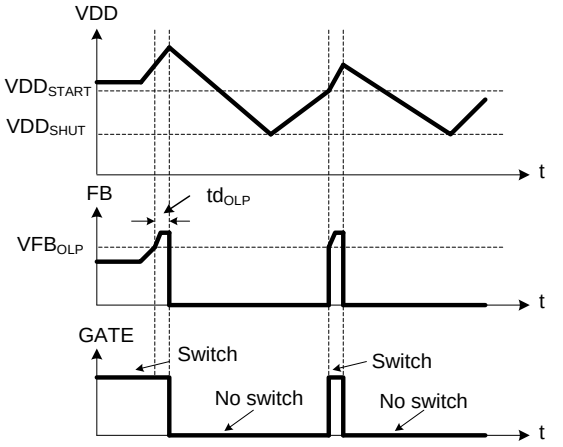


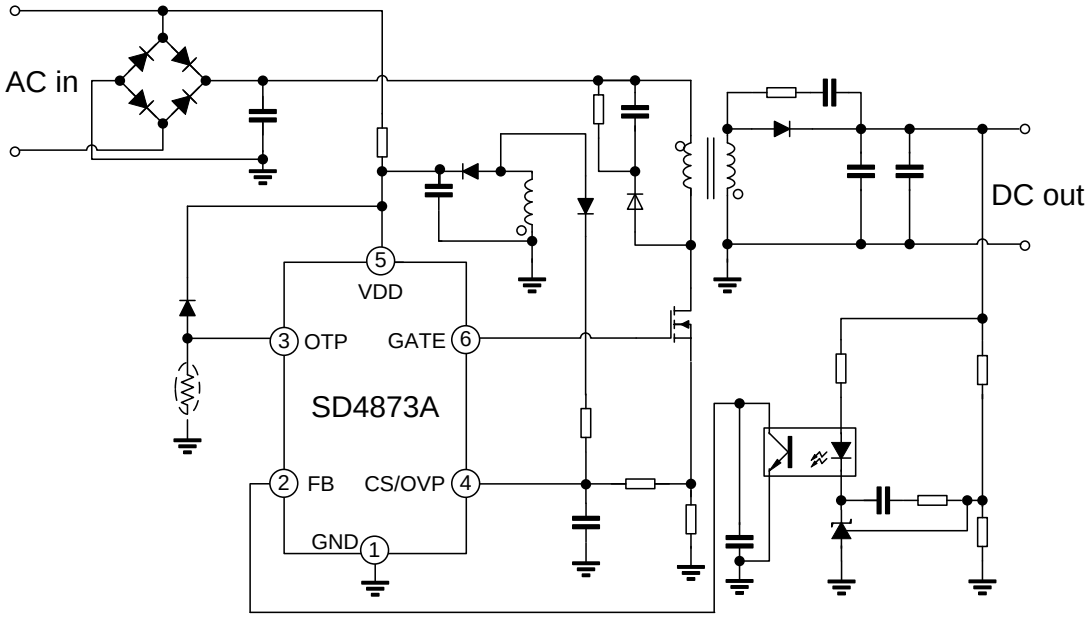
Figure 5. OLP waveforms

Internal and Settable Over-temperature Protection

The internal OTP threshold is 150°C, and the hysteresis temperature is 25°C, when the temperature exceeds the threshold value, the OTP is activated to shut off MOSFET, and the system restarts automatically; when the temperature drops to 125°C, the OTP is deactivated, the system recovers.

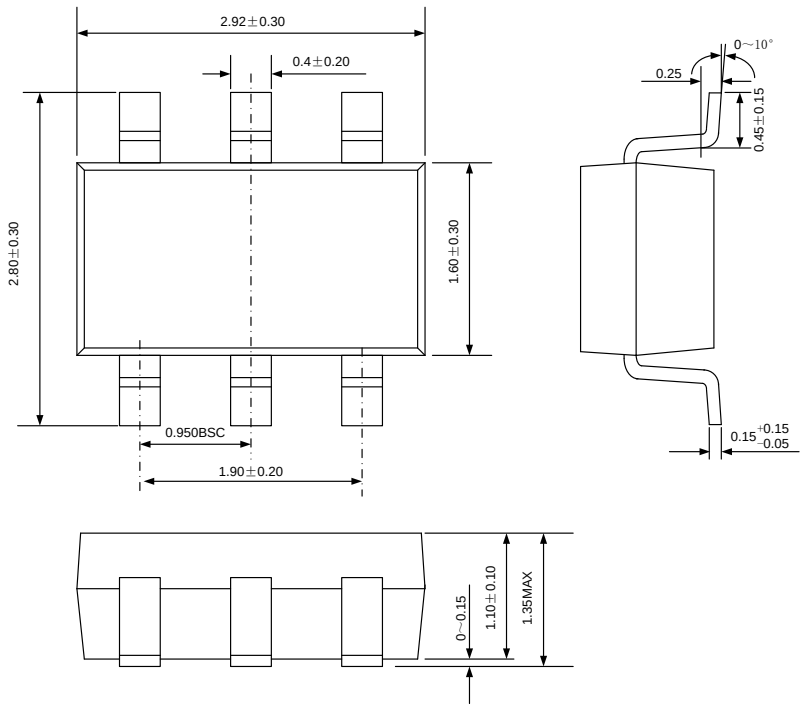
When OTP pin of SD4873A is used for settable OTP detection, the output current (100μA) flows to ground through the NTC resistor. When the temperature rises, the value of NTC resistor decreases and the voltage across NTC resistor also decreases. When the voltage is smaller than detection threshold (1V) for settable OTP, and lasts for 16~32 switching cycles or above, the OTP is activated to shut off MOSFET, and the system restarts automatically.

TYPICAL APPLICATION CIRCUIT



PACKAGE OUTLINE

SOT-23-6L **UNIT: mm**



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

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Rev.:	1.3	Author:	Lin Haifeng

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1. Modify the electrical characteristic

Rev.:	1.2	Author:	Lin Haifeng

Revision History:

1. Modify the electrical characteristic

Rev.:	1.1	Author:	Lin Haifeng

Revision History:

1. Modify the electrical characteristic
2. Modify the function descriptions

Rev.:	1.0	Author:	Lin Haifeng

Revision History:

1. First release