NOVOSENSE

NSI1300D25-DSWWAR
High Reliability Reinforced Isolated Amplifier
Datasheet (EN) 1.0

Product Overview

NSI1300D25-DSWWAR is a high-performance isolated amplifier with output separated from input based on the NOVOSENSE capacitive isolation technology. The device has a linear differential input signal range of ±250mV (±320mV full-scale). The differential input is ideally suited to shunt resistor-based current sensing in high voltage applications where isolation is required.

The device has a fixed gain of 8.2 and provides a differential analog output.

The low offset and gain drift ensure the accuracy over the entire temperature range. High common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in motor control applications.

The fail-safe functions including input common-mode overvoltage detection and missing VDD1 detection simplify system-level design and diagnostics.

Key Features

- Up to 7500V_{rms} Insulation voltage
- ±250mV linear Input Voltage Range
- Fixed Gain: 8.2
- Low Offset Error and Drift:

  NSI1300D25: ±0.2mV (Max), 4μV/℃ (Max)
- Low Gain Error and Drift:

  ±0.3% (Max), ±50ppm/℃ (Max)
- Low Nonlinearity and Drift:

  ±0.03% (Max), ±1ppm/℃ (Typ)
- SNR: 86dB (Typ, BW=10kHz), 72dB (Typ, BW=100kHz)
- Wide bandwidth: 310kHz (Typ)
- High CMTI: 150kV/μs (Typ)
- System-Level Diagnostic Features:
  - VDD1 monitoring
  - Input common-mode overvoltage detection
- Operation Temperature: -40℃ ~125℃
- RoHS-Compliant Packages: SOP8(600mil)

Safety Regulatory Approvals

- UL recognition: up to 7500V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1
- CSA component notice 5A
- DIN VDE V 0884-17

Applications

- Shunt current monitoring
- Motor Drives
- Uninterruptible Power Suppliers
- Solar Inverters

Device Information

Part Number	*Package*	*Body Size*
NSI1300D25-DSWWAR	SOP8(600mil)	6.25 mm × 13.60mm

Functional Block Diagrams

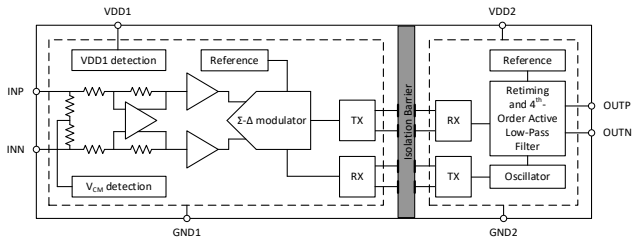

Figure 1. NSI1300 Block Diagram

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1. Pin Configuration and Functions

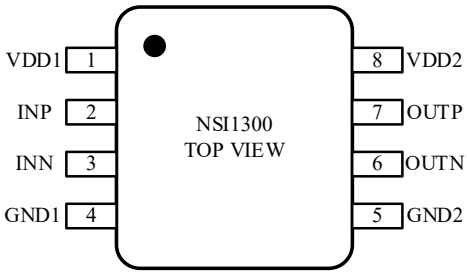


Figure 1.1 NSI1300 Package

Table 1.1 NSi1300 Pin Configuration and Description

NSI1300 PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD1	Power supply for input side(3.0V to 5.5V)
2	INP	Positive analog input (±250mV recommended for NSI1300D25 and ±50mV recommended for NSI1300D05)
3	INN	Negative analog input
4	GND1	Ground 1, the ground reference for input side
5	GND2	Ground 2, the ground reference for output side
6	OUTN	Negative output
7	OUTP	Positive output
8	VDD2	Power supply for input side (3.0V to 5.5V)

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD1, VDD2	-0.3		6.5	V
Input Voltage	INP, INN	GND1-6		VDD1+0.5	V
Output Voltage	OUTP, OUTN	GND2-0.5		VDD2+0.5	V
Output current per Output Pin	Io	-10		10	mA
Operating Temperature	T_{OPR}	-40		125	℃
Junction Temperature	T_J	-40		150	℃
Storage Temperature	T_{STG}	-55		150	℃
Electrostatic discharge	HBM (1)	±2000			V
	CDM (2)	±1000			V

(1) Human body model (HBM), per AEC-Q100-002-RevD

(2) Charged device model (CDM), per AEC-Q100-011-RevB

3. Recommended Operating Conditions

Parameters		Symbol	Min	Typ	Max	Unit
Side1 Power Supply		VDD1	3.0	5.0	5.5	V
Side2 Power Supply		VDD2	3.0	3.3	5.5	V
NSI1300D25	Differential input voltage before clipping output	$V_{Clipping}$		±320		mV
	Linear differential input full scale voltage	V_{FSR}	-250		250	mV
	Operating common-mode input voltage	V_{CM}	-0.16		0.8	V
Operating Ambient Temperature		T_A	-40		125	℃

4. Thermal Information

Parameters	Symbol	SOP8(600mil)	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	78.9	℃/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	41.6	℃/W
Junction-to-board thermal resistance	$R_{\theta JB}$	43.6	℃/W

5. Specifications

5.1. Electrical Characteristics: NSI1300D25-DSWWAR

(VDD1 = 3.0V ~ 5.5V, VDD2 = 3.0V ~ 5.5V, INP = -250mV to +250mV, and INN = GND1 = 0V, T_A = -40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 3.3V, T_A = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply						
Side1 Supply Voltage	VDD1	3.0	5.0	5.5	V	
Side2 Supply Voltage	VDD2	3.0	3.3	5.5	V	
Side1 Supply Current	IDD1		11.4	15.1	mA	
Side2 Supply Current	IDD2		6.3	8.4	mA	
VDD1 undervoltage detection threshold voltage	$VDD1_{UV}$	1.8	2.3	2.7	V	VDD1 falling
Analog Input						
Common-mode overvoltage detection level	V_{CMov}	0.9			V	Detection level has a typical hysteresis of 96 mV
Input offset voltage	V_{OS}	-0.2	±0.01	0.2	mV	T_a=25℃ 4.5V≤VDD1≤5.5V INP = INN = GND1
Input offset drift	$\lvert dV_{OS}/dT_A \rvert$			4	μV/℃	
Common-mode rejection ratio	$CMRR_{dc}$		-106		dB	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
	$CMRR_{ac}$		-106		dB	INP = INN, f_{IN} = 10 kHz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
Single-ended input resistance	R_{IN}		19		kΩ	T_a=25℃ INN = GND1
Differential input resistance	R_{IND}		22		kΩ	
Input capacitance	C_I		2		pF	
Input bias current	I_{IB}	-24	-18	-12	μA	T_a=25℃ INP = INN = GND1, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$
Input bias current drift	TCI_{IB}		±1		nA/℃	
Analog Output						
Nominal Gain			8.2		V/V	
Gain error	E_G	-0.3%	±0.05%	0.3%		T_a=25℃
Gain error thermal drift	TCE_G	-50	±15	50	ppm/℃	
Nonlinearity		-0.03%	±0.01%	0.03%		T_a=25℃
Nonlinearity drift			±1		ppm/℃	
Total harmonic distortion	THD		-85		dB	V_{IN} =500mVpp, f_{IN} = 10kHz, BW = 100kHz
Output noise			195		μV_{RMS}	INP = INN = GND1, BW = 100kHz
Signal to noise ratio	SNR	80	86		dB	V_{IN} = 500mVpp, f_{IN} = 1kHz, BW = 10kHz

Parameters	Symbol	Min	Typ	Max	Unit	Comments
			72		dB	V_{IN} = 500mVpp, f_{IN} = 10kHz, BW = 100kHz
Common-mode output voltage	V_{CMout}	1.39	1.44	1.49	V	
Failsafe differential output voltage	$V_{FAILSAFE}$		-2.6	-2.5	V	V_{CM}>V_{CMov}, or VDD1 missing
Output bandwidth	BW	250	310		kHz	
Power supply rejection ratio (1)	$PSRR_{dc}$		-104		dB	PSRR vs VDD1, at DC
	$PSRR_{ac}$		-102		dB	PSRR vs VDD1, 100mV and 10kHz ripple
	$PSRR_{dc}$		-90		dB	PSRR vs VDD2, at DC
	$PSRR_{ac}$		-85		dB	PSRR vs VDD2, 100mV and 10kHz ripple
Output resistance	R_{OUT}		< 0.2		Ω	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Timing						
Rising time of OUTP, OUTN	t_r		1.3		μs	
Falling time of OUTP, OUTN	t_f		1.3		μs	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t_{PD}		1.6	2.1	μs	
Analog setting time	t_{AS}		0.5		ms	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to OUTP, OUTN valid, 0.1% settling

(1) Input referred.

5.2. Typical Performance Characteristics

Unless otherwise noted, test at VDD1 = 5V, VDD2 = 3.3V, Vin = -250mV to 250mV

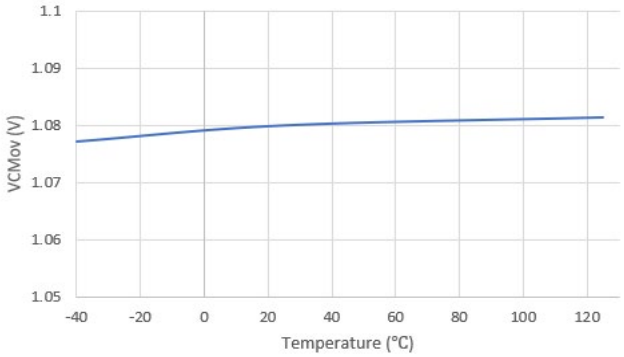


Figure 5.1 Common-Mode Overvoltage Detection Level vs Temperature

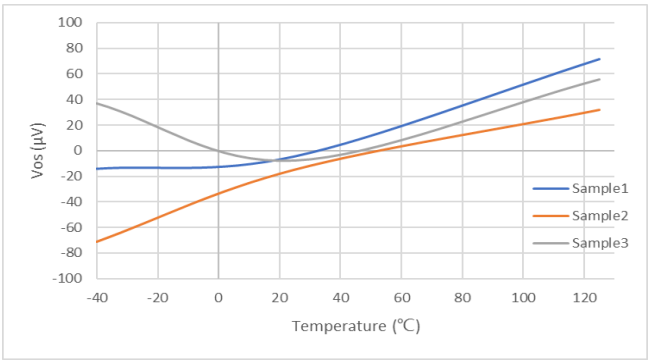


Figure 5.2 Input Offset Voltage vs Temperature

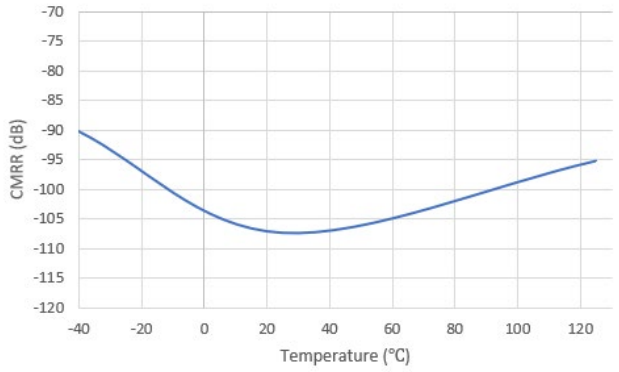


Figure 5.3 Common-Mode Rejection Ratio vs Temperature

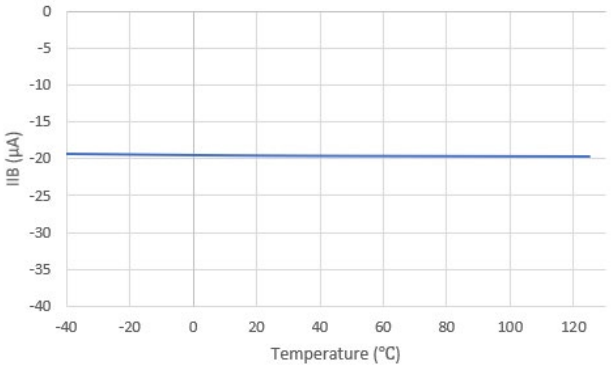


Figure 5.4 Input Bias Current vs Temperature

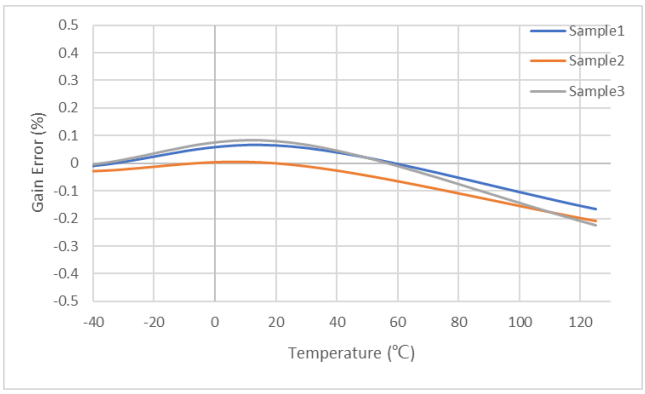


Figure 5.5 Gain Error vs Temperature

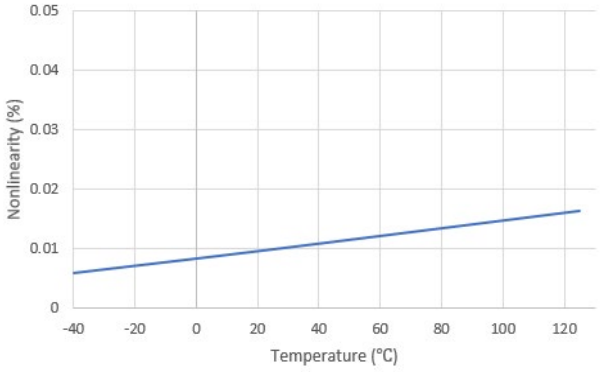


Figure 5.6 Nonlinearity vs Temperature

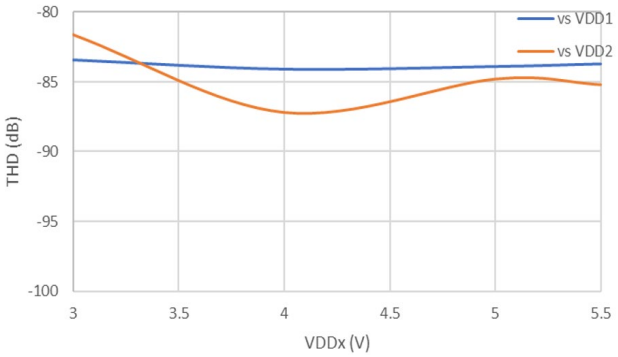


Figure 5.7 THD vs Supply Voltage

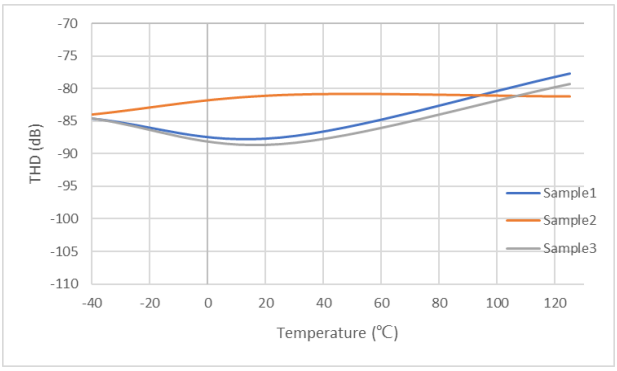


Figure 5.3 THD vs Temperature

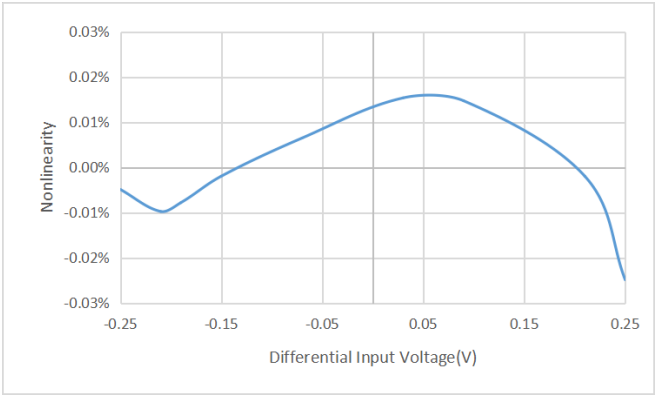


Figure 5.9 Nonlinearity vs Input Voltage

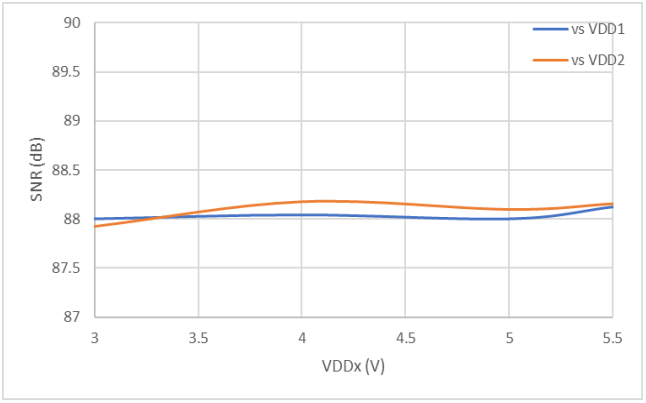


Figure 5.10 SNR vs Supply Voltage

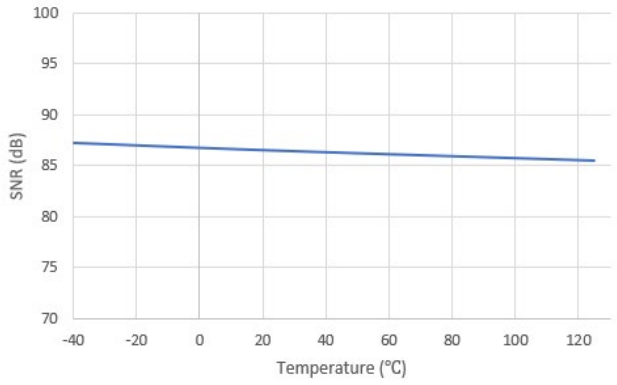


Figure 5.4 SNR vs Temperature

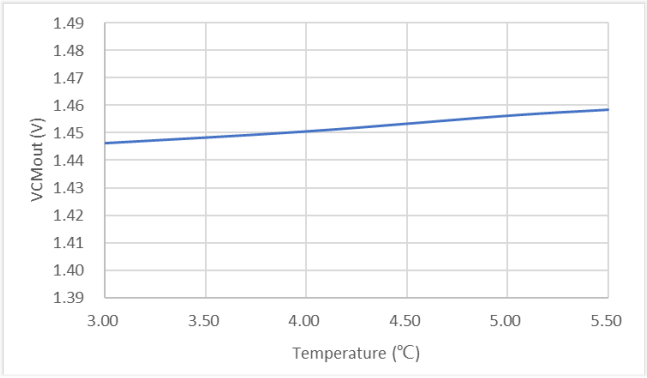


Figure 5.12 Output Common-Mode Voltage vs Side2 Supply Voltage

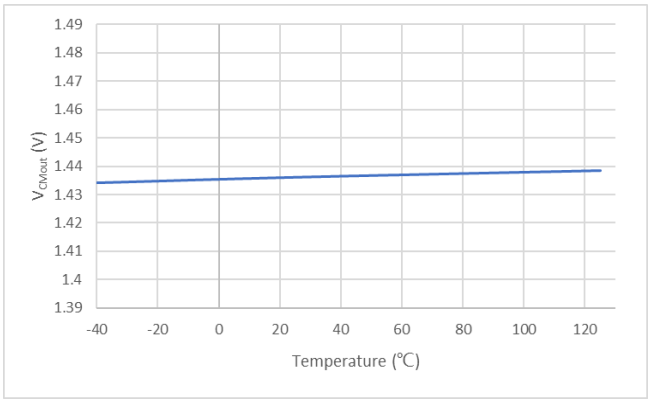


Figure 5.13 Output Common-Mode Voltage vs Temperature

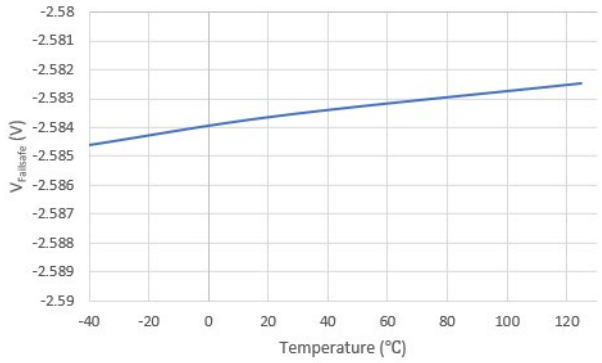


Figure 5.14Fail-Safe Output Voltage vs Temperature

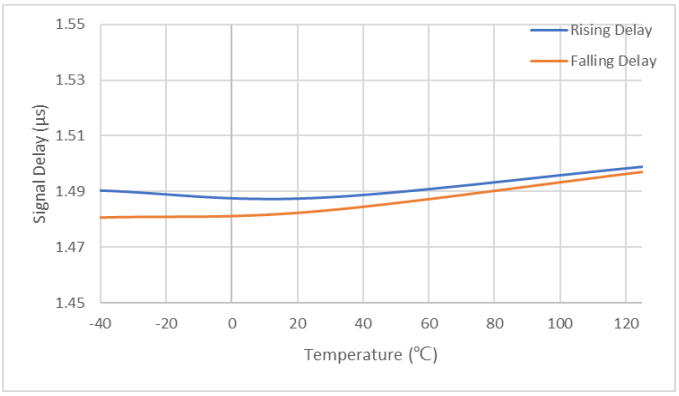


Figure 5.15 Vin to Vout Delay vs Temperature

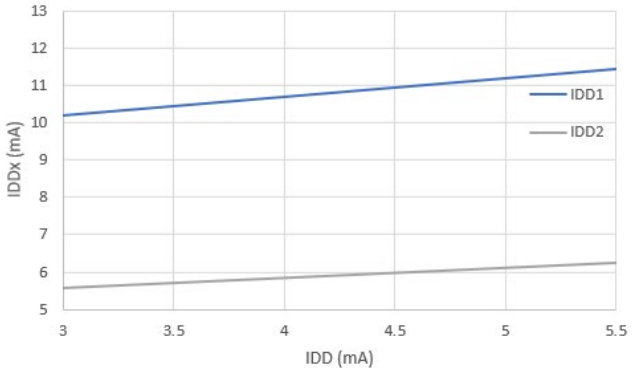


Figure 5.16 Supply Current vs Supply Voltage

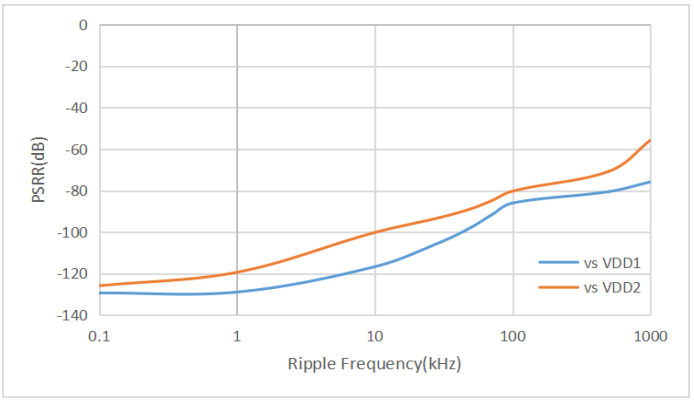


Figure 5.17 Power-Supply Rejection Ratio vs Ripple Frequency

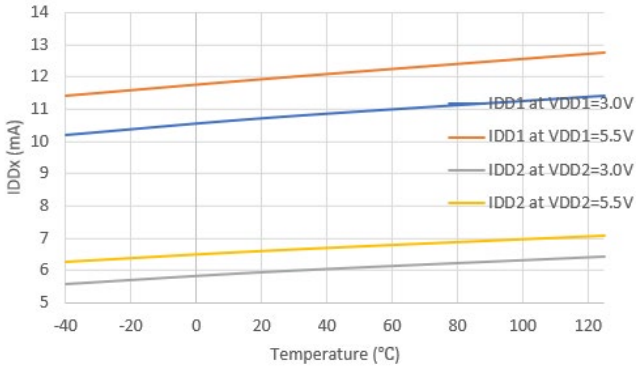


Figure 5.18 Supply Current vs Temperature

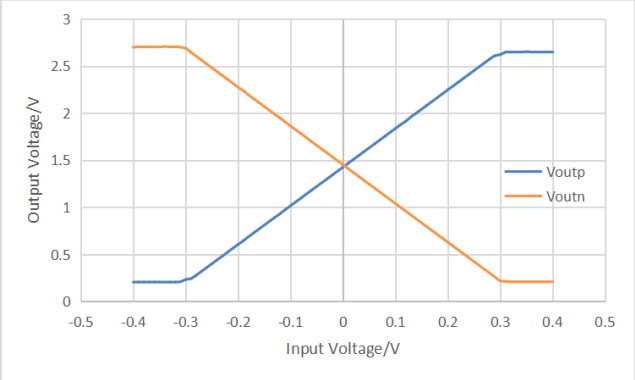


Figure 5.19 Output Voltage vs Input Voltage

5.3. Parameter Measurement Information

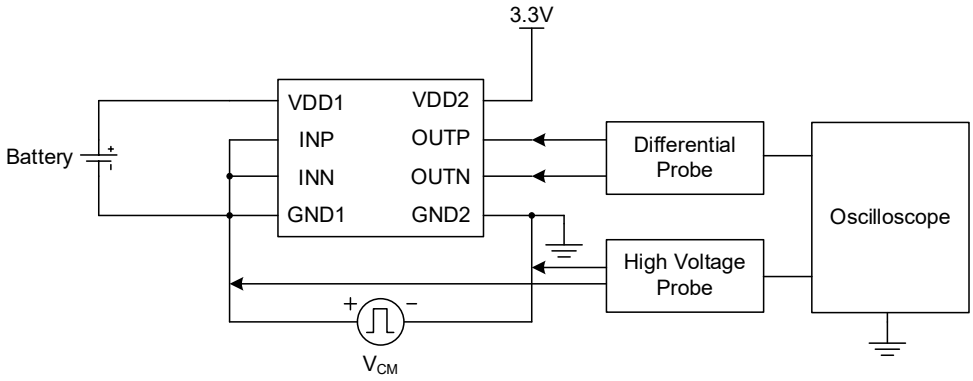


Figure 5.1 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Clearance	CLR	15	mm	IEC 60664-1:2007
Minimum External Creepage	CPG	15	mm	IEC 60664-1:2007
Distance Through Insulation	DTI	32	μm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		IEC 60664-1

Description	*Test Condition*	*Value*
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms	I to IV
	For Rated Mains Voltage ≤ 300Vrms	I to IV
	For Rated Mains Voltage ≤ 600Vrms	I to IV
	For Rated Mains Voltage ≤ 1000Vrms	I to III
Climatic Classification		40/125/21
Pollution Degree per DIN VDE 0110,		2

6.2. Insulation Characteristics

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Maximum repetitive isolation voltage		V_{IORM}	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	1500	V_{RMS}
	DC Voltage		2121	V_{DC}
Apparent Charge	Method a, after Input/output safety test subgroup 2/3, Vini=V_{IOTM}, t_{ini} = 60 s , $V_{pd(m)}$=1.2*V_{IORM}, t_m=10s.	q_{pd}	<5	pC
	Method a, after environmental tests subgroup 1, Vini=V_{IOTM}, t_{ini}=60s ,$V_{pd(m)}$=1.6*V_{IORM}, t_m=10s			

Description	Test Condition	Symbol	Value	Unit
	Method b, routine test (100% production) and preconditioning (type test);V_{ini}=1.2*V_{IOTM}, t_{ini}=1s $V_{pd(m)}$=1.875*V_{IORM}, t_m=1s（method b1）or $V_{pd(m)}$=Vini, t_m=t_{ini}(method b2)			
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	10600	Vpeak
Maximum impulse voltage	Tested in air, 1.2/50-us waveform per IEC62368-1	V_{IMP}	6250	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{IOSM} \geqslant V_{IMP} \times 1.3$	V_{IOSM}	12800	V_{PEAK}
Isolation resistance	V_{IO} =500V, T_{amb}=25℃	R_{IO}	>10^{12}	Ω
	V_{IO} =500V, 100℃ ≤ T_{amb} ≤ 125℃	R_{IO}	>10^{11}	Ω
	V_{IO} =500V, T_{amb}=T_s	R_{IO}	>10^{9}	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Ps	792	mW
Safety input, output, or supply current	V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Ps	158	mA
Maximum safety temperature		Ts	150	℃
UL1577				
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production test)	V_{ISO}	7500	V_{RMS}

6.3. Regulatory Information

The NSI1300D25-DSWWAR are approved or pending approval by the organizations listed in table

UL		*VDE*	*CQC*	*TUV*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1	Certified According to EN IEC 62368-1
Single Protection, 7500V_{rms} Isolation voltage	Single Protection, 7500V_{rms} Isolation voltage	Reinforce Insulation V_{IORM}=2121Vpeak VIOTM=10600Vpeak VIOSM=12800Vpeak	Reinforced insulation	7500Vrms for 1min
File (pending)	File (pending)	File (pending)	CQC24001426054	File (pending)

7. Function Description

7.1. Overview

The NSI1300D25-DSWWAR is a high performance isolated amplifier that accept fully-differential input. The fully-differential input is ideally suited to shunt current monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ-Δ modulator in the device, which is driven by a pre-stage fully-differential amplifier in the device. With the internal voltage reference and clock generator, the modulator convert the analog input signal to a digital bitstream. The output of the modulator is transferred by the drivers (called TX in the Functional Block Diagram) across the isolation barrier that separates the isolated side1 and side2 voltage. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order analog filter on the side2 and has a differential output.

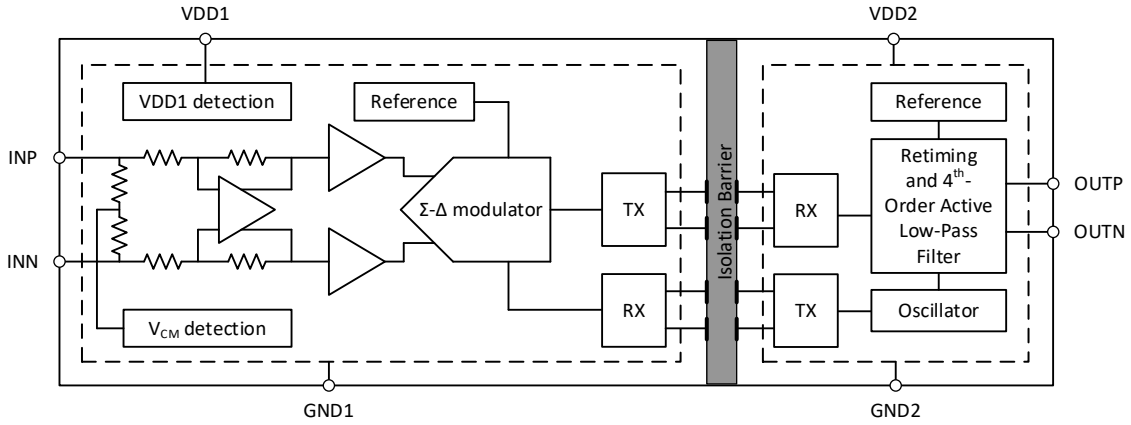


Figure 7.1 Function Block Diagram

7.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range GND1 – 6 V to VDD1 + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

7.3. Analog Output

For linear input range, the analog output of NSI1300D25-DSWWAR has a fixed gain of 8.2. If a full-scale input signal is applied between VINP & VINN ($V_{IN} \geq V_{Clipping}$), the analog output will be clipped (typically, 2.45V for positive clipping and -2.45V for negative clipping).

In addition, NSI1300D25-DSWWAR integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage that does not occur under normal device operation, and it will only be activated in following conditions:

- When the undervoltage of VDD1 is detected (VDD1< $VDD1_{UV}$).
- When the overvoltage of common-mode input voltage is detected (V_{CM}>V_{CMov}).

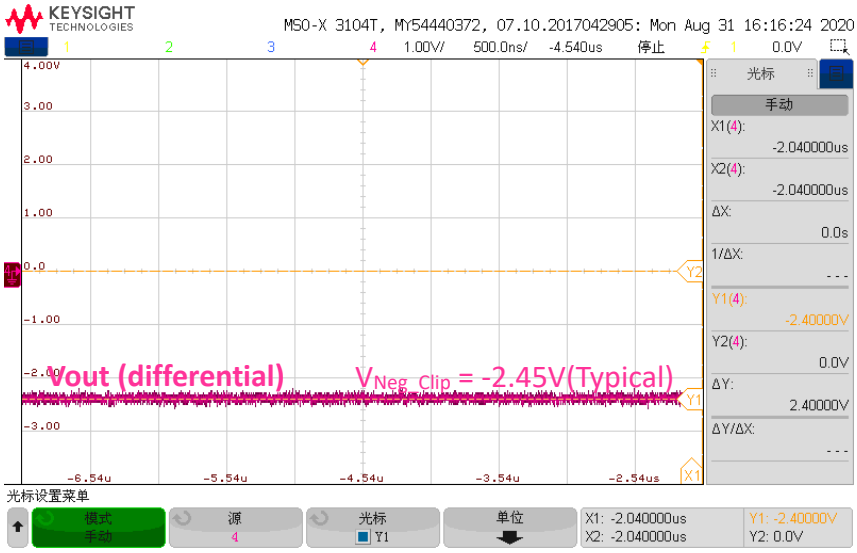


Figure 7.2 Typical negative clipping output

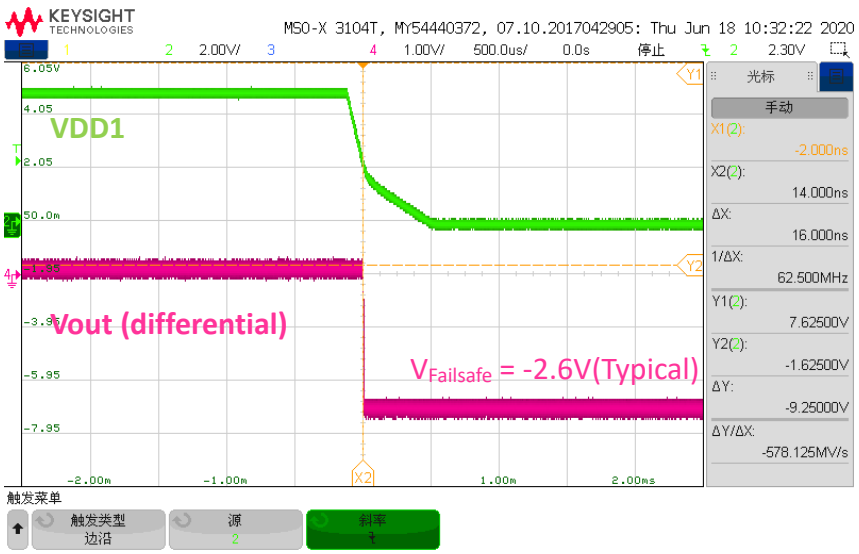


Figure 7.3 Typical Failsafe output when VDD1 undervoltage

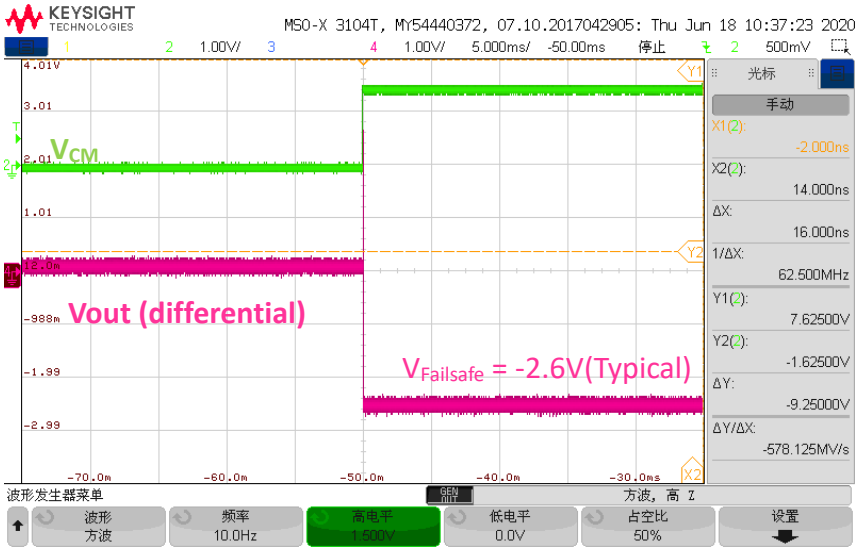


Figure 7.4 Typical Failsafe output when input common mode signal overvoltage

8. Application Note

8.1. Typical Application Circuit

NSI1300D25-DSWWAR is ideally suited to shunt resistor-based current sensing in high voltage applications such as frequency inverters. The typical application circuit is shown in Figure 8.1.

The voltage across the shunt resistor R_{sense} is applied to the differential input of NSI1300D25-DSWWAR through a RC filter. The differential output of the isolated amplifier is converted to a single-ended analog output with an operational-amplifier-based circuit. Suggest to add >1kΩ resistor on the OUTP and OUTN pin to prevent output over-current. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

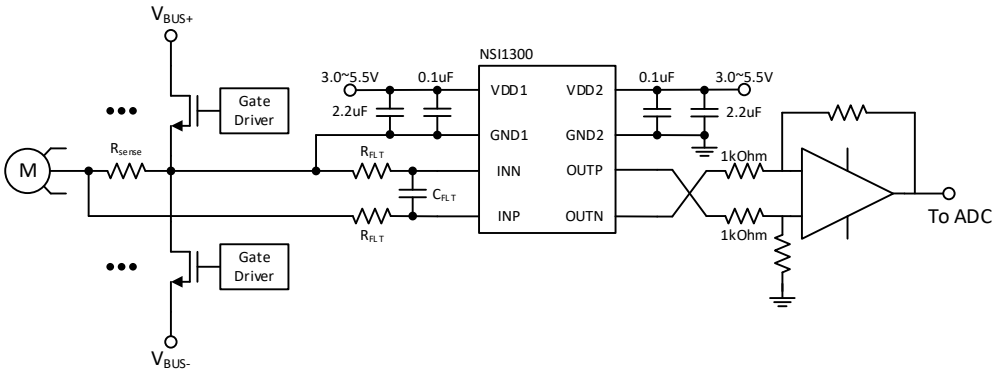


Figure 8.1 Typical application circuit in phase current sensing

8.2. Shunt Resistor Selection

Choosing a particular shunt resistor is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller sense resistor decreases power dissipation, while larger sense resistor can improve measure accuracy by utilizing the full input range of isolated amplifier.

There are two other factors should be considered when selecting the shunt resistor:

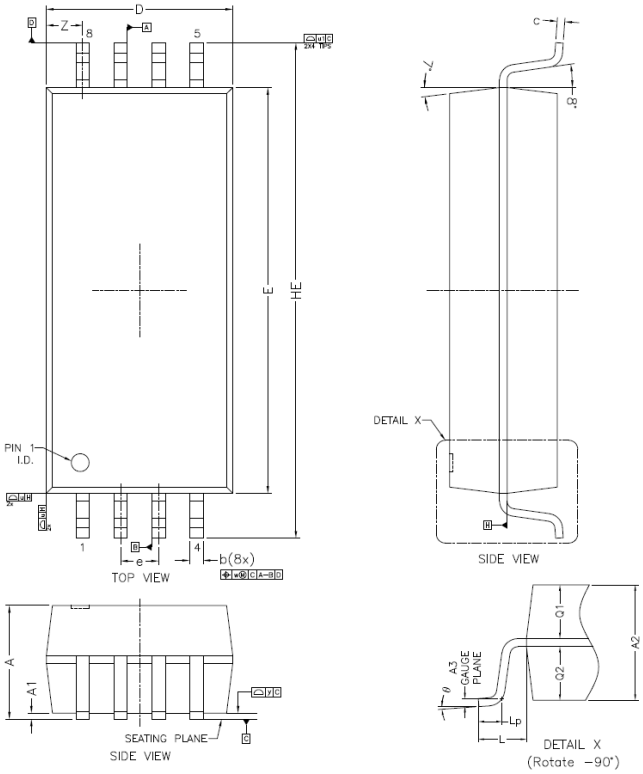
- The voltage-drop caused by the rated current range must not exceed the recommended linear input voltage range: $V_{SHUNT} \leq$ FSR.
- The voltage-drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$.

8.3. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1300 requires a 0.1μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10μF capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1300. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1300. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

9. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	3.580	3.807	4.034
A1	0.100	0.200	0.300
A2	3.480	3.607	3.734
b	0.357	0.457	0.557
c	0.254 REF		
D	6.121	6.248	6.375
E	13.473	13.600	13.727
HE	16.360	16.610	16.860
Q1	1.6515	1.6765	1.7015
Q2	1.6515	1.6765	1.7015
e	1.27 BSC		
A3	0.25 BSC		
L	1.505 REF		
Lp	0.635	--	--
w	0.25		
y	0.10		
u	0.10		
u1	0.20		
Z	0.525		
θ	0°	--	8°

Figure 9.1 SOP8(600mil)/SOWW8 Package Shape and Dimension in millimeters

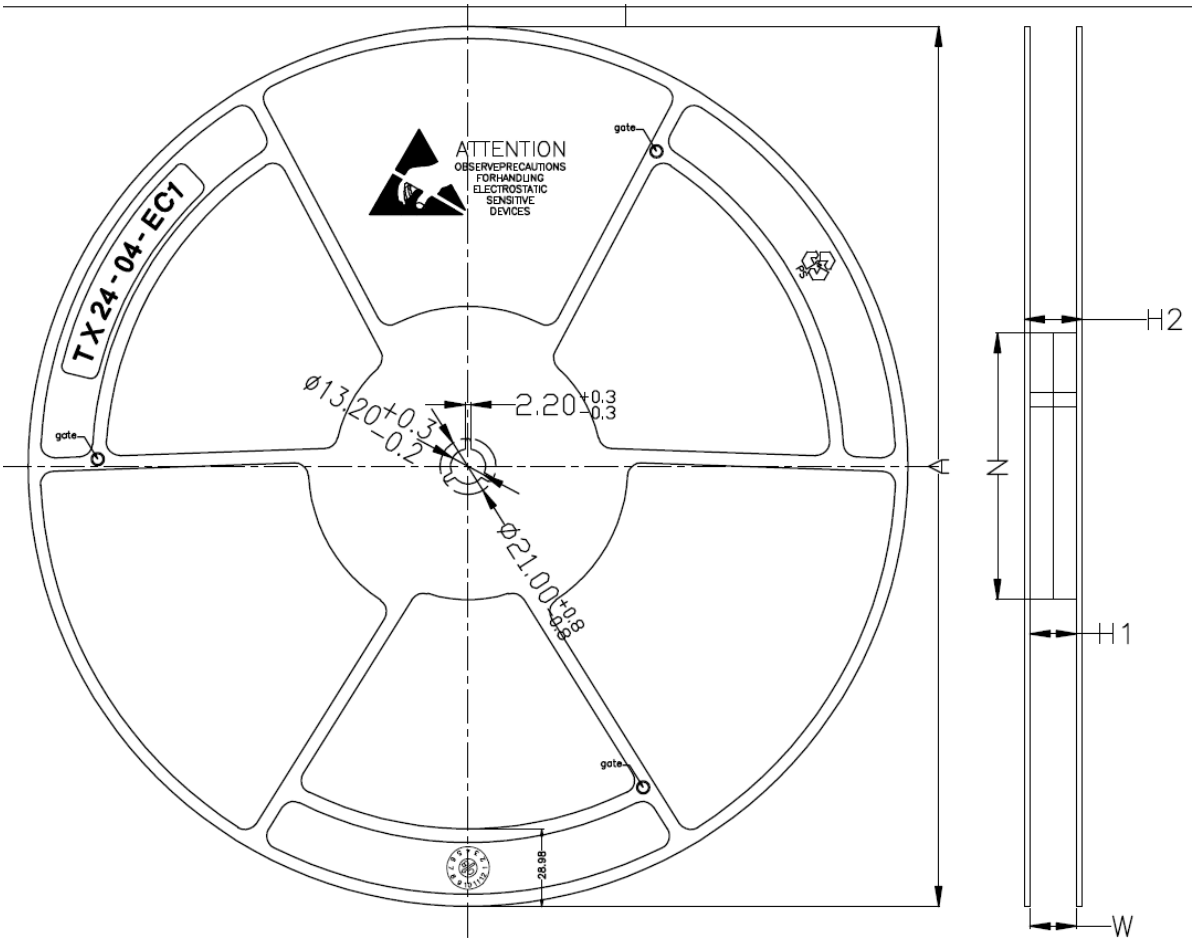
10. Ordering Information

Part No.	*Isolation Rating(kV)*	*Linear Input Range(mV)*	*Moisture Sensitivity Level*	*Temperature*	*Automotive*	*Package Type*	*Package Drawing*	*SPQ*
NSI1300D25 - DSWWAR	7.5	-250 ~ 250	Level-3	-40 to 125℃	NO	SOP8 (600mil)	SOWW8	1000

11. Documentation Support

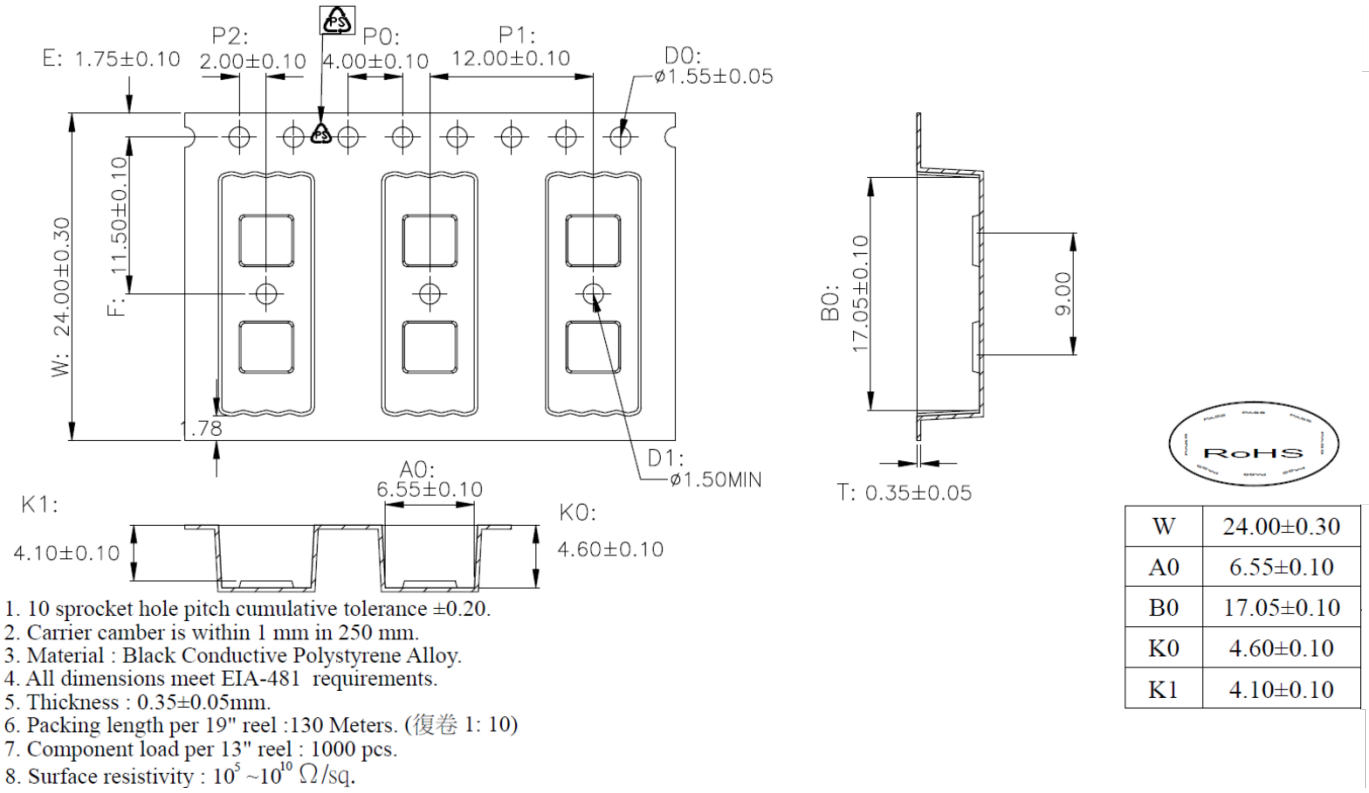
Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSI1300D25-DSWWAR	Click here	Click here	Click here	Click here

12. Tape and Reel Information



PRODUCT SPECIFICATIONS					
TAPE WIDTH	ØA $^{+2}_{-2}$	ØN $^{+2}_{-2}$	H1 $^{+2}_{-0}$	H2 $^{+1}_{-1}$	W $^{+3.5}_{-0.2}$
24MM	330	100	24.4	28.6	24.4

NOTES:
1.MATERIAL:DISSIPATIVE(BLACK)
2.FLANGE WARPAGE:3 MM MAXIMUM 5
3.ALL DIMENSIONS ARE IN MM
4.ESD - SURFACE RESISTIVITY-10 TO 10 OHMS/SQ
5.GENERAL TOLERANCE: ±0.25 MM



1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.35±0.05mm.
6. Packing length per 19" reel :130 Meters. (復卷 1: 10)
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity : 10^5 ~10^{10} Ω/sq.

W	24.00±0.30
A0	6.55±0.10
B0	17.05±0.10
K0	4.60±0.10
K1	4.10±0.10

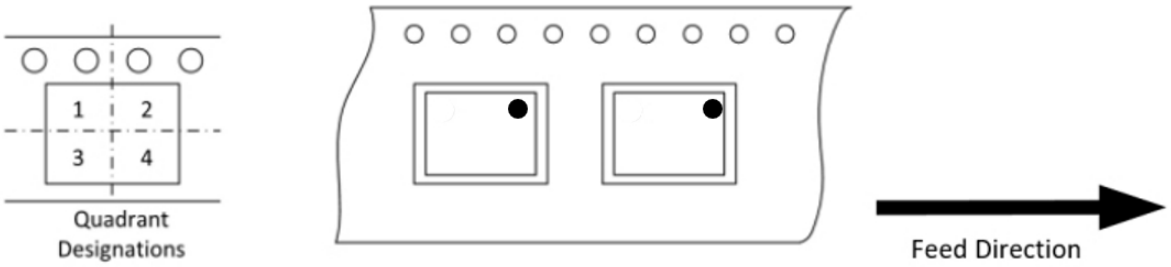


Figure 12.1 Tape and Reel Information of SOP8(600mil)

13. Revision History

Revision	Description	Date
1.0	Initial Version.	2024/9/24

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