

DUAL LOW VOLTAGE POWER AMPLIFIER

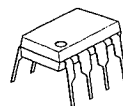
■ GENERAL DESCRIPTION

The NJM2073 is a monolithic integrated circuit in 8 lead dual-in-line package, which is designed for dual audio power amplifier in portable radio and handy cassette player.

■ FEATURES

- Operating Voltage $V^+ = 1.8 \sim 15V$
- Low Crossover Distortion
- Low Operating Current
- Bridge or Stereo Configuration
- No Turn-on Noise
- Package Outline DIP8, DMP8, SIP9
- Bipolar Technology

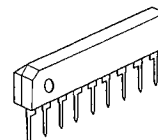
■ PACKAGE OUTLINE



NJM 2073 D

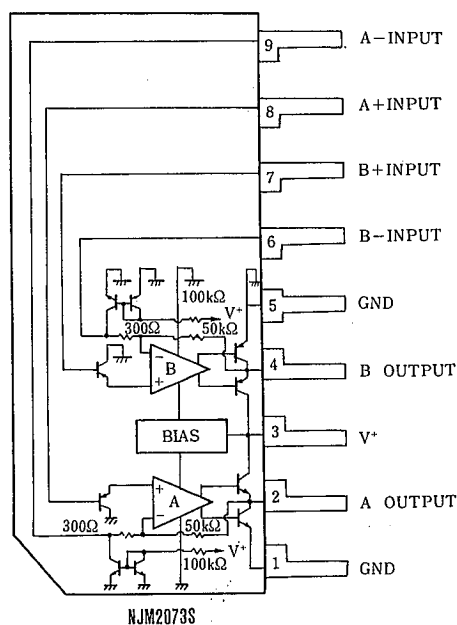
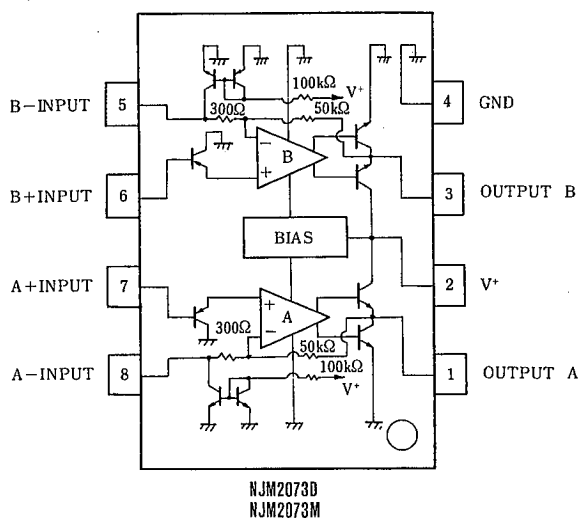


NJM 2073 M



NJM 2073 S

■ PIN CONFIGURATION



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V ⁺	.15	V
Output Peak Current	I _{OP}	1	A
Power Dissipation	P _D	(DIP8) 700 (SIP9) 700 (DMP8) 300	mW
Input Voltage Range	V _{IN}	±0.4	V
Operating Temperature Range	T _{opr}	-40 ~ +85	°C
Storage Temperature Range	T _{stg}	-40 ~ +125	°C

■ ELECTRICAL CHARACTERISTICS

(1) BTL Configuration (Test Circuit Fig. 1)

(V⁺=6V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V ⁺		1.8	—	15	V
Operating Current	I _{CC}	R _L = ∞	—	6	9	mA
Output Offset Voltage (Between the Outputs)	ΔV _O	R _L = 8Ω	—	10	50	mV
Input Bias Current	I _B		—	100	—	nA
Output Power	P _O	THD=10%, f=1kHz	—	2.0	—	W
	P _O	V ⁺ =9V, R _L =16Ω (Note)	—	1.2	—	W
	P _O	V ⁺ =6V, R _L =8Ω (Note)	0.9	0.6	—	W
	P _O	V ⁺ =4.5V, R _L =8Ω	—	0.8	—	W
	P _O	V ⁺ =4.5V, R _L =4Ω (Note)	—	—	—	W
	P _O	V ⁺ =3V, R _L =4Ω	200	300	—	mW
	P _O	V ⁺ =2V, R _L =4Ω	—	80	—	mW
	P _O	THD=1%, f=40kHz~15kHz	—	—	—	—
	P _O	V ⁺ =6V, R _L =8Ω	—	1.0	—	W
	P _O	V ⁺ =4.5V, R _L =4Ω	—	0.6	—	W
Total Harmonic Distortion	THD	P _O =0.5W, R _L =8Ω, f=1kHz	—	0.2	—	%
Close Loop Voltage Gain	A _V	f=1kHz	41	44	47	dB
Input Impedance	Z _{IN}	f=1kHz	100	—	—	kΩ
Equivalent Input Noise Voltage	V _{NI1}	R _S =10kΩ, A Curve	—	2	—	μV
	V _{NI2}	R _S =10kΩ, B=22Hz~22kHz	—	2.5	—	μV
Ripple Rejection	RR	f=100Hz	—	40	—	dB
Cutoff Frequency	f _H	A _V =-3dB from f=1kHz, R _L =8Ω, P _O =1W	—	130	—	kHz

(Note) At on PC Board

(2) Stereo Configuration (Test Circuit Fig. 2)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V ⁺		1.8	—	15	V
Output Voltage	V _O		—	2.7	—	V
Operating Current	I _{CC}	R _L = ∞	—	6	9	mA
Input Bias Current	I _B		—	100	—	nA
Output Power (Each Channel)		THD=10%, f=1kHz				
	P _O	V ⁺ =6V, R _L =4Ω (Note)	0.5	0.65	—	W
	P _O	V ⁺ =4.5V, R _L =4Ω	—	0.32	—	W
	P _O	V ⁺ =3V, R _L =4Ω	—	120	—	mW
	P _O	V ⁺ =2V, R _L =4Ω	—	30	—	mW
		THD=1%, f=1kHz				
	P _O	V ⁺ =6V, R _L =4Ω	—	500	—	mW
	P _O	V ⁺ =4.5V, R _L =4Ω	—	250	—	mW
Total Harmonic Distortion	THD	P _O =0.4W, R _L =4Ω, f=1kHz	—	0.25	—	%
Voltage Gain	A _V	f=1kHz	41	44	47	dB
Channel Balance	ΔA _V		—	—	±1	dB
Input Impedance	Z _{IN}	f=1kHz	100	—	—	kΩ
Equivalent Input Noise Voltage	V _{NI1}	R _S =10kΩ, A Curve	—	2.5	—	μV
	V _{NI2}	R _S =10kΩ, B=22Hz~22kHz	—	3	—	μV
Ripple Rejection	RR	f=100Hz, C _X =100μF	24	30	—	dB
Cutoff Frequency	f _H	A _V =-3dB from f=1kHz R _L =8Ω, P _O =250mW	—	200	—	kHz

(Note) At on PC Board

■ ELECTRICAL CHARACTERISTICS M-Type

(1) BTL Configuration (Test Circuit Fig. 1)

(V⁺=6V, T_a=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V ⁺		1.8	—	15	V
Operating Current	I _{CC}	R _L = ∞	—	6	9	mA
Output Offset Voltage (Between the Outputs)	ΔV _{CO}	R _L =8Ω	—	10	50	mV
Input Bias Current	I _B		—	100	—	nA
Output Power		THD=10%, f=1kHz				
	P _O	V ⁺ =6V, R _L =16Ω (Note)	—	0.8	—	W
	P _O	V ⁺ =4V, R _L =8Ω (Note)	350	460	—	mW
	P _O	V ⁺ =3V, R _L =4Ω (Note)	200	300	—	mW
	P _O	V ⁺ =2V, R _L =4Ω	—	80	—	mW
		THD=1%, f=40Hz~15kHz				
	P _O	V ⁺ =4V, R _L =8Ω	—	380	—	mW
Total Harmonic Distortion	THD	V ⁺ =4V, R _L =8Ω, P _O =200mW, f=1kHz	—	0.2	—	%
Close Loop Voltage Gain	A _V	f=1kHz	41	44	47	dB
Input Impedance	Z _{IN}	f=1kHz	100	—	—	kΩ
Equivalent Input Noise Voltage	V _{NI1}	R _S =10kΩ, A Curve	—	2	—	μV
	V _{NI2}	R _S =10kΩ, B=22Hz~22kHz	—	2.5	—	μV
Ripple Rejection	RR	f=100Hz	—	40	—	dB
Cutoff Frequency	f _H	A _V =-3dB from f=1kHz, R _L =16Ω, P _O =0.5W	—	130	—	kHz

(Note) At on PC Board

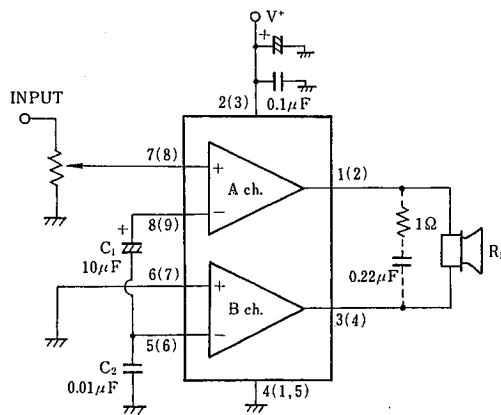
(2) Stereo Configuration (Test Circuit Fig. 2)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V ⁺		1.8	—	15	V
Output Voltage	V _O		—	2.7	—	V
Operating Current	I _{CC}	R _L = ∞	—	6	9	mA
Input Bias Current	I _B		—	100	—	nA
Output Power (Each Channel)	P _O	THD = 10%, f = 1kHz				
	P _O	V ⁺ = 6V, R _L = 16Ω	—	240	—	mW
	P _O	V ⁺ = 5V, R _L = 8Ω (Note)	—	270	—	mW
	P _O	V ⁺ = 4V, R _L = 4Ω (Note)	180	250	—	mW
	P _O	V ⁺ = 3V, R _L = 4Ω	—	120	—	mW
	P _O	V ⁺ = 2V, R _L = 4Ω	—	30	—	mW
	P _O	THD = 1%, f = 1kHz				
	P _O	V ⁺ = 4V, R _L = 4Ω	—	180	—	mW
Total Harmonic Distortion	THD	V ⁺ = 4V, R _L = 4Ω, P _O = 150mW, f = 1kHz	—	0.25	—	%
Voltage Gain	A _V	f = 1kHz	41	44	47	dB
Channel Balance	ΔA _V		—	—	±1	dB
Input Impedance	Z _{IN}	f = 1kHz	100	—	—	kΩ
Equivalent Input Noise Voltage	V _{N1}	R _S = 10kΩ, A Curve	—	2.5	—	μV
	V _{N12}	R _S = 10kΩ, B = 22Hz ~ 22kHz	—	3	—	μV
Ripple Rejection	RR	f = 100Hz, C _X = 100μF	24	30	—	dB
Cutoff Frequency	f _H	A _V = -3dB from f = 1kHz	—	200	—	kHz
		R _L = 16Ω, P _O = 125mW				

(Note) At on PC Board

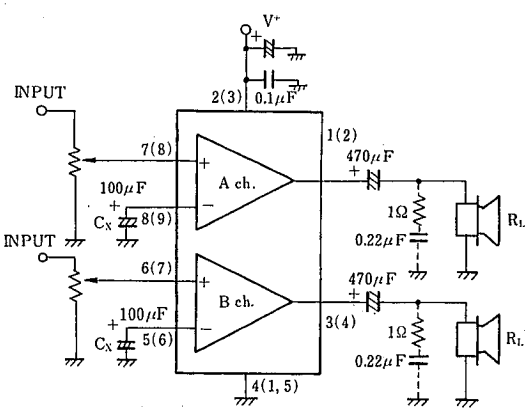
■ TYPICAL APPLICATION & TEST CIRCUIT

Fig.1 BTL Configuration



note: pin No. to D,M-Type
() to S-Type

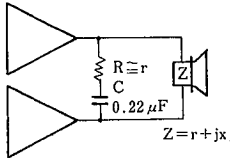
Fig.2 Stereo Configuration



■ PARASITIC OSCILLATION PREVENTING CIRCUIT

Put $1\Omega + 0.22\mu\text{F}$ on parallel to load, if the load is speaker. Recommend putting $0.1\mu\text{F}$ and more than $100\mu\text{F}$ capacitors with good high frequency characteristics in to near ground and supply voltage pins.

In BTL operation of less than 2V supply voltage, parasitic oscillation may be occurred with $R = 1\Omega$. And so recommended R to be the same value of pure resistance(r) when it is lower than 3V.



■ MUTING CIRCUIT

When Mute ON, OUTPUT level saturates to GND side.

Fig.3 BTL Configuration

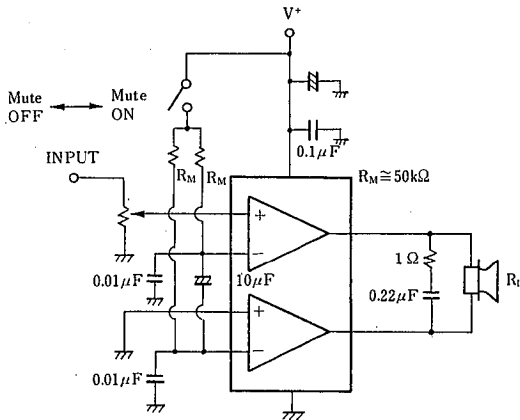
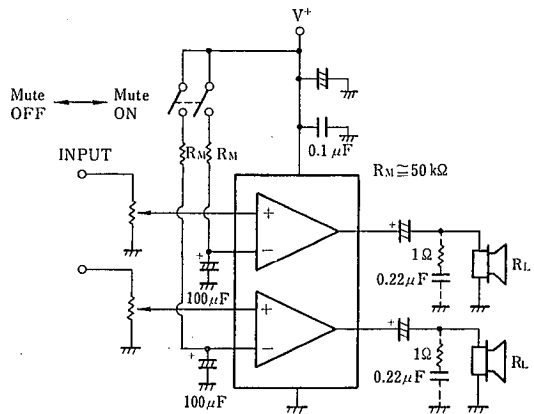


Fig.4 Stereo Configuration



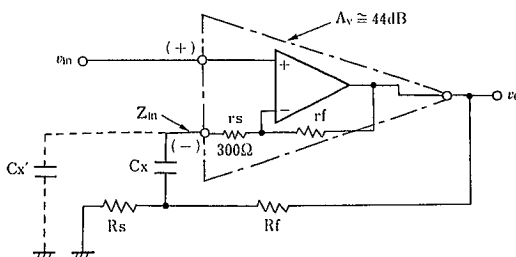
■ VOLTAGE GAIN REDUCTION APPLICATION EXAMPLE

(1) Outline of way to further Reduction

NJM2073 by taking in assumption, as one of OP-AMP (Gain 44dB, minus input impedance about 300Ω), to feedback from output to minus input helps to get reduction of stablized voltage Gain. Fig.5 indicates the model example.

Here is the point to be noticed that, in order to get the appropriate output Bias Voltage, it is important to keep the minus input floating as DC condition,(inserting C_x), and also that when extended too much reduction of Gain might cause Oscillation due to high band phase margin. The reduction of voltage gain is limited at around 26 dB(20 times), and when oscillation, it in necessary to attach the oscillation atopper. Please examine the C_x value accordingly to the application requirement.

Fig.5 Model of Voltage Gain Reduction



$$A_v = \frac{v_o}{v_{in}} \approx \frac{R_s + R_f}{R_s + \frac{R_s \times R_f}{160} + \frac{R_s \times R_f}{160 \times 300}} \quad (\text{倍})$$

(Av) (Av)(Zin)

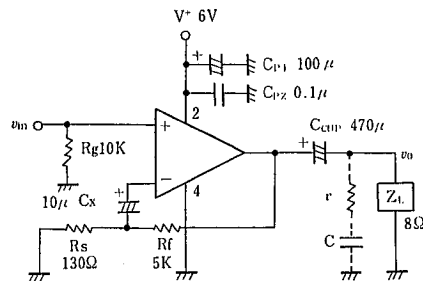
(2) The Application Example of Voltage Gain Reduction.(STEREO)

Fig.6 indicates the application example and Table 1 indicates the recommendable value of parts to be attached externally.

Table 1, Applying purpose and Recommended Value of Externally parts to be attached.

EXTERNAL PARTS	APPLICATION PURPOSE	RECOMMENDED VALUE	REMARKS
R_g	Plus input to be grounded by fixed DC	Under about $100k\Omega$	Catch the noise when much higher.
R_s	AV shall be decided with R_f	—	The co-temperature of AV becomes higher in case when R_s is higher resistance. The current from output pin to GND becomes higher, in case when R_s is lower resistance. (The current sinks in vain.)
R_f	AV shall be decided with R_s	About $5k\Omega$	
C_x	Minus input to be grounded by fixed DC	—	Low-band Cut off frequency (f_L) is to be decided.
C_{cup}	Output DC Decoupling	When $R_L = 8\Omega$, More than $220\mu F$	The rise time becomes longer in case that C_x is big. f_L shall be decided by C_{cup} and Z_L .
C_{p1}	Stabilization of V^+	More than about C_{cup}	Inserting near around V^+ pin and GND .pin.
C_{p2}	Prevention of Oscillation	More than $0.1\mu F$	
r	"	About R_L	"
C	"	$0.22\mu F$	To be examined by about the resisitor volume of the speaker load.

Fig.6 STEREO Application Example.



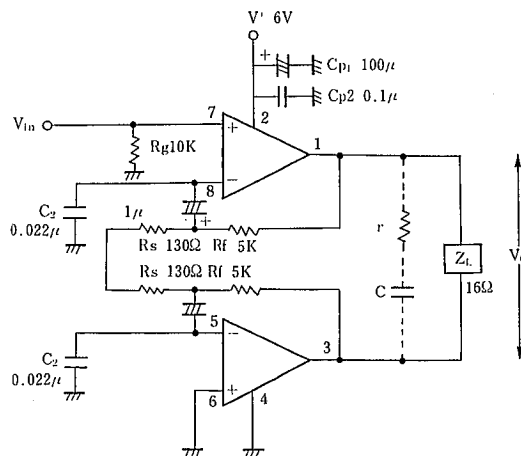
● Application for Voltage Gain Reduction (BTL)

Fig.7 indicates the application example, Table 2 shows recommended value of externally attaching parts.

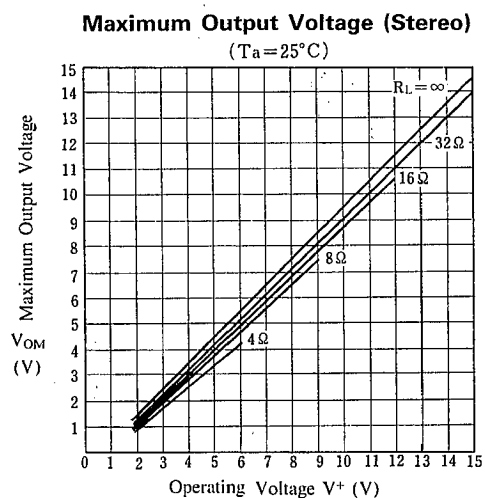
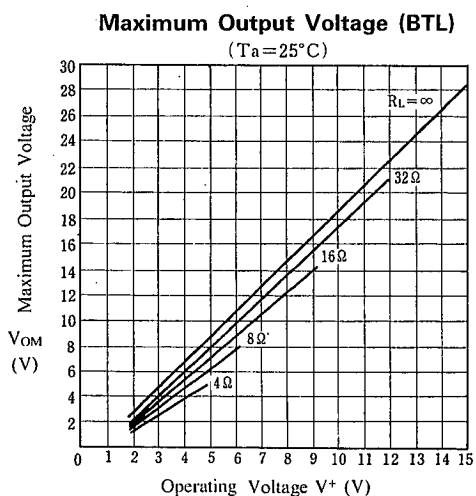
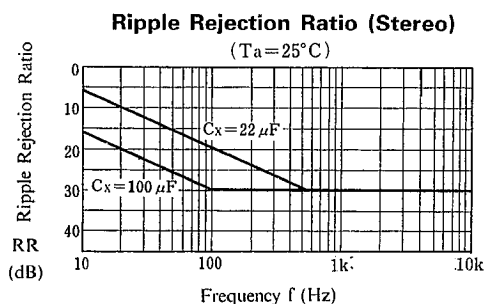
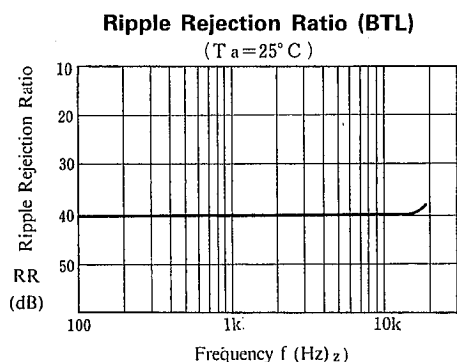
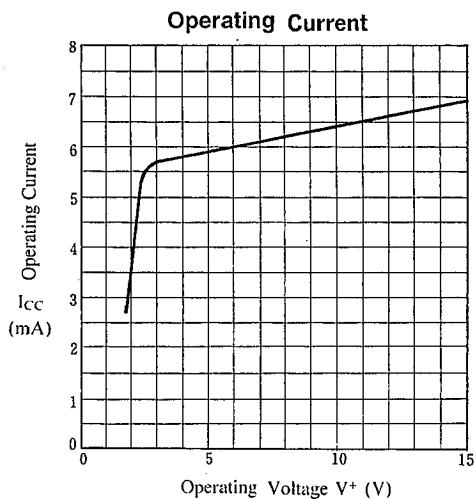
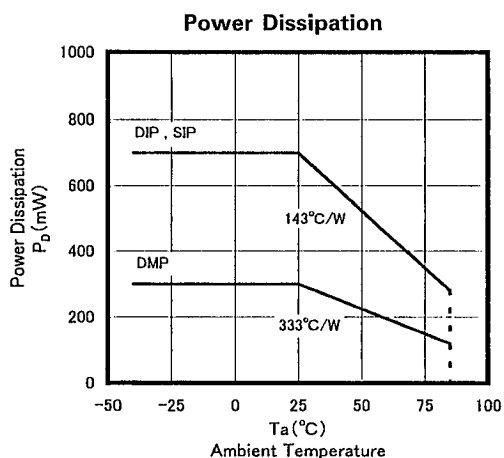
Table 2 Applying purpose and Recommended Value of External Part

EXTERNAL PARTS	APPLICATION PURPOSE	RECOMMENDED VALUE	REMARKS
R_B	DC condition ground of plus input	Below about $10k\Omega$	Making noise when higher.
R_s	AV shall be decided with R_f		
R_f	AV shall be decided with R_s	About $5k\Omega$	Temperature feature to be increased accordingly as in higher AV value. When lower, to be trended of Oscillation.
C_1	Releasing minus input in to DC condition		Setting up low band Cut-off frequency (fL). More higher, the rise time become longer.
C_2	Preventing Oscillation	About $0.02\mu F$	The more higher in value, the high band THD, due to phase slipping to be deteriorated.
C_{P1}	Stability of V^+	more than about $100\mu F$	When lower, to be trended of oscillation.
C_{P2}	Preventing Oscillation	more than $0.1\mu F$	Inserting near around at V^+ and the GND pin.
r	"	About R_L	"
C	"	$0.22\mu F$	To be examined at around pure resistor Value of speaker load.

Fig.7 BTL Application



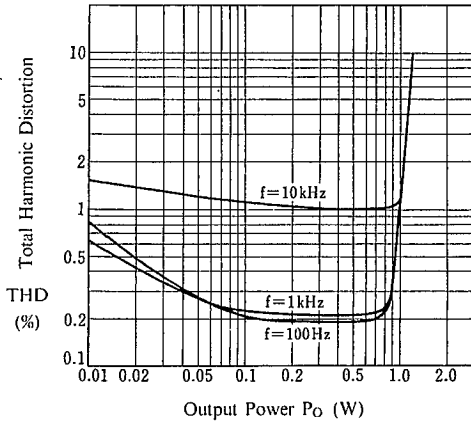
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS

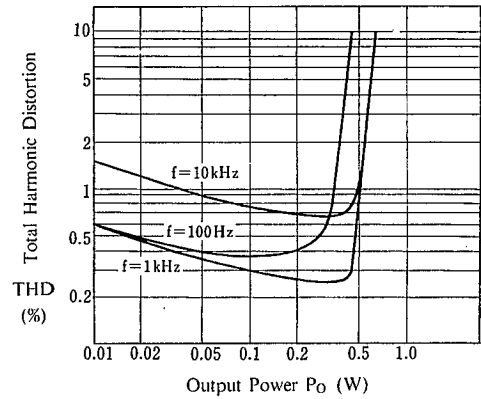
Total Harmonic Distortion (BTL)

($V^+ = 6V$, $R_L = 8\Omega$)

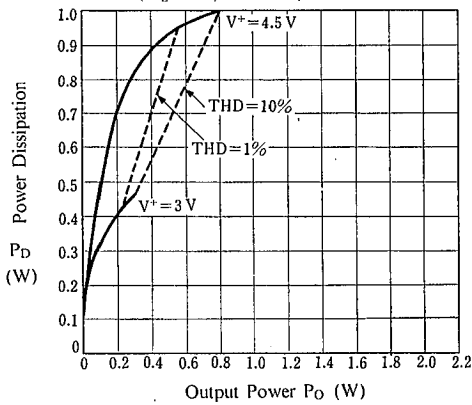


Total Harmonic Distortion (Stereo)

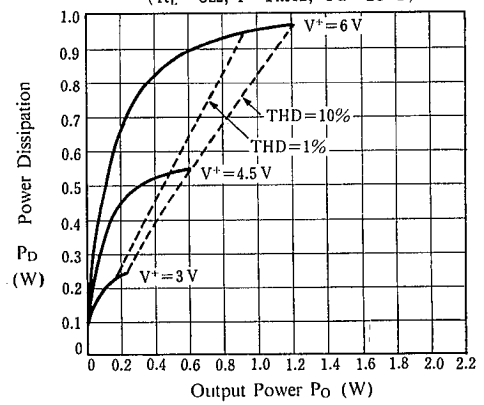
($V^+ = 6V$, $R_L = 4\Omega$)



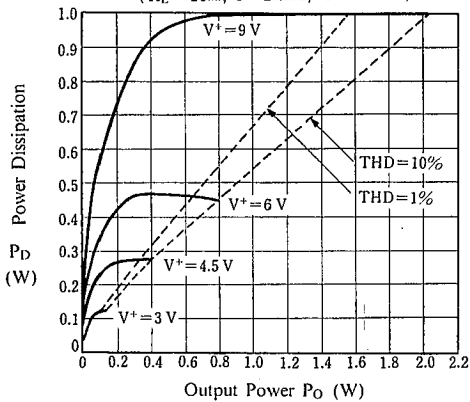
Power Dissipation vs. Output Power (BTL)
($R_L = 4\Omega$, $f = 1kHz$, $T_a = 25^\circ C$)



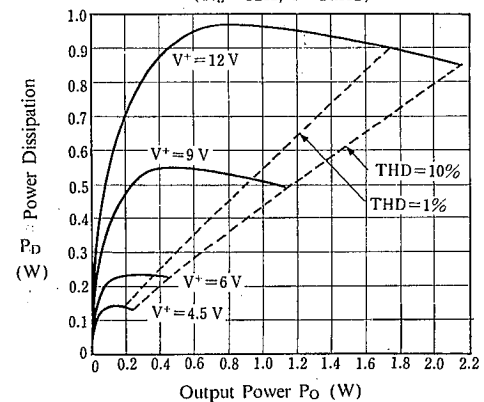
Power Dissipation vs. Output Power (BTL)
($R_L = 8\Omega$, $f = 1kHz$, $T_a = 25^\circ C$)



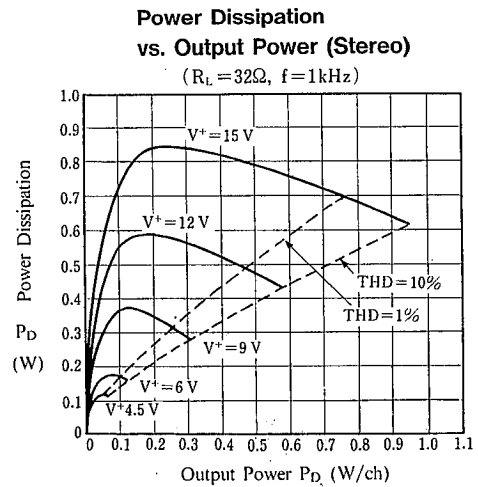
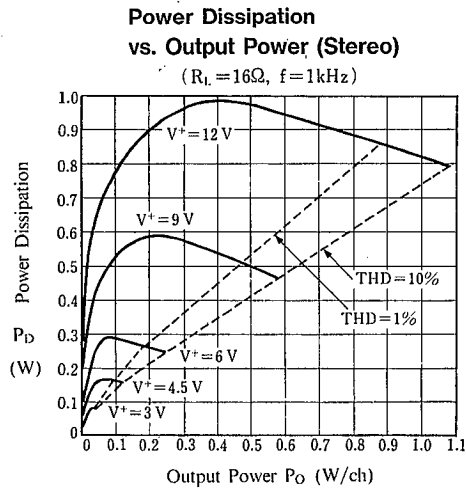
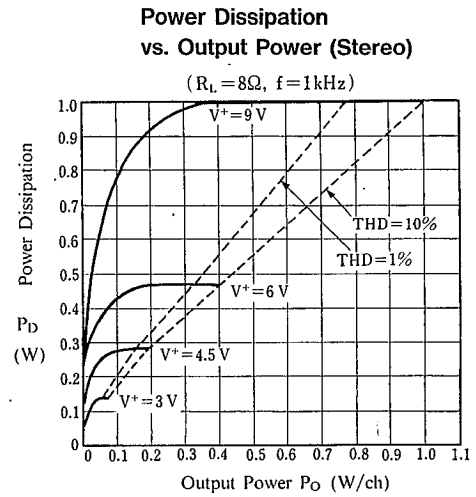
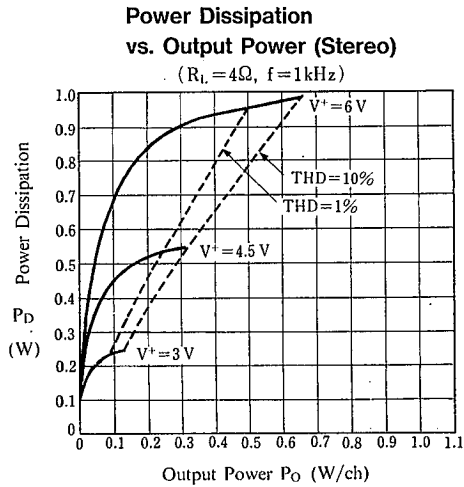
Power Dissipation vs. Output Power (BTL)
($R_L = 16\Omega$, $f = 1kHz$, $T_a = 25^\circ C$)



Power Dissipation vs. Output Power (BTL)
($R_L = 32\Omega$, $f = 1kHz$)

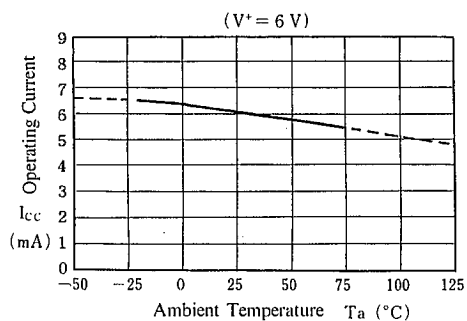


TYPICAL CHARACTERISTICS

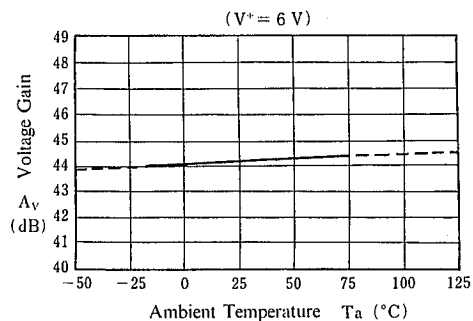


■ TYPICAL CHARACTERISTICS

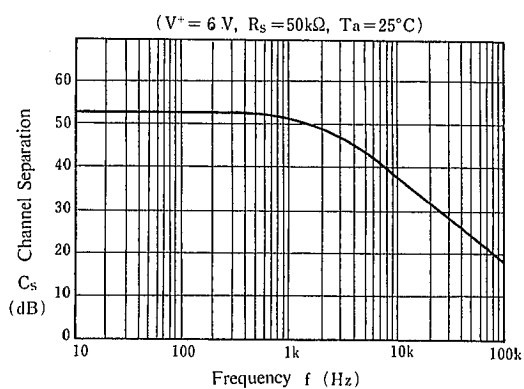
Operating Current vs. Temperature



Voltage Gain vs. Temperature



Channel Separation vs. Frequency



MEMO

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.