



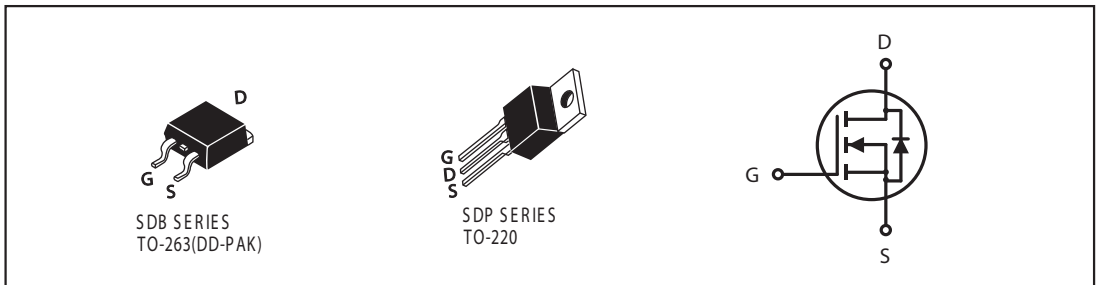
# SDP/B60N03L

## N-Channel Logic Level Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DS</sub>	I <sub>D</sub>	R <sub>DS(on)</sub> (mΩ) Max
30V	56A	11 @ V <sub>GS</sub> = 10V
		19 @ V <sub>GS</sub> = 4.5V

### FEATURES

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- TO-220 & TO-263 package.



### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous @ T <sub>J</sub> =125°C -Pulsed <sup>a</sup>	I <sub>D</sub>	56	A
	I <sub>DM</sub>	168	A
Drain-Source Diode Forward Current	I <sub>S</sub>	60	A
Maximum Power Dissipation @ T <sub>C</sub> =25°C	P <sub>D</sub>	75	W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-65 to 175	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	°C/W

# SDP/B60N03L

ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V			10	uA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±16V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS <sup>a</sup></b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	1.5	3	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =30A		9.5	11	m ohm
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =24A		16	19	m ohm
On-State Drain Current	I <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =10V	60			A
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =26A		32		S
<b>DYNAMIC CHARACTERISTICS <sup>b</sup></b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V f=1.0MHz		1200		pF
Output Capacitance	C <sub>OSS</sub>			550		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			160		pF
<b>SWITCHING CHARACTERISTICS <sup>b</sup></b>						
Turn-On Delay Time	t <sub>D(on)</sub>	V <sub>DD</sub> =15V, I <sub>D</sub> =1A, V <sub>GS</sub> =10V, R <sub>GEN</sub> =60 ohm		25		ns
Rise Time	t <sub>r</sub>			30.5		ns
Turn-Off Delay Time	t <sub>D(off)</sub>			60		ns
Fall Time	t <sub>f</sub>			27.5		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =30A, V <sub>GS</sub> =10V		34.1		nC
		V <sub>DS</sub> =15V, I <sub>D</sub> =30A, V <sub>GS</sub> =4.5V		18.7		nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> =15V, I <sub>D</sub> =30A, V <sub>GS</sub> =10V		6.3		nC
Gate-Drain Charge	Q <sub>gd</sub>			7		nC

# S DP /B 60N03L

## ELECTRICAL CHARACTERISTICS ( $T_c=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS <sup>a</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_s = 26A$		0.9	1.3	V

### Notes

- a. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

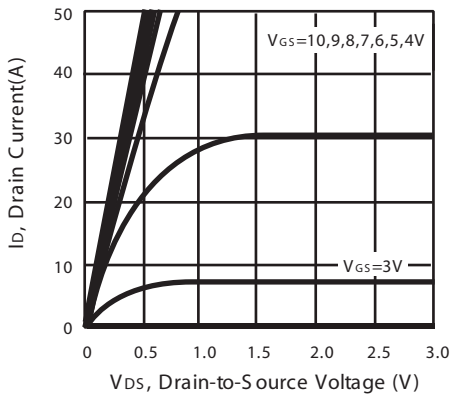


Figure 1. Output Characteristics

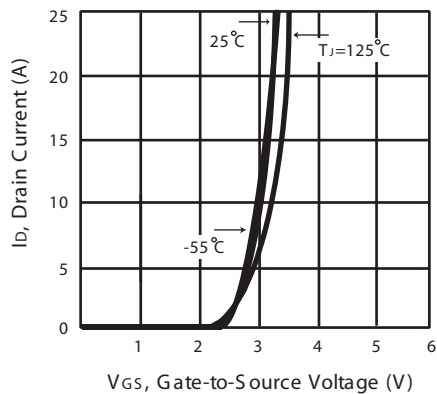


Figure 2. Transfer Characteristics

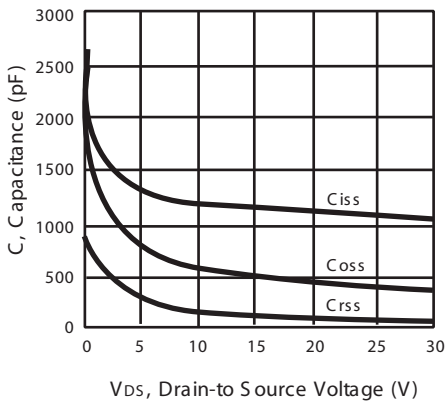


Figure 3. Capacitance

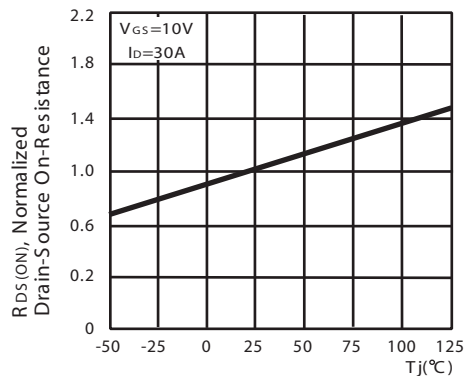


Figure 4. On-Resistance Variation with Temperature

# S DP /B 60N03L

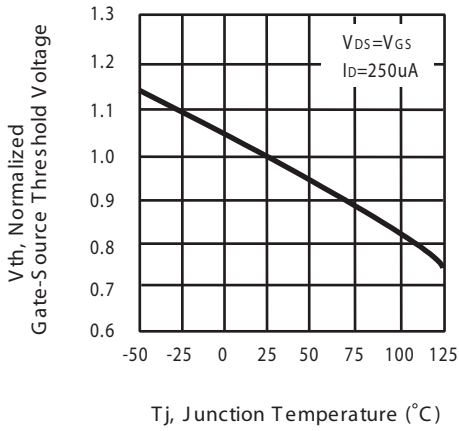


Figure 5. Gate Threshold Variation with Temperature

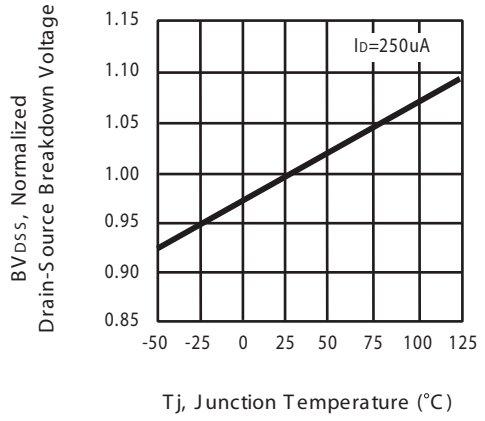


Figure 6. Breakdown Voltage Variation with Temperature

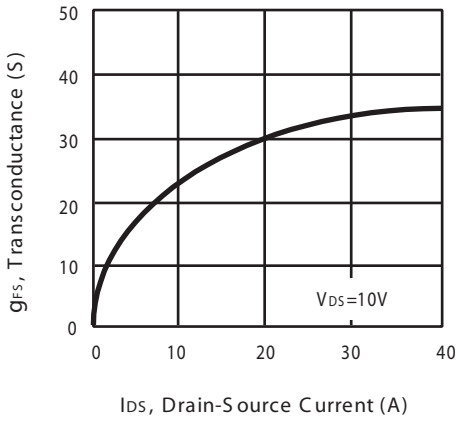


Figure 7. Transconductance Variation with Drain Current

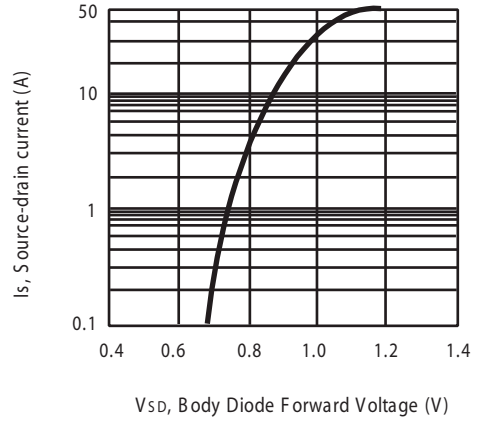


Figure 8. Body Diode Forward Voltage Variation with Source Current

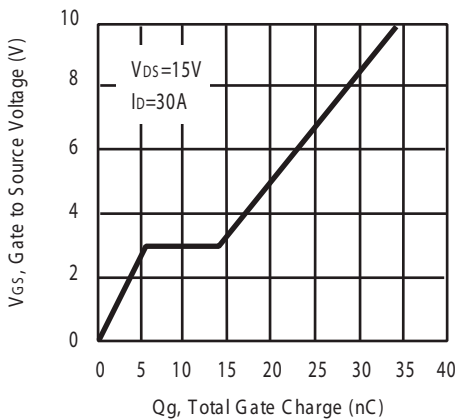


Figure 9. Gate Charge

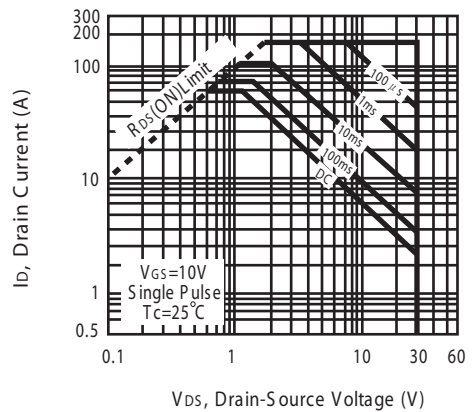


Figure 10. Maximum Safe Operating Area

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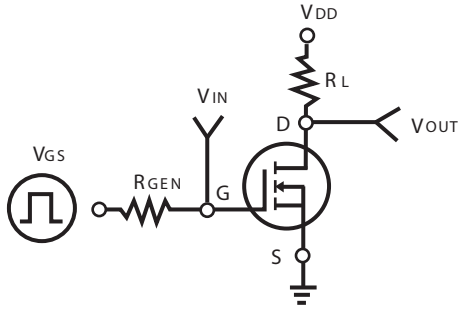


Figure 11. Switching Test Circuit

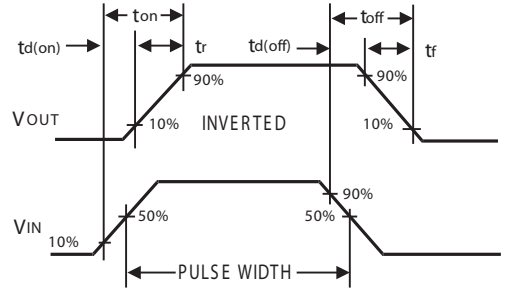


Figure 12. Switching Waveforms

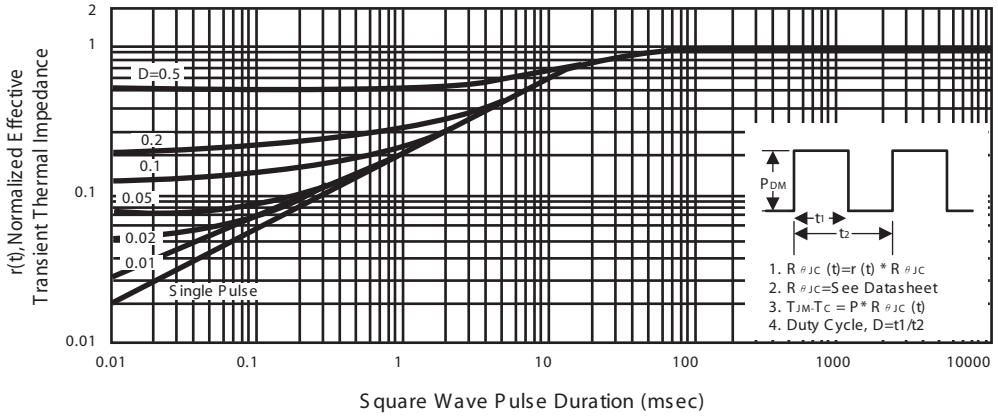
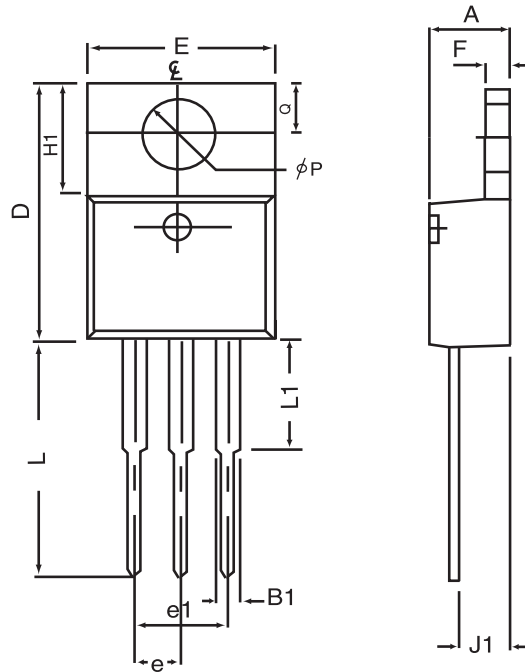


Figure 13. Normalized Thermal Transient Impedance Curve

# SDP/B60N03L

## PACKAGE OUTLINE DIMENSIONS

TO-220



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	4.80	0.170	0.189
B1	1.27	1.65	0.050	0.630
D	14.6	16.00	0.575	0.610
E	9.70	10.41	0.382	0.410
e	2.34	2.74	0.092	0.108
e1	4.68	5.48	0.184	0.216
F	1.14	1.40	0.045	0.055
H1	5.97	6.73	0.235	0.265
J1	2.20	2.79	0.087	0.110
L	12.88	14.22	0.507	0.560
L1	3.00	6.35	0.120	0.250
$\phi P$	3.50	3.94	0.138	0.155
Q	2.54	3.05	0.100	0.120