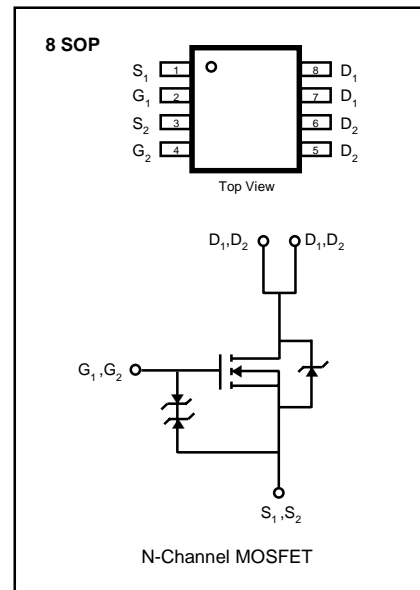


## FEATURES

- ❑ Extremely Lower  $R_{DS(ON)}$
- ❑ Improved Inductive Ruggedness
- ❑ Fast Switching Times
- ❑ Rugged Polysilicon Gate Cell Structure
- ❑ Low Input Capacitance
- ❑ Extended Safe Operating Area
- ❑ Improved High Temperature Reliability
- ❑ Surface Mounting Package : **8SOP**



## Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
$V_{DSS}$	Drain-to-Source Voltage(1)	50	V
$V_{DGR}$	Drain-Gate Voltage( $R_{GS}=1.0M\Omega$ )(1)	50	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current $T_A=25^\circ C$	2.0	A
$I_D$	Continuous Drain Current $T_A=100^\circ C$	1.6	A
$I_{DM}$	Drain Current-Pulsed (2)	8.0	V
$P_D$	Total Power Dissipation $T_A=25^\circ C$ $T_A=70^\circ C$	2.0	W
		1.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	- 55 to +150	$^\circ C$
$T_L$	Maximum Lead Temp. for Soldering Purposes, 1/16" from case for 5 seconds	300	

## Notes ;

(1)  $T_J=25^\circ C$  to  $150^\circ C$ 

(2) Repetitive Rating : Pulse Width Limited by Max. Junction Temperature

### Electrical Characteristics ( $T_A=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$BV_{DSS}$	Drain-Source Breakdown Voltage	600	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$I_{GSS}$	Gate-Source Leakage, Forward	--	--	1.0	$\mu A$	$V_{GS}=20V$
	Gate-Source Leakage, Reverse	--	--	-1.0	$\mu A$	$V_{GS}=-20V$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	2	$\mu A$	$V_{DS}=50V$
		--	--	25		$V_{DS}=40V, T_J=55^\circ\text{C}$
$I_{DON}$	On-State Drain-Source Current(2)	8.0	--	--	A	$V_{GS}=10V, V_{DS}=5V$
$R_{DS(on)}$	Static Drain-Source			0.3	$\Omega$	$V_{GS}=10V, I_D=1.5A$
	On-State Resistance(2)			0.5		$V_{GS}=5.0V, I_D=0.6A$
$g_{fs}$	Forward Transconductance	--	2.5	--	S	$V_{DS} \geq 15V, I_D=2.0A$
$t_{d(on)}$	Turn-On Delay Time	--	--	40	ns	$V_{DD}=30V, I_D=0.6A,$ $Z_\theta=6.0\Omega,$
$t_r$	Rise Time	--	--	70		
$t_{d(off)}$	Turn-Off Delay Time	--	--	100		
$t_f$	Fall Time	--	--	70		
$Q_g$	Total Gate Charge	--	--	15	nC	$V_{DS}=25V, V_{GS}=10V,$ $I_D=1.3A$
$Q_{gs}$	Gate-Source Charge	--	1.0	--		
$Q_{gd}$	Gate-Drain ("Miller") Charge	--	2.0	--		

### Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	$^\circ\text{C/W}$

#### Notes ;

- $T_J=25^\circ\text{C}$  to  $150^\circ\text{C}$
- Pulse Test : Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$

### Source-Drain Diode Ratings and Characteristics


Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
$I_S$	Continuous Source Current (Body Diode)	--	--	1.8	A	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier 
$V_{SD}$	Diode Forward Voltage(2)	--	--	1.2	V	$T_J=25^\circ\text{C}, I_S=1.25A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	--	--	100	ns	$T_J=25^\circ\text{C}, I_F=2.5A, di_F/dt=100A/\mu\text{s}$

Fig 1. Output Characteristics

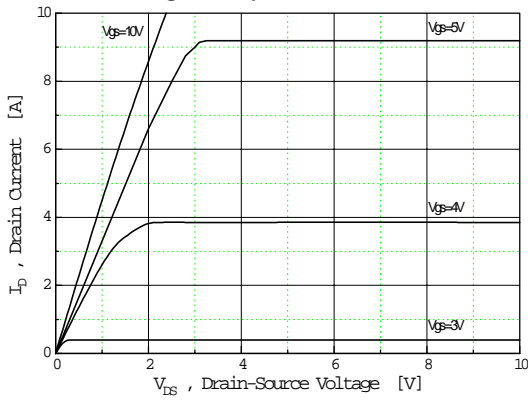


Fig 2. Transfer Characteristics

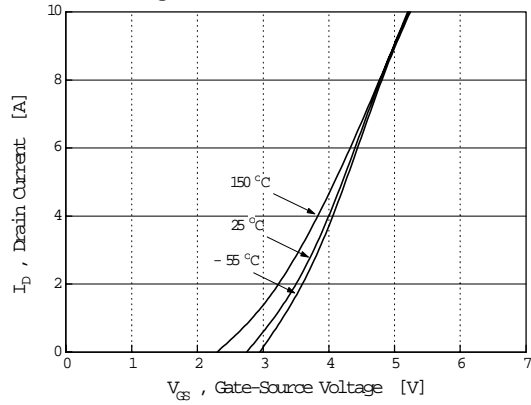


Fig 3. On-Resistance vs. Drain Current

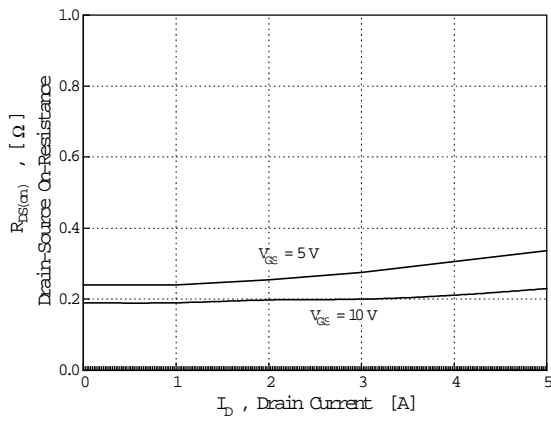


Fig 4. Capacitance vs. Drain-Source Voltage

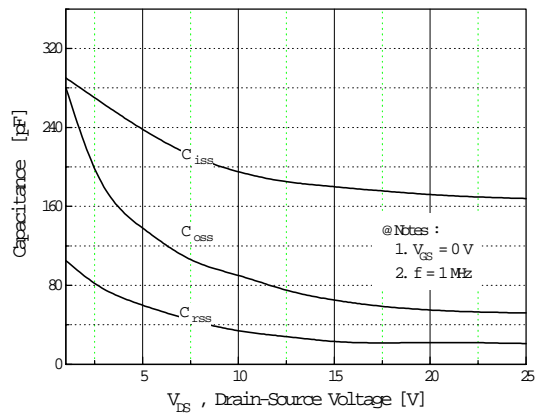


Fig 5. Breakdown Voltage vs. Temperature

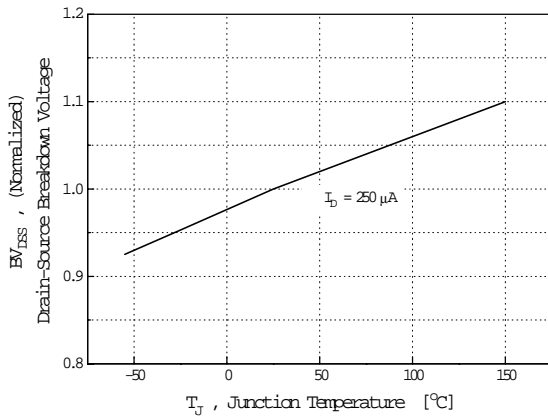
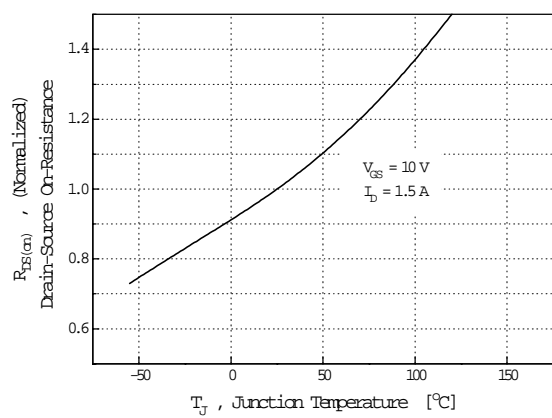
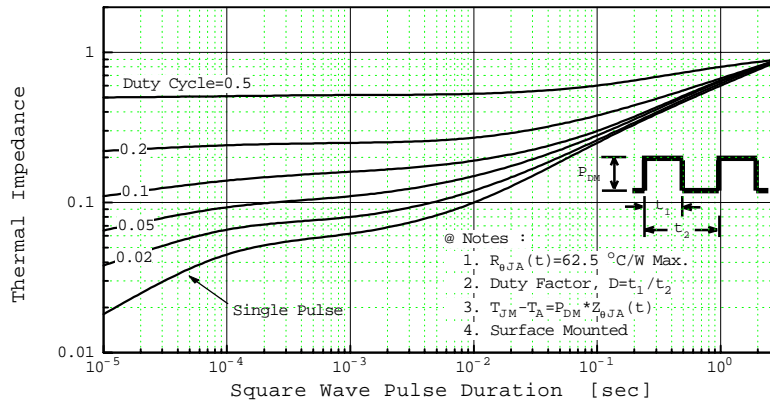


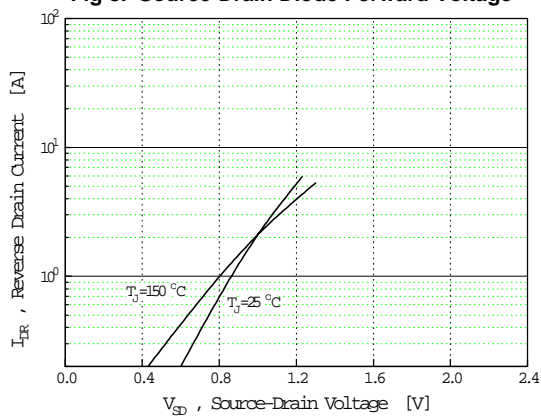
Fig 6. Normalized On-Resistance vs. Temperature



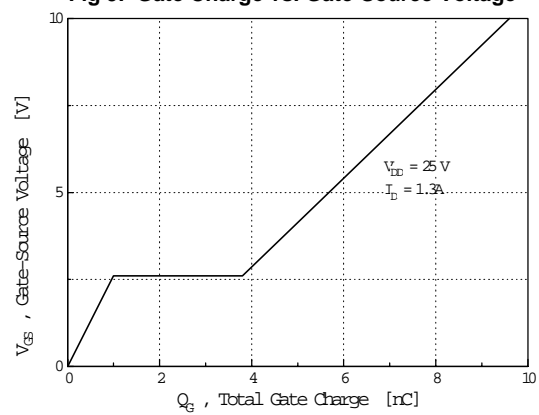
**Fig 7. Normalized Effective Transient Thermal Impedance, Junction-to-Ambient**



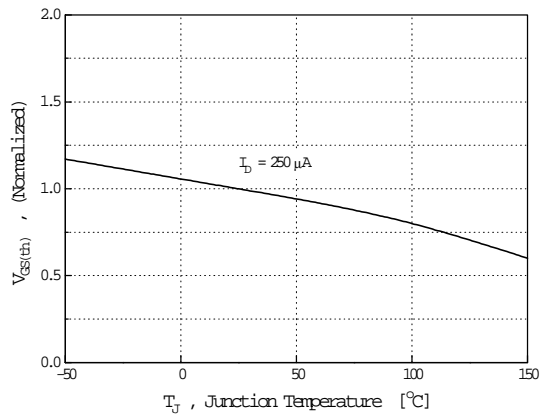
**Fig 8. Source-Drain Diode Forward Voltage**



**Fig 9. Gate Charge vs. Gate-Source Voltage**



**Fig 10. Threshold Voltage**



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E <sup>2</sup> CMOS <sup>™</sup>	ISOPLANAR <sup>™</sup>	QFET <sup>™</sup>	SuperSOT <sup>™</sup> -8	
EnSigna <sup>™</sup>	LittleFET <sup>™</sup>	QS <sup>™</sup>	SyncFET <sup>™</sup>	
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