600V High and Low Side Driver

PRODUCT SUMMARY

- **V_{OFFSET}** 600 V max.
- **I_O+/-** 1 A / 1.6 A
- **V_{OUT}** 10 V - 20 V
- **$t_{on/off}$ (typ.)** 140 ns/140 ns
- **Delay Matching (typ.)** 10 ns

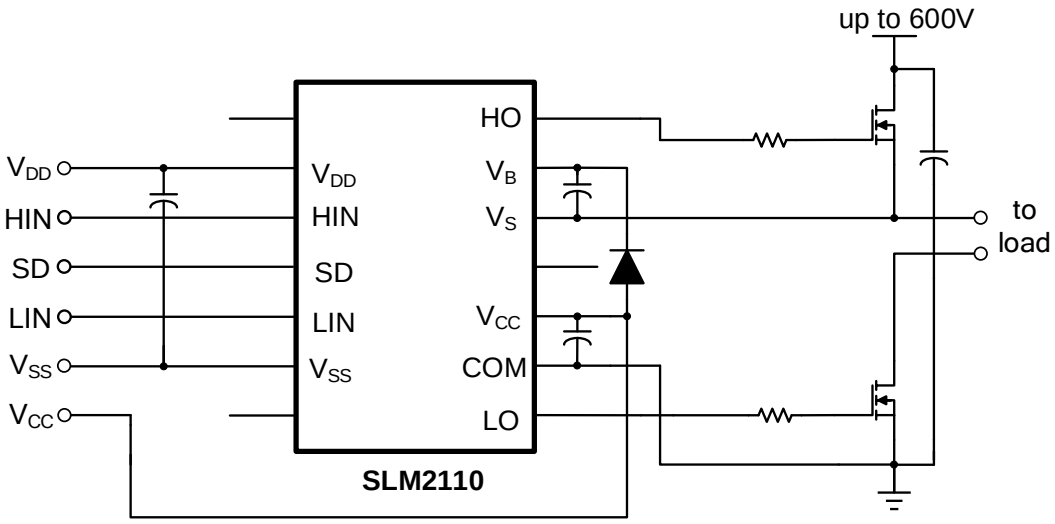
GENERAL DESCRIPTION

The SLM2110 is a high voltage, high speed power MOSFET and IGBT drivers with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

FEATURES

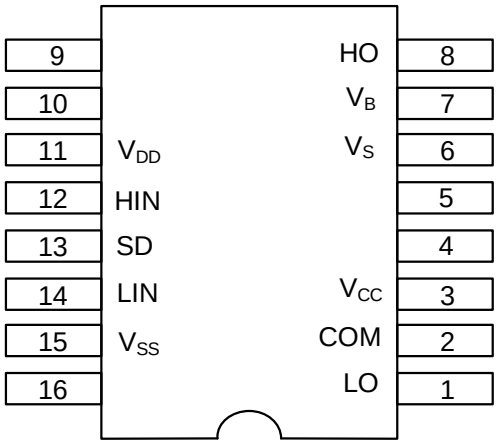
- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- Logic and power ground +/- 5V offset
- Cross-conduction prevention logic
- Schmitt-triggered inputs with pull-down
- Cycle-by-cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant
- SOP16W package

TYPICAL APPLICATION CIRCUIT



Refer to Pin Configuration for correct configuration. This diagram shows electrical connections only.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP16W	

PIN DESCRIPTION

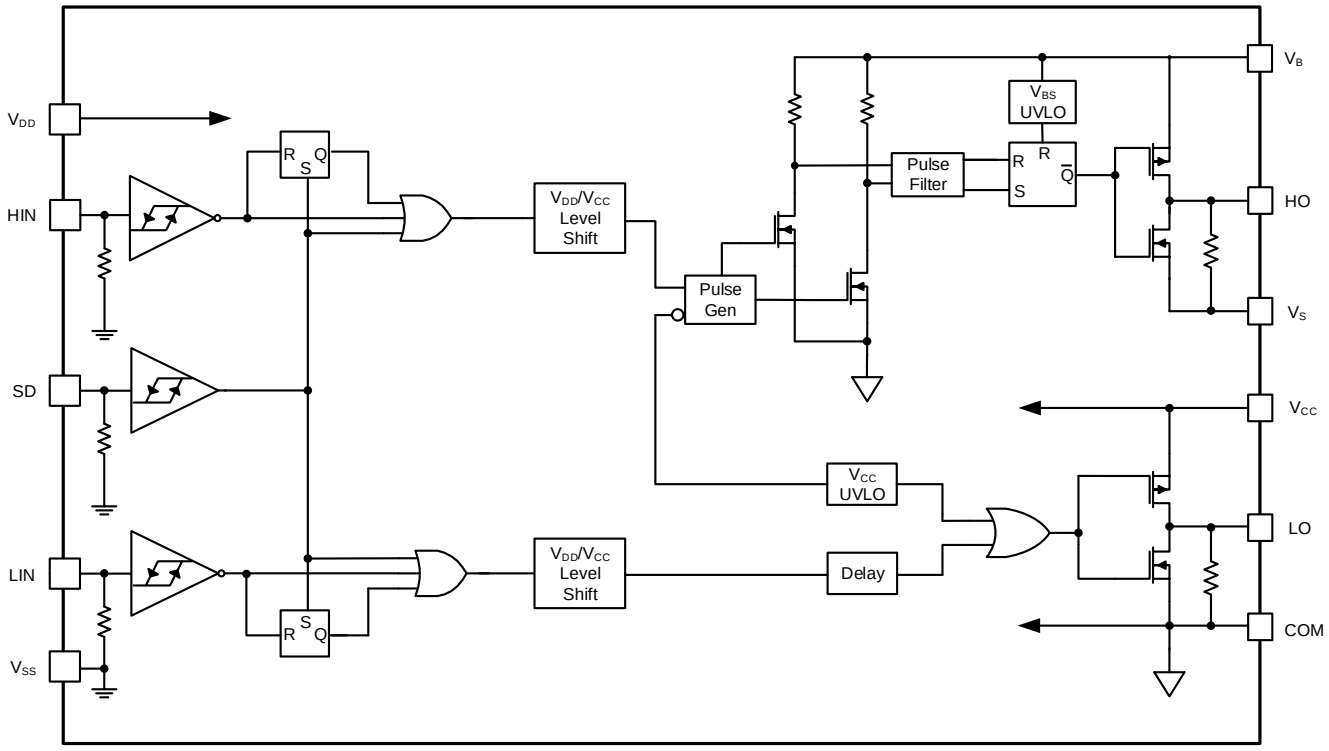
No.	Pin	Description
1	LO	Low-side gate drive output
2	COM	Low-side return
3	V_{CC}	Low-side supply
4	NC	No connection
5	NC	No connection
6	V_S	High-side floating supply return
7	V_B	High-side floating supply
8	HO	High-side gate drive output
9	NC	No connection
10	NC	No connection
11	V_{DD}	Logic supply
12	HIN	Logic input for high-side gate driver output (HO), in phase
13	SD	Logic input for shutdown
14	LIN	Logic input for low-side gate driver output (LO), in phase
15	V_{SS}	Logic ground
16	NC	No connection

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SLM2110CG	SOP16W, Pb-Free	1500/Reel

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	-0.3	625	V
V_S	High-side floating supply offset voltage	V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side supply voltage	-0.3	25	
V_{DD}	Logic supply voltage	-0.3	V_{SS} + 20	
V_{SS}	Logic supply offset voltage	V_{CC} - 20	V_{CC} + 0.3	
V_{LO}	Low-side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN, & SD)	V_{SS} - 0.3	V_{DD} + 0.3	
dV_S/dt	Allowable offset supply voltage transient	---	50	V/ns
P_D	Package power dissipation @ $T_A \leqslant +25°C$	---	1.25	W
θ_{JA}	Thermal resistance, junction to ambient	---	100	°C/W
T_J	Junction temperature	---	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	---	300	

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	V_S + 10	V_S + 20	V
V_S	High-side floating supply offset voltage		600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side supply voltage	10	20	
V_{DD}	Logic supply voltage	V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic supply offset voltage	-5	5	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN, LIN, & SD)	V_{SS}	V_{DD}	
T_A	Ambient temperature	- 40	125	°C

Note: The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The VS offset rating is tested with all supplies biased at a 15 V differential.

Note: Logic operational for V_S of (COM – 5 V) to (COM + 600V). Logic state held for V_S of (COM-5V) to (COM - V_{BS}).

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	V_S = 0 V	---	140	200	ns
t_{off}	Turn-off propagation delay	V_S = 0 V	---	140	200	
t_{sd}	Shutdown propagation delay	V_S = 0 V	---	130	160	
t_r	Turn-on rise time		---	15	25	
t_f	Turn-off fall time		---	9	15	
MT	Delay matching, HS & LS turn-on/off		---	---	10	

STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN, and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic “1” input voltage		V_{DD}× 80%	---	---	V
V_{IL}	Logic “0” input voltage		---	---	V_{DD}× 25%	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2 mA	---	---	0.2	
V_{OL}	Low level output voltage, V_O		---	0.02	0.15	
I_{LK}	Offset supply leakage current	V_B = V_S = 600 V	---	---	50	µA
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0 V	---	65	120	
I_{QCC}	Quiescent V_{CC} supply current		---	300	550	
I_{QDD}	Quiescent V_{DD} supply current		---	0.1	1	
I_{IN+}	Logic “1” input bias current	V_{IN} = 5V	---	8	15	
I_{IN-}	Logic “0” input bias current	V_{IN} = 0V	---	---	5	
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold		7.5	8.9	9.7	V
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold		7.4	8.2	9.4	
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold		7.5	8.9	9.7	V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold		7.4	8.2	9.4	
I_{O+}	Output high short circuit pulsed current[1]	V_O = 0 V, V_{IN} = Logic “1”, PW ≤ 10 µs	0.8	1		A

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{O-}	Output low short circuit pulsed current[1]	V_O = 15 V, V_{IN} = Logic "0", PW ⩽ 10 μs	1.2	1.6		

1） Values are verified by characterization on bench.

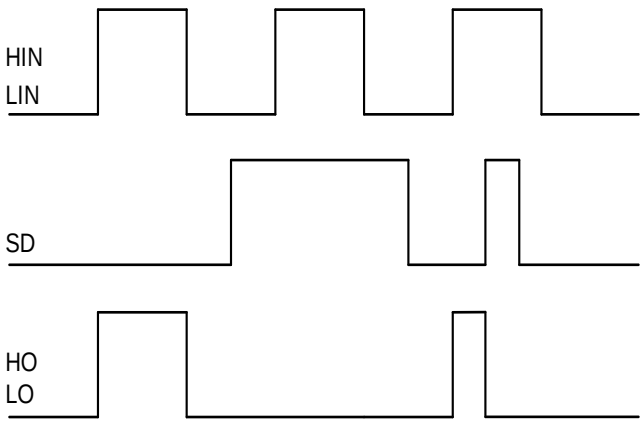


Figure 1. Input/Output Timing Diagram

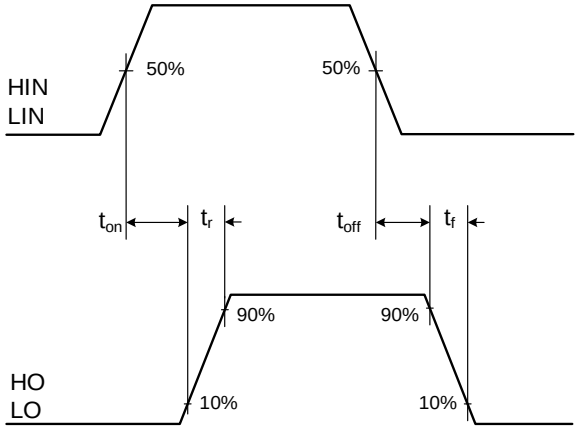


Figure 2. Switching Time Waveform Definition

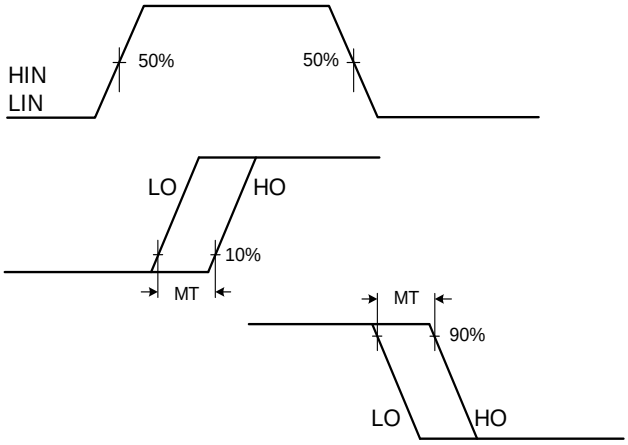


Figure 3. Delay Matching Waveform Definition

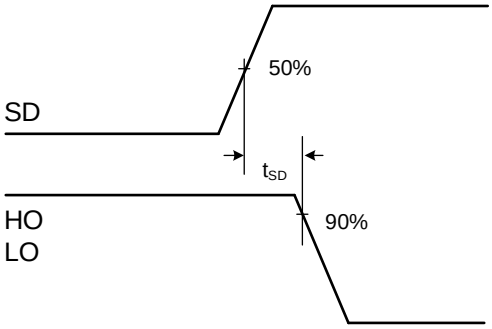


Figure 4. Shutdown Waveform Definition

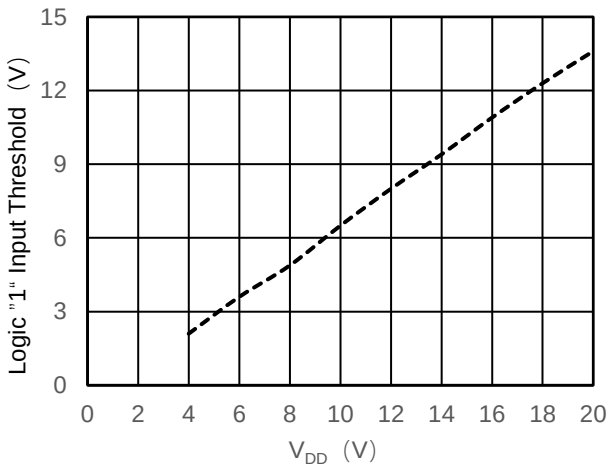


Figure 5. Logic "1" Input Threshold vs. VDD

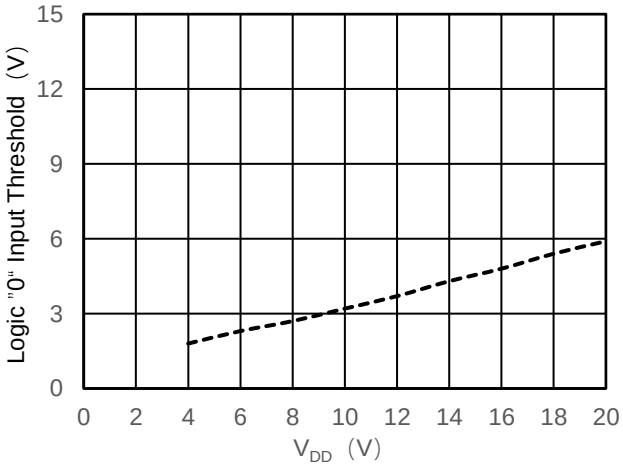
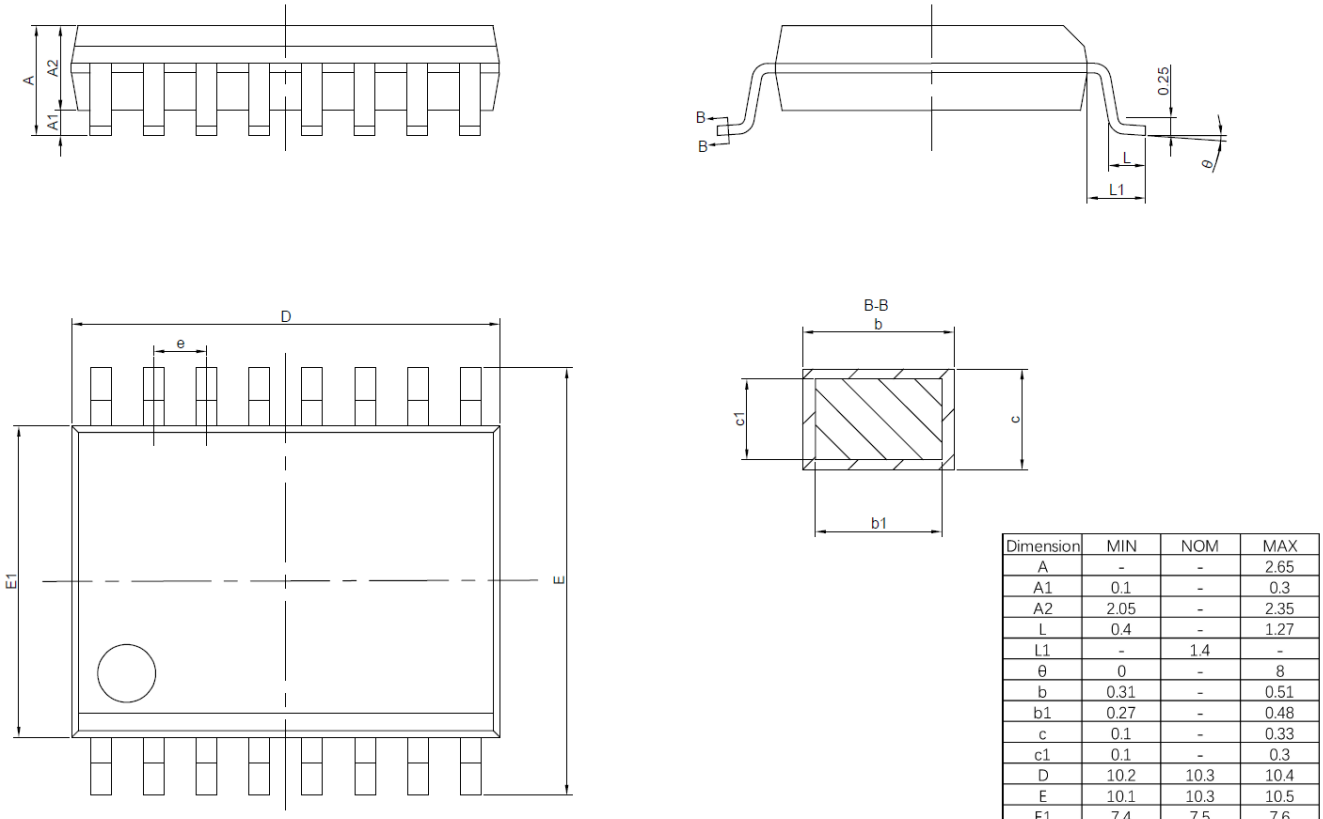


Figure 6. Logic "0" Input Threshold vs. VDD

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	2.65
A1	0.1	-	0.3
A2	2.05	-	2.35
L	0.4	-	1.27
L1	-	1.4	-
θ	0	-	8
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.1	-	0.33
c1	0.1	-	0.3
D	10.2	10.3	10.4
E	10.1	10.3	10.5
E1	7.4	7.5	7.6
e	1.02	1.27	1.52
Unit : mm			

Figure 7. SOP16W Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet, 2019-8-27	
Whole document	New company logo released
Page 1	Remove “May 2019”
Rev 1.4 datasheet, 2020-3-17	
Page 5	Change V_{IL} min from 10.5V to 12.5V
Rev 1.5 datasheet, 2020-7-29	
Page 3	Modify typo in function block
Rev 1.6 datasheet, 2021-11-16	
Whole datasheet	Update the Logo and format
Page 5	Updated the t_{on}, t_{off}, t_r and t_f value in the Dynamic Electrical Characteristics. Update the V_{OH}, I_{QDD}, I_{IN+} , I_{O+} and I_{O-} value in the Static Electrical Characteristics.
Rev 1.7 datasheet, 2023-09-10	
Page 5	Update VIL/VIH value.
Page 1, 2, 7	Update Package Case Outlines, Change SOIC-16(WB) to SOP16W
Page 6	Add Logic input voltage threshold vs. V_{DD} curve.