US1881

CMOS Multi-Purpose Latch

Features and Benefits

- Chopper stabilized amplifier stage
- Optimized for brushless DC motor applications
- Miniature high reliability package
- Operation down to 3.5V
- CMOS for optimum stability, quality and cost
- Low power consumption

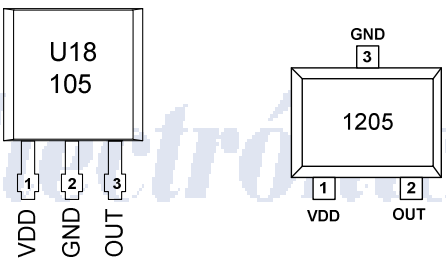
Ordering Information

Part No.	Temperature Suffix	Package Code
US1881	E (-40°C to 85°C)	SO (SOT-23) or UA(TO-92)
US1881	K (-40°C to 125°C)	SO (SOT-23) or UA(TO-92)
US1881	L (-40°C to 150°C)	SO (SOT-23) or UA(TO-92)

Applications

- Solid state switch
- Brushless DC motor commutation
- Speed Sensing
- Linear position sensing
- Angular position sensing
- Current sensing

Pinout:



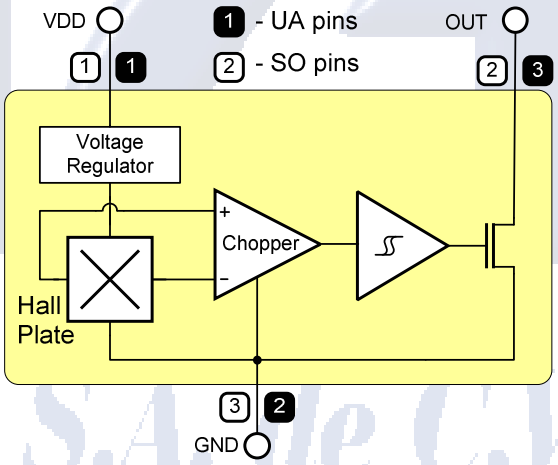
UA Package:

Pin1: VDD - supply
Pin2: GND - Ground
Pin3: OUT - Output

SO Package:

Pin1: VDD - supply
Pin2: OUT – Output
Pin3: GND - Ground

1 Functional Diagram



Note: Static electricity sensitive device; please observe ESD precautions. Reverse voltage protection is not included. For reverse polarity protection, a 100Ohm resistor in series with V_{DD} is recommended.

2 Description

The US1881 is the industry's first Hall integrated circuit in SOT-23 package. The US1881 is a bipolar Hall effect sensor IC based on mixed signal CMOS technology. It incorporates advanced chopper stabilization techniques to provide accurate and stable magnetic switch points. There are many applications for this HED in addition to those listed above. The design, specifications and performance have been optimized for commutation applications in 5V and 12V brushless DC motors.

In UA packaged device the output transistor will be latched on (Bop) in presence of a sufficiently strong South pole magnetic field facing the marked side of the package. Similarly, the output will be latched off (Brp) in the presence of a North field. The SOT-23 device behaviour is reverse to the UA device. The SOT-23 output transistor will be latched on (B_{OP}) in the presence of a sufficiently strong North pole magnetic field on the marked side.

Table of Contents

3 Glossary of Terms

MilliTesla (mT), Gauss: Units of magnetic flux density; 1 milliTesla = 10 Gauss.
CMOS – *Complementary Metal-Oxide Silicon* - A technology for building logic circuits that employs both "N" and "P" channel MOS transistors. It allows one to make ICs with lots of transistors that consume small amounts of power.

4 Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Supply Voltage (Operating)	V_{DD}	24	V
Supply Current (Fault)	I_{DD}	50	mA
Output Voltage	V_{OUT}	24	V
Output Current (Fault)	I_{OUT}	50	mA
Power Dissipation, UA/SO packages	P_D	700/389	mW
Maximum Junction Temperature	T_J	165	℃
Storage Temperature	T_S	-50 to 150	°C

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Operating Temperature Range	Value	Units
Temperature Suffix "E"	-40 to 85	℃
Temperature Suffix "K"	-40 to 125	℃
Temperature Suffix "L"	-40 to 150	℃

5 US1881 Electrical Characteristics

DC operating parameters: T_A = 25°C, V_{DD} = 12V (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Voltage	VDD	Operating	3.5		24	V
Supply current	I_{DD}	B < B_{OP}	1.1	2.0	5.0	mA
Saturation Voltage	$V_{DS(on)}$	I_{OUT} = 20mA, B > B_{op}, V_{DD}=4.5÷18V		0.4	0.5	V
Output Leakage	I_{OFF}	B < B_{RP}, V_{OUT}=24V		0.01	10	uA
Output Rise Time	t_r	V_{DD} = 12V, R_L = 1k, C_L = 20pF		0.04		us
Output Fall Time	t_f	V_{DD} = 12V, R_L = 1k, C_L = 20pF		0.18		us
Maximum Switching Frequency	fsw	Operating		10		KHz

6 Magnetic Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Point	B_{OP}	E/LUA, E/LSO,Ta=25°C,Vdd=3.5 … 24V DC	1.0	5.0	9.0	mT
Release Point	B_{RP}	E/LUA, E/LSO,Ta=25°C,Vdd=3.5 … 24V DC	-9.0	-5.0	-1.0	mT
Hysteresis	B_{HYS}	E/LUA, E/LSO,Ta=25°C,Vdd=3.5 … 24V DC	7.0	10.0	12.0	mT
Operating Point	B_{OP}	EUA, ESO, Ta=85°C,Vdd=3.5 … 24V DC	0.5	5.0	9.5	mT
Release Point	B_{RP}	EUA, ESO, Ta=85°C,Vdd=3.5 … 24V DC	-9.5	-5.0	-0.5	mT
Hysteresis	B_{HYS}	EUA, ESO, Ta=85°C,Vdd=3.5 … 24V DC	7.0	10.0	12.0	mT
Operating Point	B_{OP}	KUA, KSO, Ta=125°C,Vdd=3.5 … 24V DC	0.5	5.0	9.5	mT
Release Point	B_{RP}	KUA, KSO, Ta=125°C,Vdd=3.5 … 24V DC	-9.5	-5.0	-0.5	mT
Hysteresis	B_{HYS}	KUA, KSO, Ta=125°C,Vdd=3.5 … 24V DC	7.0	10.0	12.0	mT
Operating Point	B_{OP}	LUA, LSO, Ta=150°C,Vdd=3.5 … 24V DC	0.5	5.0	9.5	mT
Release Point	B_{RP}	LUA, LSO, Ta=150°C,Vdd=3.5 … 24V DC	-9.5	-5.0	-0.5	mT
Hysteresis	B_{HYS}	LUA, LSO, Ta=150°C,Vdd=3.5 … 24V DC	6.0	10.0	12.5	mT

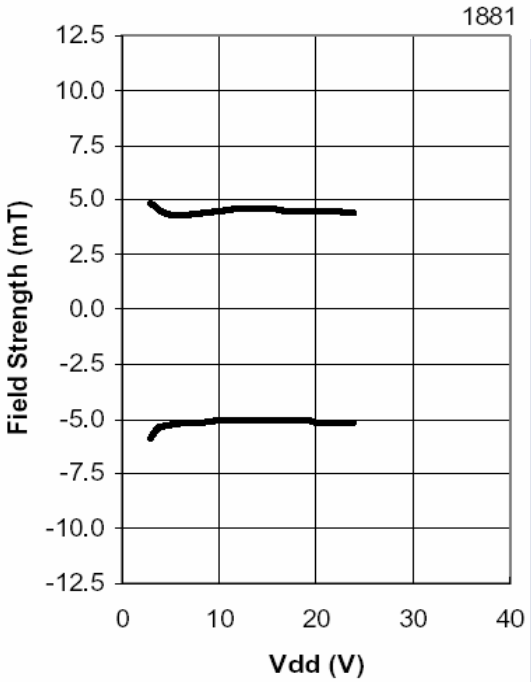
Note: 1 mT = 10 Gauss

7 Unique Features

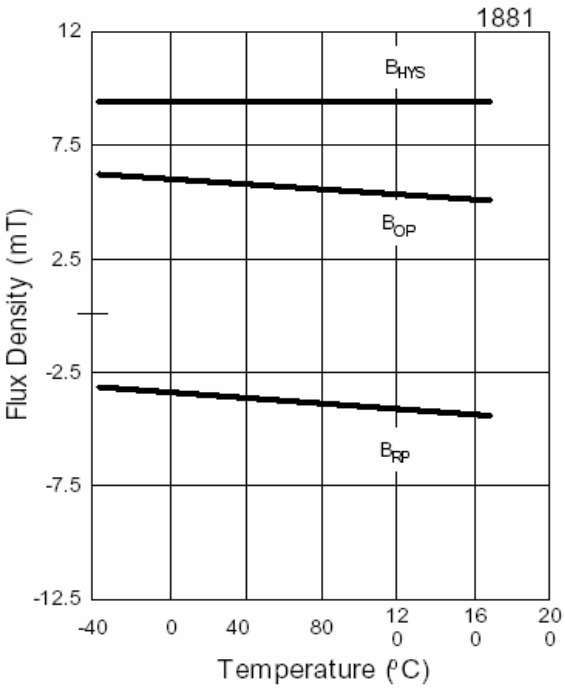
CMOS Hall IC Technology
The chopper stabilized amplifier uses switched capacitor techniques to eliminate the amplifier offset voltage, which, in bipolar devices, is a major source of temperature sensitive drift. CMOS makes this advanced technique possible. The CMOS chip is also much smaller than a bipolar chip, allowing very sophisticated circuitry to be placed in less space. The small chip size also contributes to lower physical stress and less power consumption.

8 Performance Graphs – unless otherwise specified Ta=25°C, VDD=12V

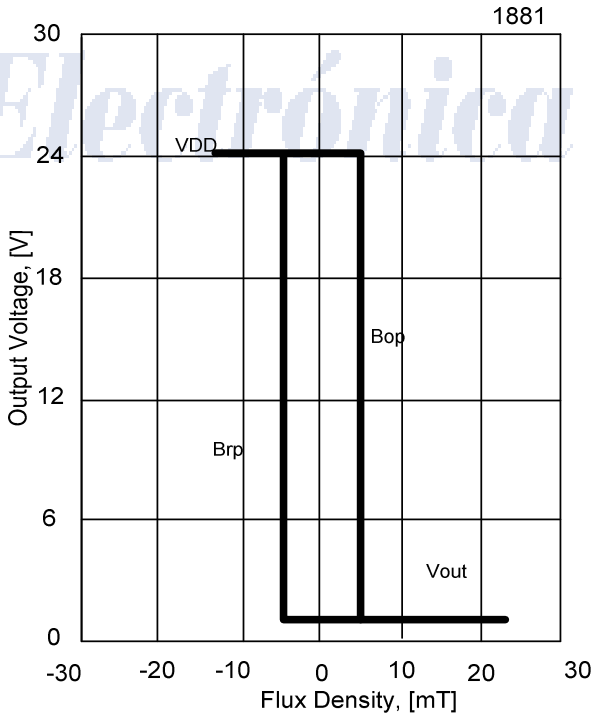
8.1 Typical Magnetic Switch Points vs V_{DD}



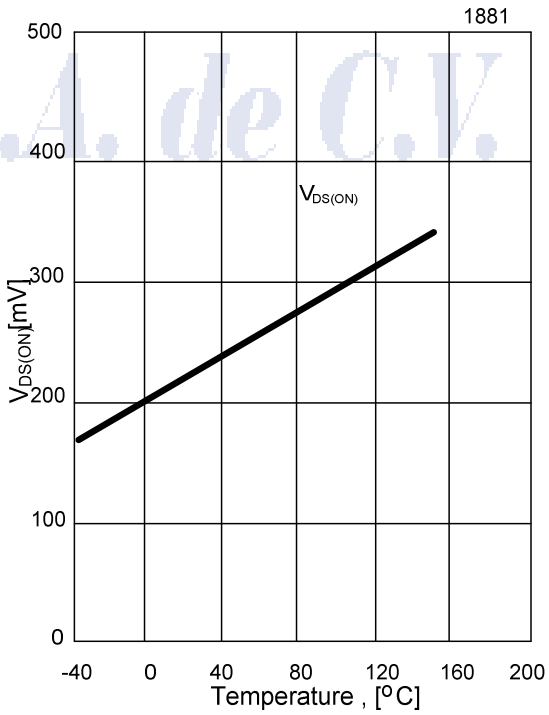
8.2 Magnetic Switch Points vs Temperature



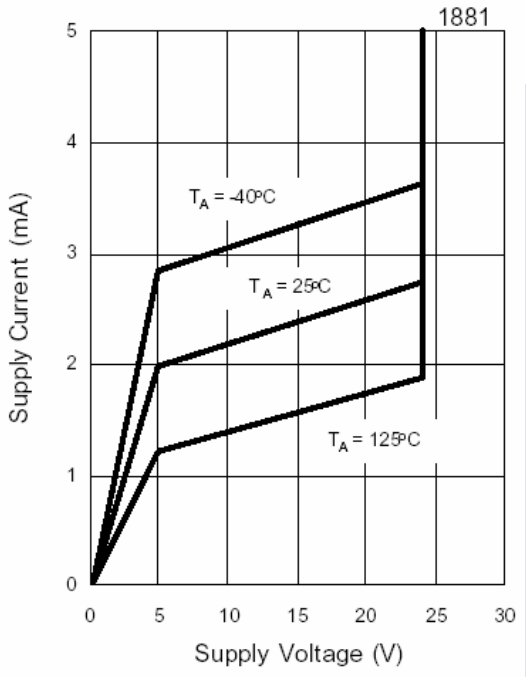
8.3 Output Voltage vs Magnetic Flux Density (Hysteresis)



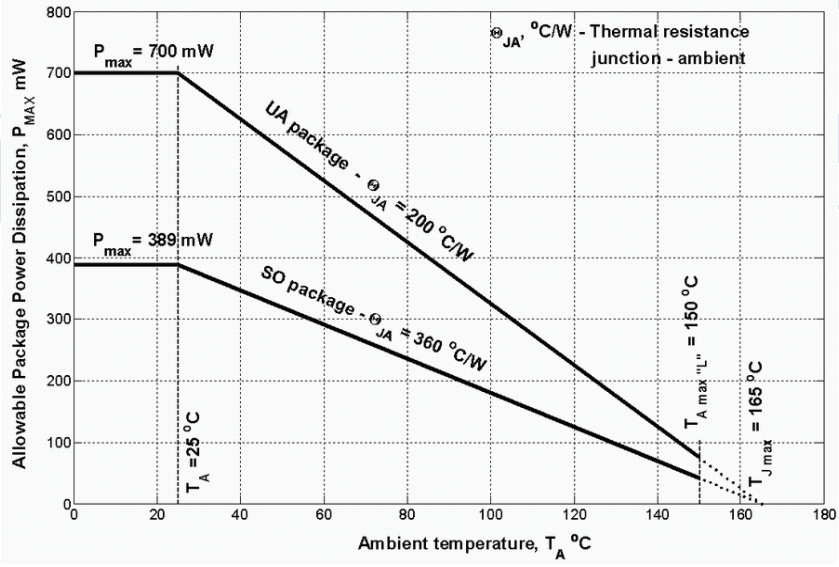
8.4 Typical Saturation Voltage vs Temperature(V_{DD}=12V;Iout=20mA)



8.5 Typical Supply Current vs V_{DD}



8.6 Maximal Power Dissipation (MPD) Versus Temperature

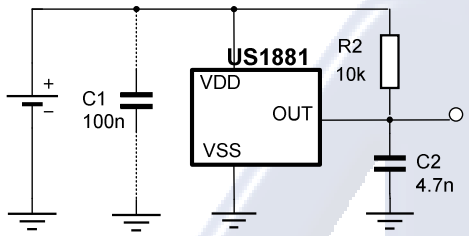


The thermal resistance Θ_{JA} and rated power dissipation are defined in accordance with EIA/JESD51-3 Standard.

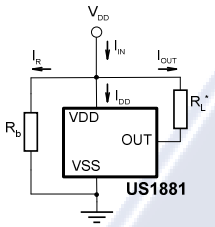
Some differences may be observed between values in the specification tables and the performance graphs.
The performance graphs are based on initial characterization of several ICs from one lot. Hence a particular IC may vary from the performance graphs but all ICs should meet the values stated in the specification tables.

9 Application Information

9.1 Typical Three-Wire Application Circuit



9.2 Two-Wire Circuit



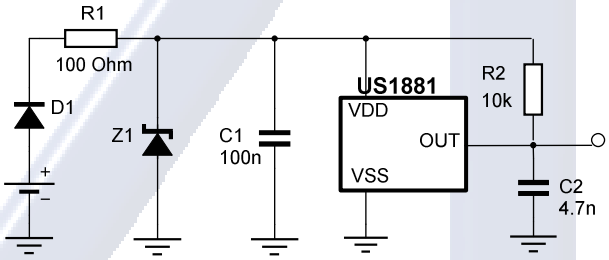
Note:

With this circuit, precise ON and OFF currents can be detected using only two connecting wires.

The resistors RL and Rb can be used to bias the input current. Refer to the part specifications for limiting values.

B_{RP} : $I_{OFF} = I_R + I_{DD} = V_{DD}/R_b + I_{DD}$
B_{OP} : $I_{ON} = I_{OFF} + I_{OUT} = I_{OFF} + V_{DD}/R_L$

9.3 Automotive and Harsh, Noisy Environments Three-Wire Circuit



10 Application Comments

If a weak power supply is used or the chip is intended to be used in noisy environment, it is recommended that figure 9.3 from the Application Information section is used. R1 and C1 form a RC filter, which bypasses the disturbances over the supply pin.
If a continuous reverse polarity protection is required for supply voltages above 5 Volts, it is recommended to use a diode instead of resistor, because the power dissipation demands become higher.

11 Pin Definitions and Descriptions

UA Pins	SO Pins	Pin Name	Type	Description
1	1	VDD	Supply	Power Supply pin
3	2	OUT	Output	Hall output pin (clamped)
2	3	VSS	Ground	Ground pin

12 Reliability Information

This Melexis device is classified and qualified regarding soldering technology, solderability and moisture sensitivity level, as defined in this specification, according to following test methods:

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)
- CECC00802
  Standard Method For The Specification of Surface Mounting Components (SMDs) of Assessed Quality
- EIA/JEDEC JESD22-B106
  Resistance to soldering temperature for through-hole mounted devices
- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices
- MIL 883 Method 2003 / EIA/JEDEC JESD22-B102
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Based on Melexis commitment to environmental responsibility, European legislation (Directive on the Restriction of the Use of Certain Hazardous substances, RoHS) and customer requests, Melexis has installed a Roadmap to qualify their package families for lead free processes also.
Various lead free generic qualifications are running, current results on request.

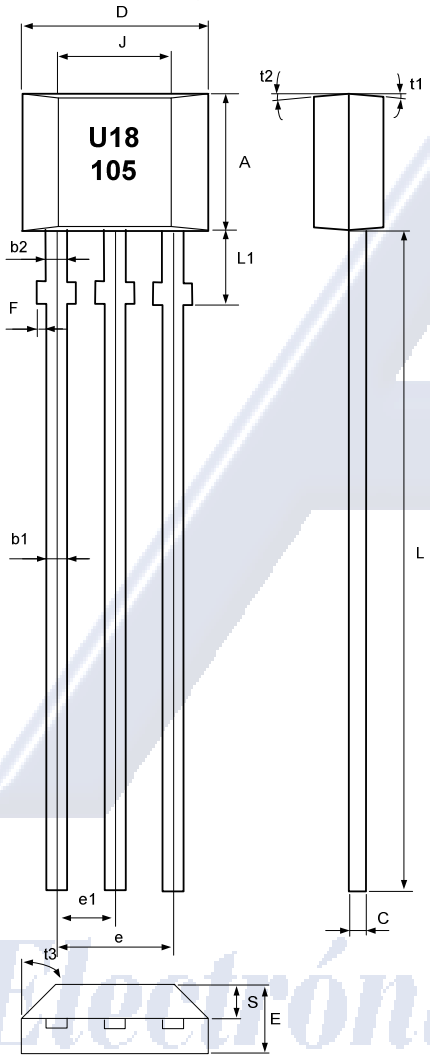
For more information on Melexis lead free statement see quality page at our website:
http://www.melexis.com/html/pdf/MLXleadfree-statement.pdf

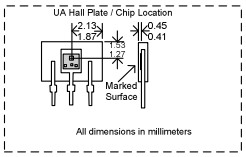
13 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

14 Physical Characteristics

14.1 UA Package Information





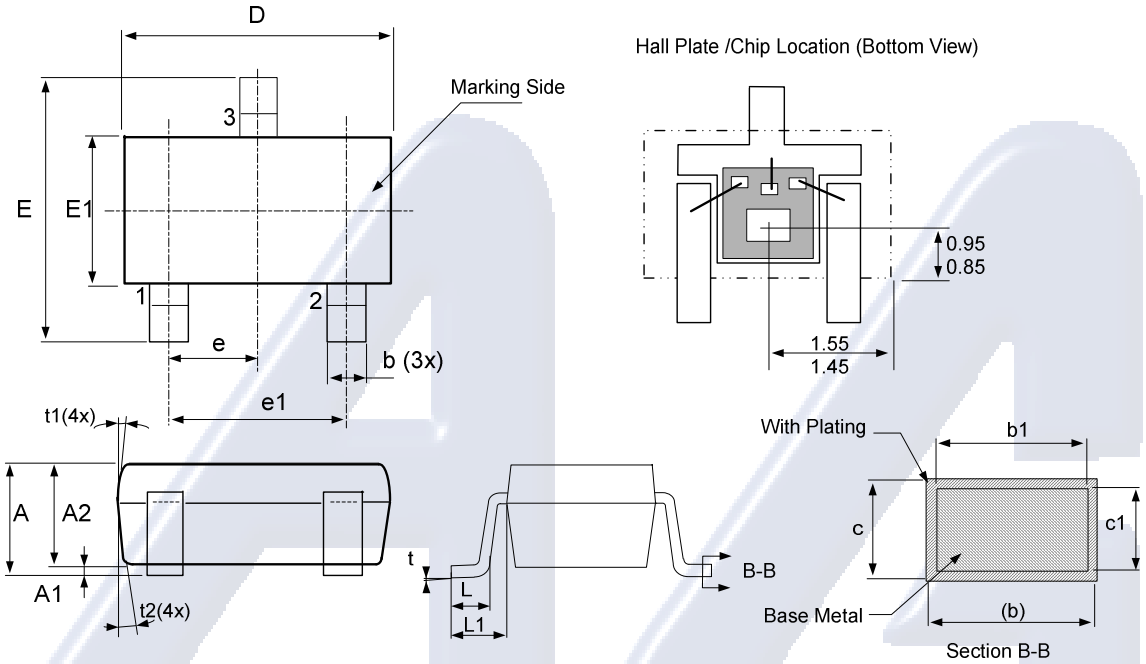
MARKING
Line 1:
1st letter (U) =Supplier (Melexis)
2nd and 3rd digits(18) =Series (1881)

Line2:
1st digit (1) =Year (2001)
2nd and 3rd digits =Week of the year

Symbols	Dimensions in millimeters		
	min	nom	max
A	2.80	3.00	3.20
b1	0.35	0.38	0.41
b2	0.43	0.46	0.48
C	0.35	0.38	0.41
D	3.90	4.10	4.30
e	2.51	2.54	2.57
e1	1.24	1.27	1.30
E	1.40	1.50	1.60
J	2.51	2.62	2.72
L	14.0	14.5	15.0
S	0.63	0.74	0.84
t3	-	45°	-
t2	-	5°	-
t1	-	-	5°
L1	1.55	1.65	1.75
F	0	-	0.20

Note:
1. Controlling Dimension: mm
2. Tolerance: +/-0.004" unless otherwise specified
3. Package dimensions exclude molding flash
4. The end flash shall not exceed 0.005" on each side

14.2 SOT23 Package Information



Note:
1. Controlling Dimension : mm
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash , protrusions or gate burrs shall not exceed 0.10mm per side.
3. Dimension E1 does not include interlead flash or protrusion shall not exceed 0.10mm per side.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive or mold flash, tie bar burrs, interlead flash and gate burrs, but including any mismatch between the top and bottom of the molded body.
5. The section B-B applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Marking (on top of the chip)
1YXX - First Digit (1) - part number; YXX- date code(Y - last digit of the Year, XX - week)

Symbols	Dimensions in millimeters		
	min	nom	max
A	1.05	-	1.35
A1	0.05	-	0.15
A2	1.00	1.10	1.20
b	0.25	-	0.50
b1	0.25	0.40	0.45
c	0.08	-	0.20
c1	0.08	0.11	0.15
D	2.70	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
L	0.35	0.45	0.55
L1	0.60 REF		
e	0.95 BSC		
e1	1.90 BSC		
t	0^o	5^o	10^o
t1	3^o	5^o	7^o
t2	6^o	8^o	10^o

15 Disclaimer

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