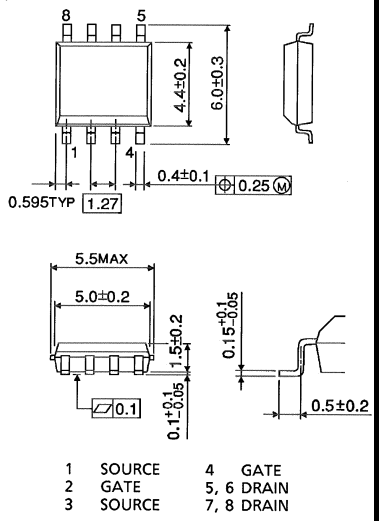
TOSHIBA Field Effect Transistor Silicon N, P Channel MOS Type (π−MOSVI/U−MOSII)

TPC8402

Lithium-Ion Secondary Battery Applications
Notebook PCs
Portable Equipment Applications

- Low drain−source ON resistance : P Channel $R_{DS\ (ON)}$ = 27 mΩ (typ.)
  N Channel $R_{DS\ (ON)}$ = 37 mΩ (typ.)
- High forward transfer admittance : P Channel $|Y_{fs}|$ = 7 S (typ.)
  N Channel $|Y_{fs}|$ = 6 S (typ.)
- Low leakage current : P Channel I_{DSS} = −10 μA (V_{DS} = −30 V)
  N Channel I_{DSS} = 10 μA (V_{DS} = 30 V)
- Enhancement−mode
  : P Channel V_{th} = −0.8~ −2.0 V (V_{DS} = −10 V, I_D = −1mA)
  N Channel V_{th} = 0.8~2.0 V (V_{DS} = 10 V, I_D = 1mA)

Unit: mm



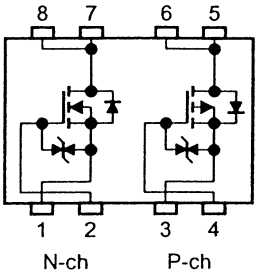
JEDEC	—
JEITA	—
TOSHIBA	2-6J1E

Weight: 0.080 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics			Symbol	Rating		Unit
				P Channel	N Channel	
Drain-source voltage			V_{DSS}	−30	30	V
Drain-gate voltage (R_{GS} = 20 kΩ)			V_{DGR}	−30	30	V
Gate-source voltage			V_{GSS}	±20	±20	V
Drain current	DC	(Note 1)	I_D	−4.5	5	A
	Pulse	(Note 1)	I_{DP}	−18	20	
Drain power dissipation (t = 10s) (Note 2a)	Single-device operation	(Note 3a)	$P_{D\ (1)}$	1.5	1.5	W
	Single-device value at dual operation	(Note 3b)	$P_{D\ (2)}$	1.0	1.0	
Drain power dissipation (t = 10s) (Note 2b)	Single-device operation	(Note 3a)	$P_{D\ (1)}$	0.75	0.75	
	Single-device value at dual operation	(Note 3b)	$P_{D\ (2)}$	0.45	0.45	
Single-pulse avalanche energy			E_{AS}	26.3 (Note 4a)	32.5 (Note 4b)	mJ
Avalanche current			I_{AR}	−4.5	5	A
Repetitive avalanche energy Single-device value at operation (Note 2a, Note 3b, Note 5)			E_{AR}	0.10		mJ
Channel temperature			T_{ch}	150		°C
Storage temperature range			T_{stg}	−55~150		°C

Circuit Configuration



Note: For Notes 1 to 5, see the next page.

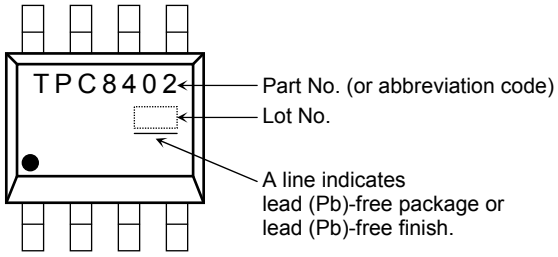
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

Thermal Characteristics

Characteristics		Symbol	Max.	Unit
Thermal resistance, channel to ambient (t = 10s) (Note 2a)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	83.3	°C/W
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	125	
Thermal resistance, channel to ambient (t = 10s) (Note 2b)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	167	
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	278	

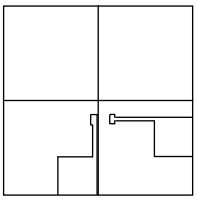
Marking



Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2:

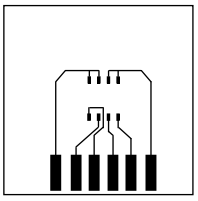
a) Device mounted on a glass-epoxy board (a)



FR-4
25.4 × 25.4 × 0.8
(unit: mm)

(a)

b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(unit: mm)

(b)

Note 3:

a) The power dissipation and thermal resistance values shown are for a single device. (During single-device operation, power is applied to one device only.)

b) The power dissipation and thermal resistance values shown are for a single device. (During dual operation, power is applied to both devices evenly.)

Note 4:

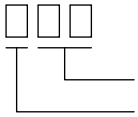
a) V_{DD} = −24 V, T_{ch} = 25°C (Initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = −4.5 A

b) V_{DD} = 24 V, T_{ch} = 25°C (Initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = 5.0 A

Note 5: Repetitive rating: pulse width limited by maximum channel temperature

Note 6: • on lower left of the marking indicates Pin 1.

* Weekly code: (Three digits)

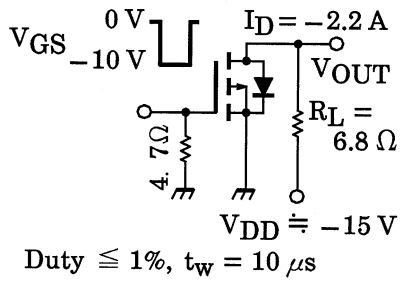


Week of manufacture
(from “01” for first week of the year, continuing up to “52” or “53”)

Year of manufacture
(the last digit of the calendar year)

P-ch

Electrical Characteristics (Ta = 25°C)

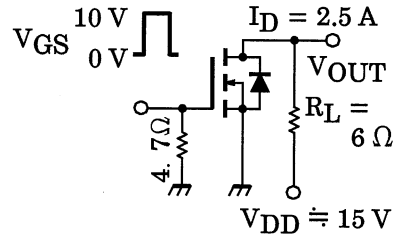
Characteristics		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut−off current		I_{DSS}	V_{DS} = −30 V, V_{GS} = 0 V	—	—	−10	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−30	—	—	V
		$V_{(BR)\ DSX}$	I_D = −10 mA, V_{GS} = 20 V	−15	—	—	
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −1 mA	−0.8	—	−2.0	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −4 V, I_D = −2.2 A	—	55	65	mΩ
		$R_{DS\ (ON)}$	V_{GS} = −10 V, I_D = −2.2 A	—	27	35	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −2.2 A	3.5	7	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	970	—	pF
Reverse transfer capacitance		C_{rss}		—	180	—	
Output capacitance		C_{oss}		—	370	—	
Switching time	Rise time	t_r		—	17	—	ns
	Turn−on time	t_{on}		—	20	—	
	Fall time	t_f		—	75	—	
	Turn−off time	t_{off}		—	160	—	
Total gate charge (gate−source plus gate−drain)		Q_g	V_{DD} ≈ −24 V, V_{GS} = −10 V, I_D = −4.5 A	—	28	—	nC
Gate−source charge 1		Q_{gs1}		—	6	—	
Gate−drain (“miller”) charge		Q_{gd}		—	12	—	

Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	−18	A
Forward voltage (diode)		V_{DSF}	I_{DR} = −4.5 A, V_{GS} = 0 V	—	—	1.2	V

N-ch

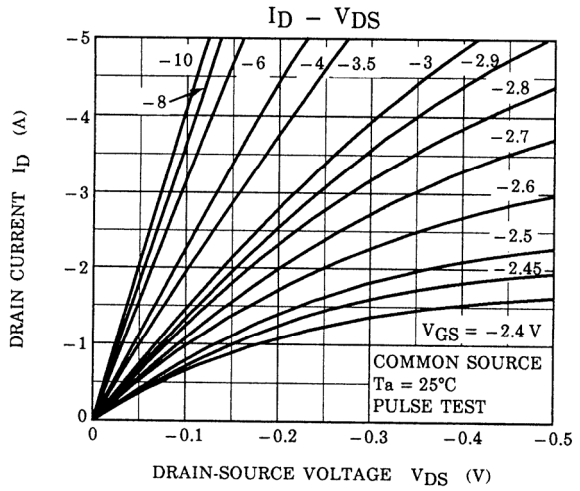
Electrical Characteristics (Ta = 25°C)

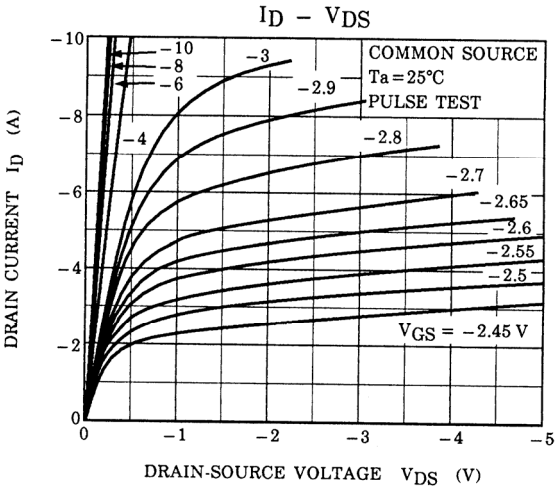
Characteristics		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut−off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	10	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	30	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	0.8	—	2.0	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4 V, I_D = 2.5 A	—	58	80	mΩ
		$R_{DS\ (ON)}$	V_{GS} = 10 V, I_D = 2.5 A	—	37	50	mΩ
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 2.5 A	3	6	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	475	—	pF
Reverse transfer capacitance		C_{rss}		—	85	—	
Output capacitance		C_{oss}		—	270	—	
Switching time	Rise time	t_r		—	10	—	ns
	Turn−on time	t_{on}		—	16	—	
	Fall time	t_f		—	13	—	
	Turn−off time	t_{off}		—	70	—	
Total gate charge (gate−source plus gate−drain)		Q_g	V_{DD} ≈ 24 V, V_{GS} = 10 V, I_D = 5 A	—	16	—	nC
Gate−source charge 1		Q_{gs1}		—	11	—	
Gate−drain (“miller”) charge		Q_{gd}		—	5	—	

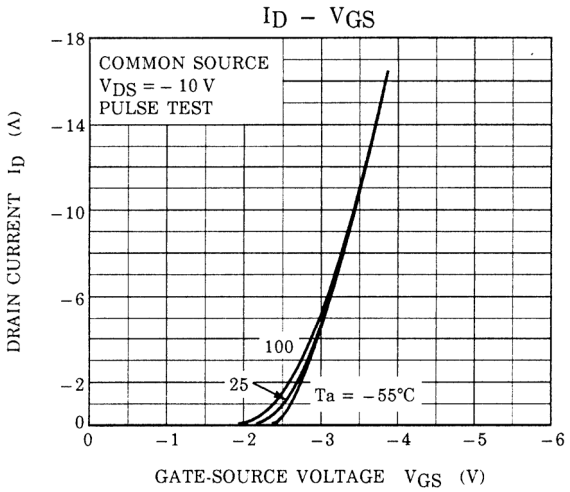
Source−Drain Ratings and Characteristics (Ta = 25°C)

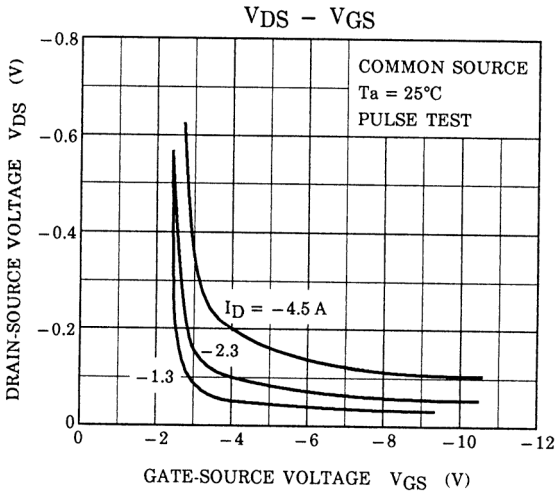
Characteristics		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	20	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 6 A, V_{GS} = 0 V	—	—	−1.2	V

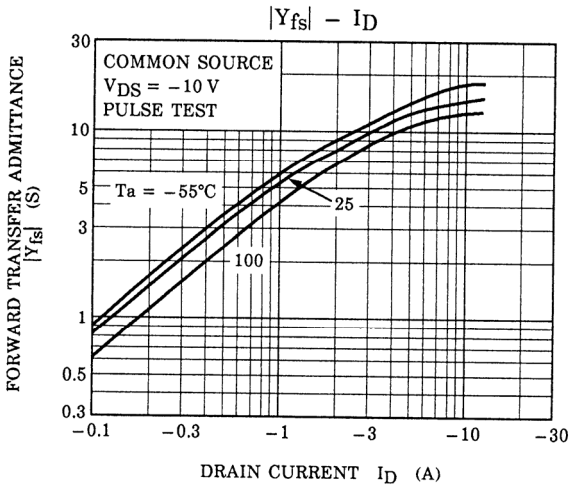
P-ch

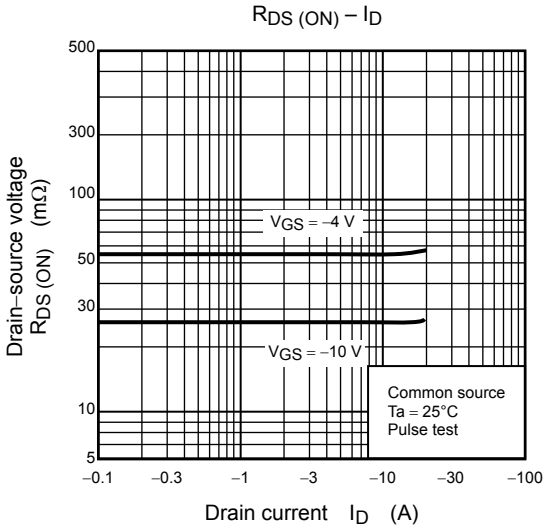

I_D – V_{DS}
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)
−10
−8
−6
−4
−3.5
−3
−2.9
−2.8
−2.7
−2.6
−2.5
−2.45
V_{GS} = −2.4 V
COMMON SOURCE
Ta = 25°C
PULSE TEST


I_D – V_{DS}
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)
COMMON SOURCE
Ta = 25°C
PULSE TEST
−10
−8
−6
−4
−3
−2.9
−2.8
−2.7
−2.65
−2.6
−2.55
−2.5
V_{GS} = −2.45 V


I_D – V_{GS}
DRAIN CURRENT I_D (A)
GATE-SOURCE VOLTAGE V_{GS} (V)
COMMON SOURCE
V_{DS} = − 10 V
PULSE TEST
100
25
Ta = −55°C

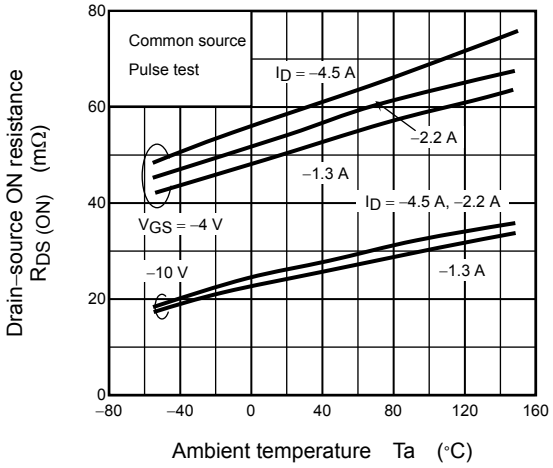

V_{DS} – V_{GS}
DRAIN-SOURCE VOLTAGE V_{DS} (V)
GATE-SOURCE VOLTAGE V_{GS} (V)
COMMON SOURCE
Ta = 25°C
PULSE TEST
I_D = −4.5 A
−2.3
−1.3


$|Y_{fs}|$ – I_D
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)
COMMON SOURCE
V_{DS} = −10 V
PULSE TEST
Ta = −55°C
25
100

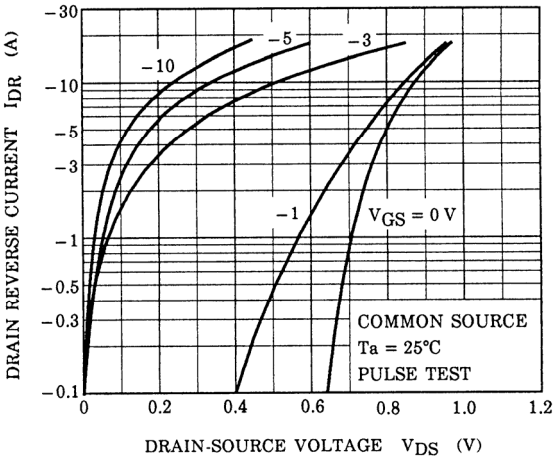

$R_{DS\ (ON)}$ – I_D
Drain–source voltage $R_{DS\ (ON)}$ (mΩ)
Drain current I_D (A)
V_{GS} = −4 V
V_{GS} = −10 V
Common source
Ta = 25°C
Pulse test

P-ch

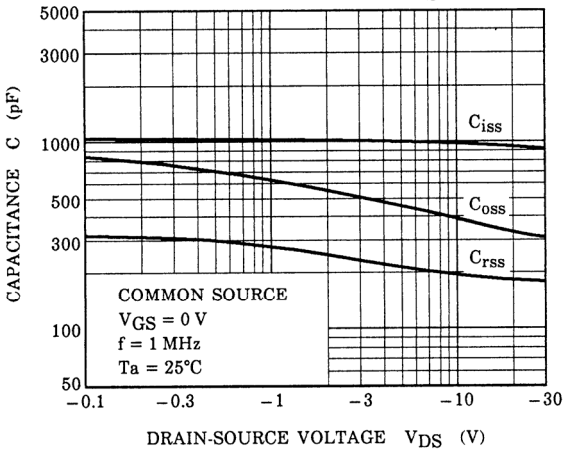
$R_{DS\ (ON)}$ – Ta



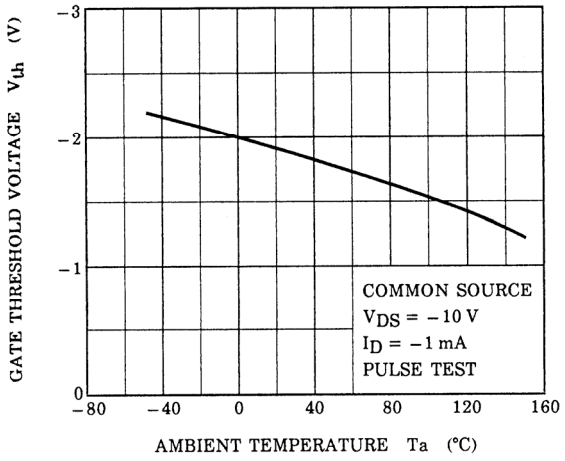
I_{DR} – V_{DS}



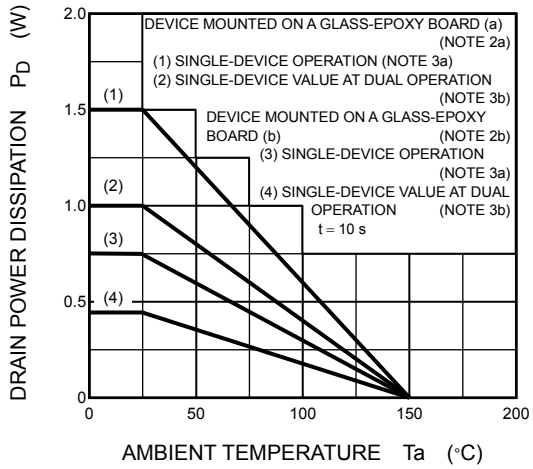
CAPACITANCE – V_{DS}



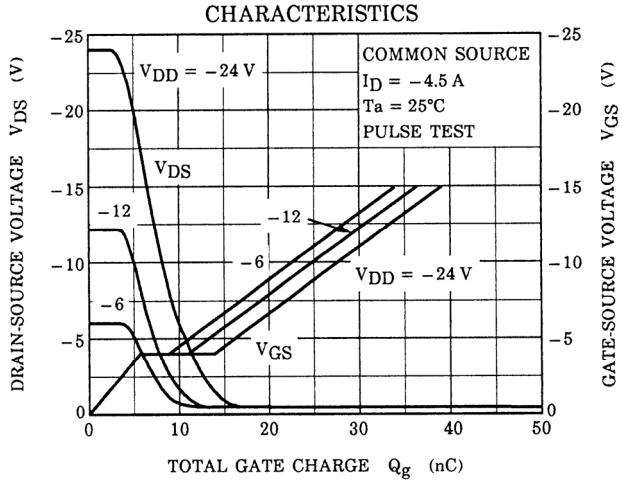
V_{th} – Ta



P_D – Ta

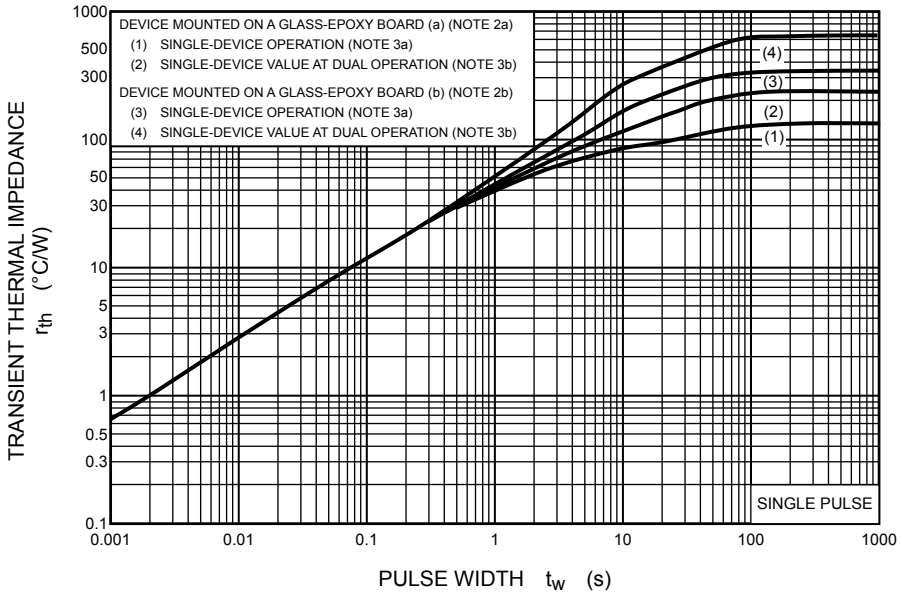


DYNAMIC INPUT / OUTPUT CHARACTERISTICS

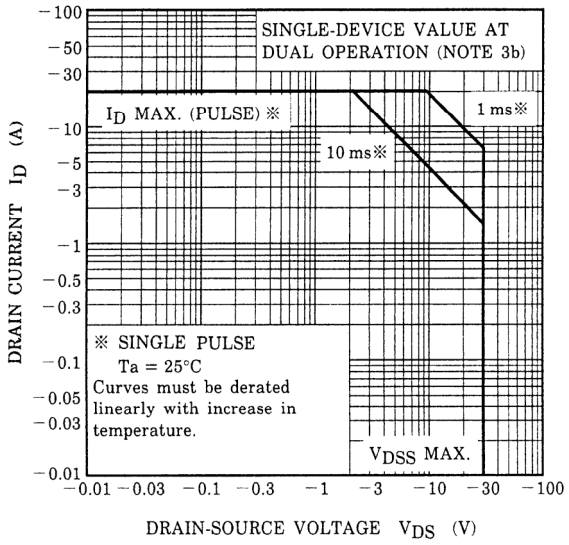


P-ch

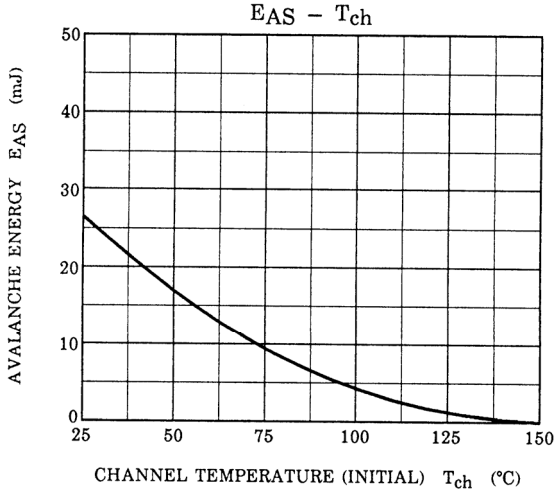
$r_{th} - t_w$

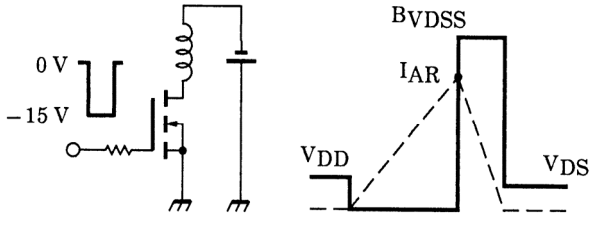


SAFE OPERATING AREA



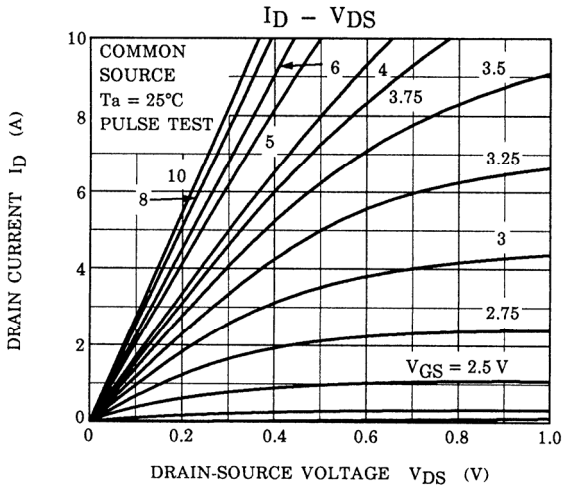
$E_{AS} - T_{ch}$

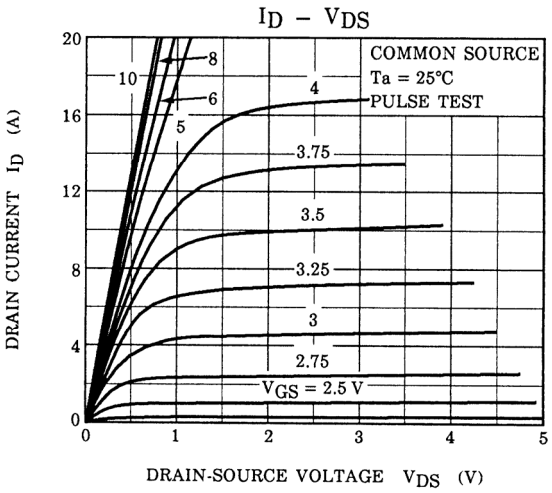


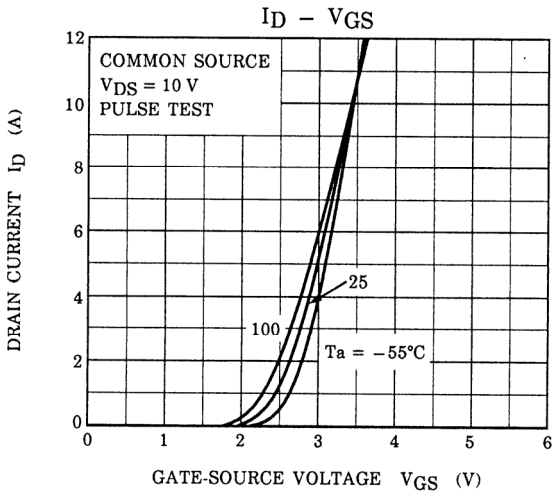


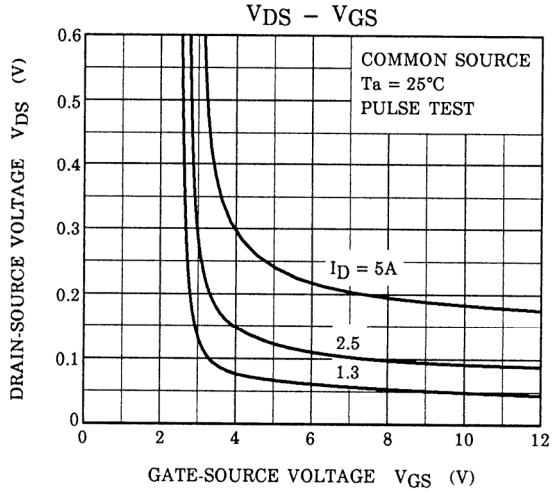
T_{ch} = 25°C (Initial)
Peak I_{AR} = −4.5 A, R_G = 25 Ω $E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$
V_{DD} = −24 V, L = 1.0 mH

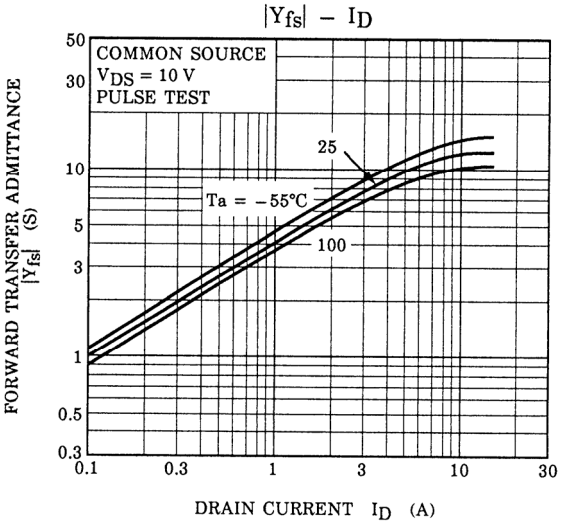
N-ch

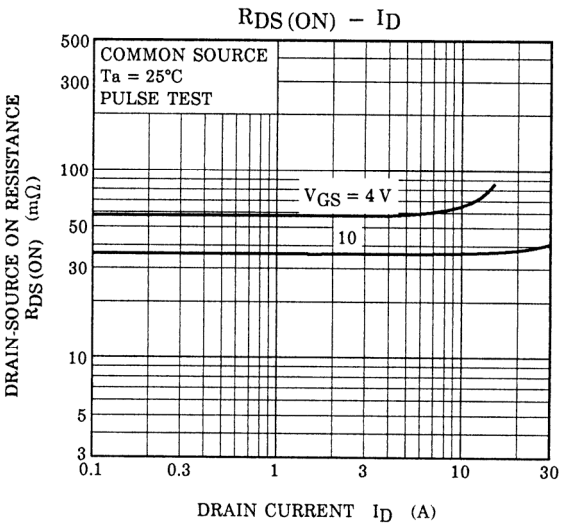

I_D – V_{DS}
COMMON SOURCE
Ta = 25°C
PULSE TEST
10
8
6
5
4
3.75
3.5
3.25
3
2.75
V_{GS} = 2.5 V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)


I_D – V_{DS}
COMMON SOURCE
Ta = 25°C
PULSE TEST
10
8
6
5
4
3.75
3.5
3.25
3
2.75
V_{GS} = 2.5 V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)


I_D – V_{GS}
COMMON SOURCE
V_{DS} = 10 V
PULSE TEST
25
100
Ta = −55°C
DRAIN CURRENT I_D (A)
GATE-SOURCE VOLTAGE V_{GS} (V)

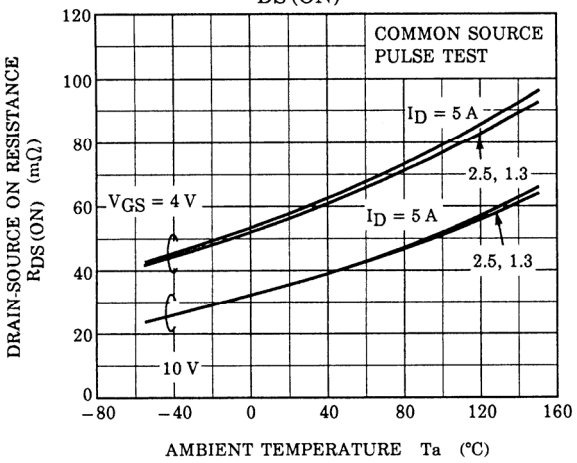

V_{DS} – V_{GS}
COMMON SOURCE
Ta = 25°C
PULSE TEST
I_D = 5A
2.5
1.3
DRAIN-SOURCE VOLTAGE V_{DS} (V)
GATE-SOURCE VOLTAGE V_{GS} (V)


$|Y_{fs}|$ – I_D
COMMON SOURCE
V_{DS} = 10 V
PULSE TEST
25
Ta = −55°C
100
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)

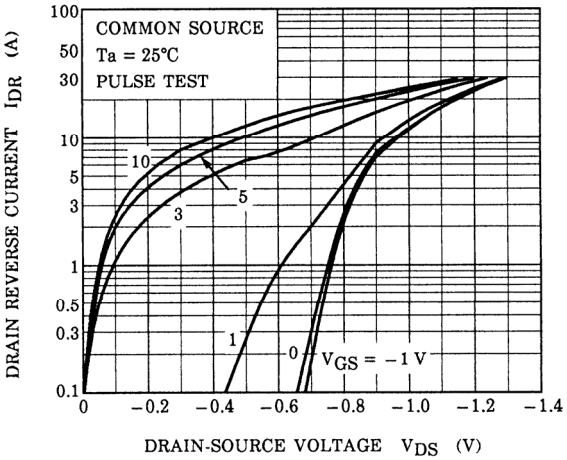

$R_{DS\,(ON)}$ – I_D
COMMON SOURCE
Ta = 25°C
PULSE TEST
V_{GS} = 4 V
10
DRAIN-SOURCE ON RESISTANCE $R_{DS\,(ON)}$ (mΩ)
DRAIN CURRENT I_D (A)

N-ch

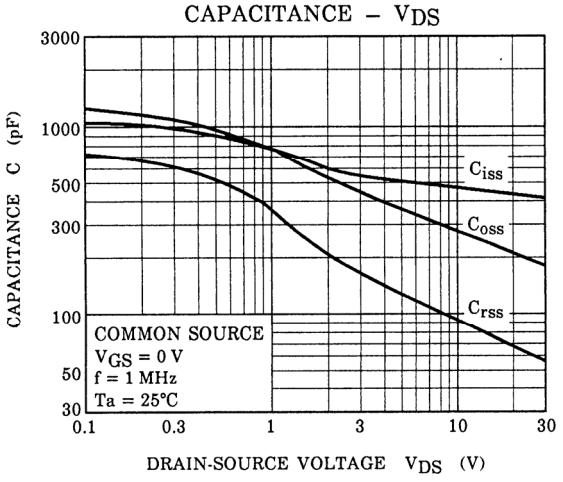
$R_{DS\,(ON)}$ – Ta



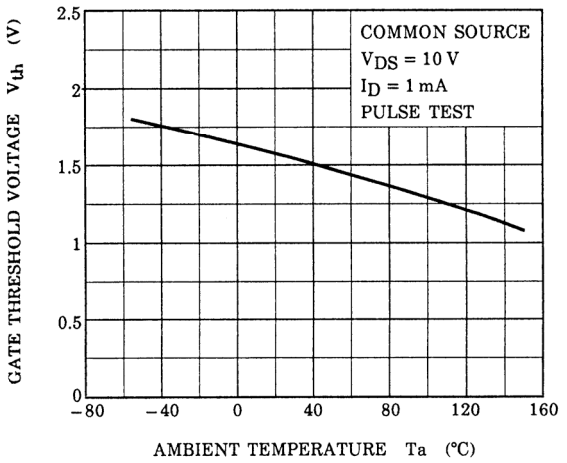
I_{DR} – V_{DS}



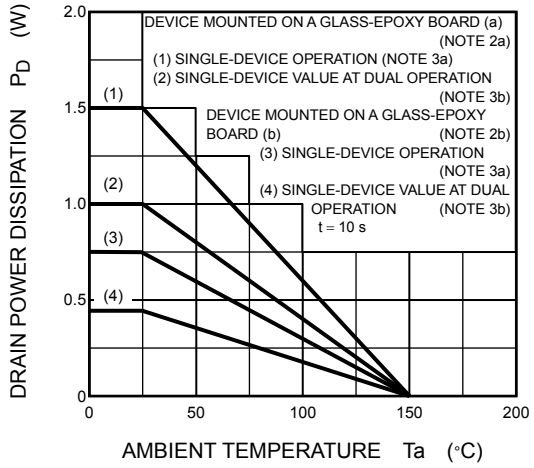
CAPACITANCE – V_{DS}



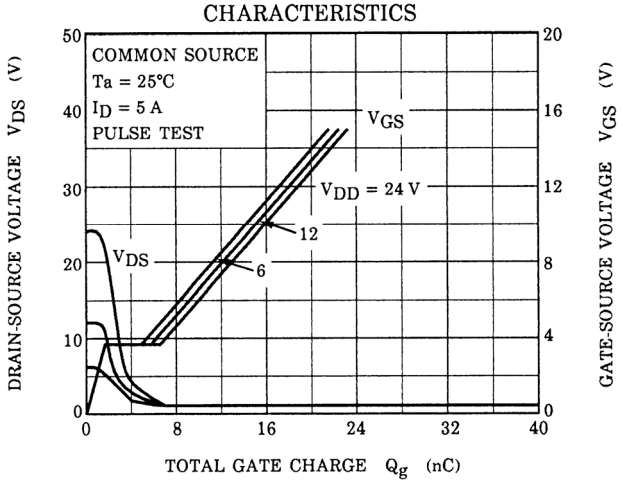
V_{th} – Ta



P_D – Ta

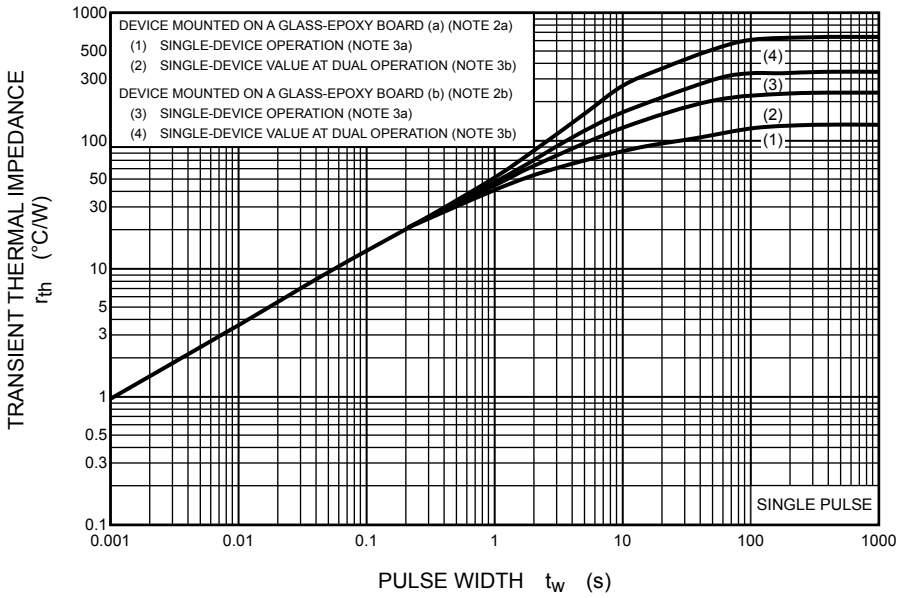


DYNAMIC INPUT / OUTPUT CHARACTERISTICS

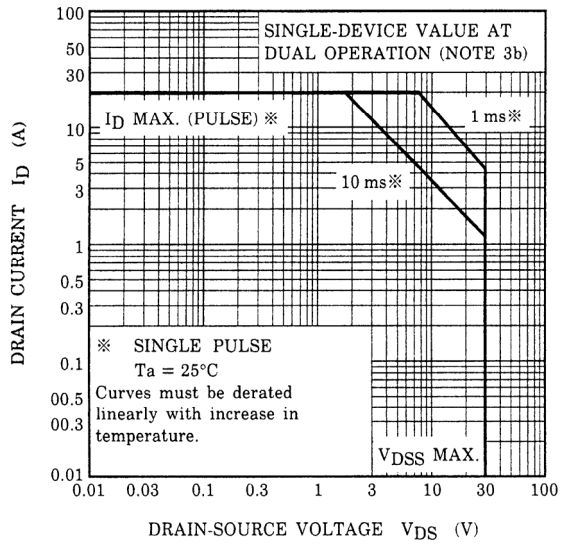


N-ch

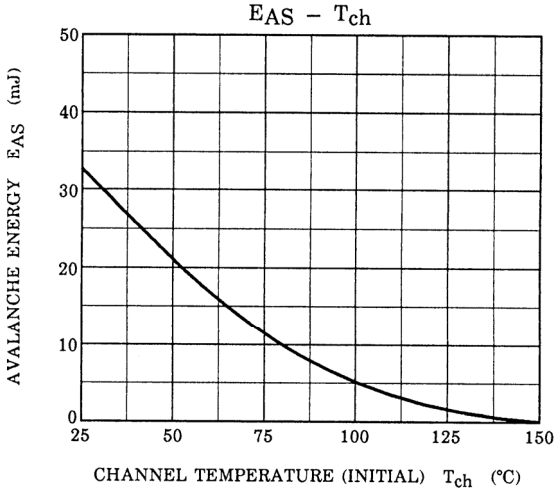
$r_{th} - t_w$

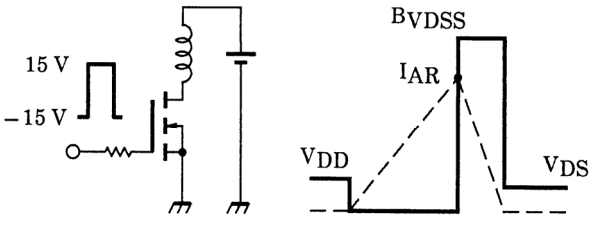


SAFE OPERATING AREA



$E_{AS} - T_{ch}$





T_{ch} = 25°C (Initial)
Peak I_{AR} = 5 A, R_G = 25 Ω
V_{DD} = 24 V, L = 1.0 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}}\right)$$

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