MP2374

6.5V-32V Input, 1A, 330kHz Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2374 is a high voltage step-down converter ideal for automotive power adapter battery chargers. Its wide 6.5V to 32V input voltage range covers the automotive battery's requirements and it achieves 1A continuous output for quick charge capability.

Current mode operation provides fast transient response and eases loop stabilization. Fault protection includes cycle-by-cycle current limiting and thermal shutdown. In shutdown mode, the converter draws only 20μA of supply current.

The MP2374 requires a minimum number of readily available external components to complete a 1A step-down DC to DC converter solution.

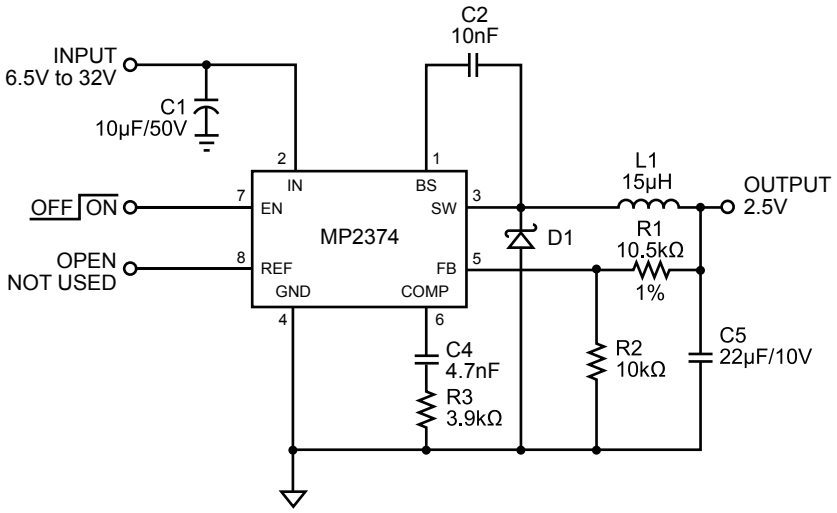
FEATURES

- Wide 6.5V to 32V Input Operating Range
- 34V Absolute Maximum Input
- 1A Continuous Load Current
- 120mΩ Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 20μA Shutdown Mode
- Fixed 330KHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Output Adjustable From 1.23V to 21V
- Under Voltage Lockout
- Reference Voltage Output
- Available in an 8-Pin SOIC Package

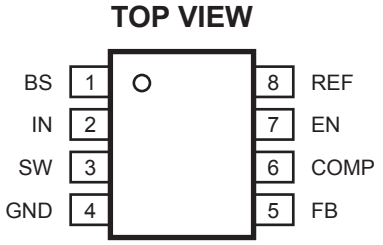
APPLICATIONS

- Automotive Power Adapters
- PDA and Cellular Phone Battery Chargers
- Automotive Aftermarket Electronics

TYPICAL APPLICATION



PACKAGE REFERENCE



Part Number*	Package
MP2374DS	SOIC8
Temperature	**Top Marking**
–40°C to +85°C	

* For Tape & Reel, add suffix –Z (eg. MP2374DS–Z)
For RoHS Compliant Packaging, add suffix –LF
(eg. MP2374DS–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

IN Supply Voltage ..... –0.3V to +34V
SW Voltage ..... –1V to V_{IN} + 0.3V
BS Voltage ..... V_{SW} – 0.3V to V_{SW} + 6V
All Other Pins ..... –0.3V to +6V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (2)

Input Voltage ..... 6.5V to 32V
Operating Temperature ..... –40°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
SOIC8	90	45	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown Supply Current		V_{EN} = 0V		20	35	µA
Supply Current		V_{EN} = 5V, V_{FB} = 1.4V		1.0	1.2	mA
Feedback Voltage		6.5V ≤ V_{IN} ≤ 32V, V_{COMP} < 2V	1.202	1.230	1.258	V
Error Amplifier Voltage Gain				400		V/V
Error Amplifier Transconductance		ΔI_C = ±10µA	500	700	1100	µA/V
High-Side Switch On Resistance (4)				120		mΩ
Low-Side Switch On Resistance (4)				8.5		Ω
High-Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V		0	10	µA
Current Limit (5)			2.3			A
Current Sense to COMP Transconductance				3.5		A/V
Oscillation Frequency			280	330	380	KHz
Short Circuit Oscillation Frequency		V_{FB} = 0V		35		KHz
Maximum Duty Cycle (4)		V_{FB} = 1.0V		90		%
Minimum Duty Cycle (4)		V_{FB} = 1.5V			0	%
EN Shutdown Threshold Voltage			0.8	1.2	1.6	V
Enable Pull-Up Current		V_{EN} = 0V		1.8		µA
EN UVLO Threshold		V_{EN} Rising	2.4	2.6	2.8	V
EN UVLO Threshold Hysteresis				250		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Shutdown (4)				160		°C
REF Voltage		I_{REF} = 0		5.0		V
REF Load Regulation (4)		ΔI_{REF} = 0 to 1mA		100		mV
REF Line Regulation (4)		I_{REF} = 100μA, V_{IN} = 6.5 to 32V		30		mV

Notes:

4) These parameters are guaranteed by design, not production tested.

PIN FUNCTIONS

Pin #	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 10nF or greater capacitor from SW to BS to power the high-side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 6.5V to 32V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Input Capacitor*.
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground.
5	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 1.230V. See *Setting the Output Voltage*.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required. See *Compensation.*
7	EN	Enable/UVLO. A voltage greater than 2.8V enables operation. For complete low current shutdown the EN pin voltage needs to be less than 800mV.
8	REF	Reference Output. REF is the 5V reference voltage output. It can supply up to 1mA to external circuitry. If used, bypass REF to GND with 10nF or greater capacitor. Leave REF unconnected if not used.

OPERATION

The MP2374 is a current mode step-down regulator. It regulates input voltages from 6.5V to 32V down to an output voltage as low as 1.230V and is able to supply up to 1A of load current.

The MP2374 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal error amplifier. The output current of the transconductance error amplifier is presented at COMP where a network compensates the regulation control system.

The voltage at COMP is compared to the switch current measured internally to control the output voltage. The converter uses an internal N-Channel MOSFET switch to step-down the input voltage to the regulated output voltage. Since the MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS drives the gate. The capacitor is internally charged while SW is low. An internal 10Ω switch from SW to GND is used to insure that SW is pulled to GND when the switch is off to fully charge the BS capacitor

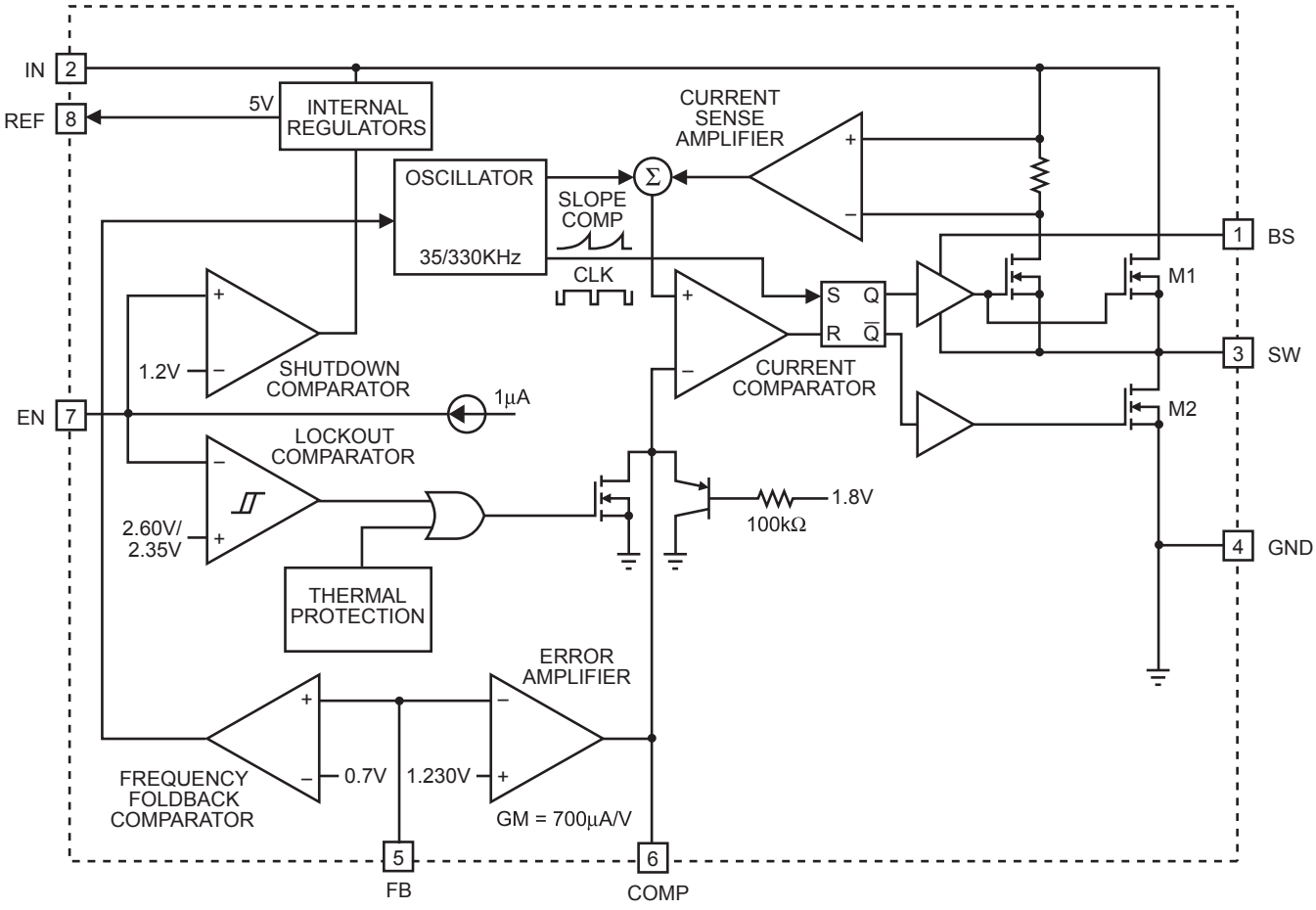


Figure 1—Functional Block Diagram

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB. The voltage divider divides the output voltage down by the ratio:

$$V_{FB} = V_{OUT} \times \frac{R2}{(R1+R2)}$$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Thus the output voltage is:

$$V_{OUT} = 1.230 \times \frac{(R1+R2)}{R2}$$

A typical value for R2 can be as high as 100kΩ, but 10kΩ is recommended. Using that value, R1 is determined by:

$$R1 \cong 8.18 \times (V_{OUT} - 1.230)$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 17kΩ.

Inductor (L1)

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor results in less ripple current that results in lower output ripple voltage. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current. Choose an inductor that does not saturate under the worst-case load conditions. A good rule to use for determining the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current that the IC can provide. Also, make sure that the peak inductor current (the load current plus half the peak-to-peak inductor ripple current) is below the 2.3A minimum current limit.

The inductance value can be calculated by the equation:

$$L1 = V_{OUT} \times \frac{(V_{IN} - V_{OUT})}{(V_{IN} \times f \times \Delta I)}$$

Where V_{IN} is the input voltage, f is the switching frequency and ΔI is the peak-to-peak inductor ripple current.

Table 1 lists a number of suitable inductors from various manufacturers.

Table 1—Inductor Selection Guide

Vendor/ Model	Core Type	Core Material	Package Dimensions (mm)		
			W	L	H
Sumida					
CR75	Open	Ferrite	7.0	7.8	5.5
CDH74	Open	Ferrite	7.3	8.0	5.2
CDRH5D28	Shielded	Ferrite	5.5	5.7	5.5
CDRH5D28	Shielded	Ferrite	5.5	5.7	5.5
CDRH6D28	Shielded	Ferrite	6.7	6.7	3.0
CDRH104R	Shielded	Ferrite	10.1	10.0	3.0
Toko					
D53LC Type A	Shielded	Ferrite	5.0	5.0	3.0
D75C	Shielded	Ferrite	7.6	7.6	5.1
D104C	Shielded	Ferrite	10.0	10.0	4.3
D10FL	Open	Ferrite	9.7	1.5	4.0
Coilcraft					
DO3308	Open	Ferrite	9.4	13.0	3.0
DO3316	Open	Ferrite	9.4	13.0	5.1

Input Capacitor (C1)

The input current to the step-down converter is discontinuous, and so a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. A low ESR capacitor is required to keep the noise at the IC to a minimum. Ceramic capacitors are preferred, but tantalum or low ESR electrolytic capacitors may also suffice.

The input capacitor value should be greater than 10µF. The capacitor can be electrolytic, tantalum or ceramic. However, since it absorbs the input switching current it requires an adequate ripple current rating. Its RMS current rating should be greater than approximately 1/2 of the DC load current.

For insuring stable operation C1 should be placed as close to the IC as possible. Alternately, a smaller high quality ceramic 0.1µF capacitor may be placed closer to the IC and a larger capacitor placed farther away. If using this technique, it is recommended that the larger capacitor be a tantalum or electrolytic type. All ceramic capacitors should be placed close to the MP2374.

Output Capacitor (C5)

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple low. The characteristics of the output capacitor also affect the stability of the regulation control system. Ceramic, tantalum or low ESR electrolytic capacitors are recommended. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated to be:

$$V_{RIPPLE} \cong 1.4 \times V_{IN} \times \left(\frac{f_{LC}}{f_{SW}} \right)^2$$

Where V_{RIPPLE} is the output ripple voltage, f_{LC} is the resonant frequency of the LC filter, f_{SW} is the switching frequency.

In the case of tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, and so the output ripple is calculated as:

$$V_{RIPPLE} \cong \Delta I \times R_{ESR}$$

Where V_{RIPPLE} is the output voltage ripple and R_{ESR} is the equivalent series resistance of the output capacitors.

Output Rectifier Diode (D1)

The output rectifier diode supplies the current to the inductor when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, use a Schottky rectifier.

Table 2 lists manufacturer's websites.

Table 2—Schottky Diode Manufacturers

#	Vendor	Web Site
1	Diodes, Inc.	www.diodes.com
2	Fairchild Semiconductor	www.fairchildsemi.com
3	General Semiconductor	www.gensemi.com
4	International Rectifier	www.irf.com
5	On Semiconductor	www.onsemi.com
6	Pan Jit International	www.panjit.com.tw

Choose a rectifier whose maximum reverse voltage rating is greater than the maximum input voltage, and whose current rating is greater than the maximum load current.

Compensation

The system stability is controlled through the COMP pin. COMP is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system. The DC loop gain is:

$$A_{VDC} = \frac{V_{REF}}{V_{OUT}} \times A_{VEA} \times G_{CS} \times R_{LOAD}$$

Where V_{REF} is the feedback threshold voltage, 1.230V, A_{VEA} is the transconductance error amplifier voltage gain, 400 V/V, and G_{CS} is the current sense gain (roughly the output current divided by the voltage at COMP), 3.5 A/V.

The system has 2 poles of importance; one is due to the compensation capacitor (C4) and the other is due to the output capacitor (C5). These are:

$$f_{P1} = \frac{G_{MEA}}{(2\pi \times A_{VEA} \times C4)}$$

Where f_{P1} is the first pole, and G_{MEA} is the error amplifier transconductance (770μS) and

$$f_{P2} = \frac{1}{(2\pi \times R_{LOAD} \times C5)}$$

The system has one zero of importance due to the compensation capacitor (C4) and the compensation resistor (R3) which is

$$f_{Z1} = \frac{1}{(2\pi \times R3 \times C4)}$$

If large value capacitors with relatively high equivalent-series-resistance (ESR) are used, the zero due to the capacitance and ESR of the output capacitor can be compensated by a third pole set by R3 and C3

$$f_{P3} = \frac{1}{(2\pi \times R3 \times C3)}$$

The system crossover frequency $f_{C,}$ (the frequency where the loop gain drops to 1, or 0dB) is important. A good rule of thumb is to set the crossover frequency to approximately one tenth of the switching frequency. In this case, the switching frequency is 330KHz, so use a crossover frequency of 33KHz. Lower crossover frequencies result in slower response and worse transient load recovery. Higher crossover frequencies can result in instability.

Choosing the Compensation Components

The values of the compensation components given in Table 3 yield a stable control loop for the output voltage and given capacitor.

Table 3—Compensation Values for Typical Output Voltage/Capacitor Combinations

V_{OUT}	C5	R3	C3	C4
2.5V	22μF Ceramic	3.9kΩ	None	4.7nF
3.3V	22μF Ceramic	5.1kΩ	None	3.9nF
5V	22μF Ceramic	7.5kΩ	None	2.7nF
12V	22μF Ceramic	18kΩ	None	1.2nF
2.5V	47μF SP-Cap	8.2kΩ	None	2.2nF
3.3V	47μF SP-Cap	10kΩ	None	2.2nF
5V	47μF SP-Cap	16kΩ	None	1.5nF
12V	47μF SP-Cap	36kΩ	None	1nF
2.5V	560μF/6.3V, AL 30mΩ ESR	100kΩ	150pF	1nF
3.3V	560μF/6.3V, AL 30mΩ ESR	120kΩ	120pF	1nF
5V	470μF/10V, AL 30mΩ ESR	150kΩ	82pF	1nF
12V	220μF/25V, AL 30mΩ ESR	180kΩ	33pF	1nF

Note: “AL” = Electrolytic

To optimize the compensation components that are not listed in Table 4, use the following procedure.

Choose the compensation resistor to set the desired crossover frequency. Determine the value by the following equation:

$$R3 = \frac{2\pi \times C5 \times V_{OUT} \times f_C}{G_{EA} \times G_{CS} \times V_{REF}}$$

Putting in the know constants and setting the crossover frequency to the desired 33KHz:

$$R3 \cong 6.88 \times 10^7 \times C5 \times V_{OUT}$$

Choose the compensation capacitor to set the zero below one fourth of the crossover frequency. Determine the value by the following equation:

$$C4 > \frac{2}{\pi \times R3 \times f_C} \approx \frac{1.93 \times 10^{-5}}{R3}$$

Determine if the second compensation capacitor, C3, is required. It is required if the ESR zero of the output capacitor occurs at less than four times the crossover frequency, or

$$8\pi \times C5 \times R_{ESR} \times f_C \geq 1$$

If this is the case, then add the second compensation resistor. Determine the value by the equation:

$$C3 = \frac{C5 \times R_{ESR(MAX)}}{R3}$$

Where $R_{ESR(MAX)}$ is the maximum ESR of the output capacitor.

Example:

V_{OUT} = 5V, C5 = 22μF Ceramic (ESR = 10mΩ)

$R3 \approx 6.88x10^7 (22x10^{-6}) (5) = 7568\Omega$

Use the nearest standard value of 7.5kΩ.

$C4 > 1.93x10^{-5} / 7.5K = 2.57nF$

Use standard value of 2.7nF.

8π x C5 x R_{ESR} x f_C = 0.22, which is less than 1. Therefore, no second compensation capacitor (C3) is required.

PCB Layout Guide

PCB layout is very important to achieve stable operation. Please follow these guidelines and take Figure2 and 3 for references.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side and low-side MOSFETs.
2) Keep the connection of low-side MOSFET between SW pin and input power ground as short and wide as possible.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability. For single layer, do not solder exposed pad of the IC

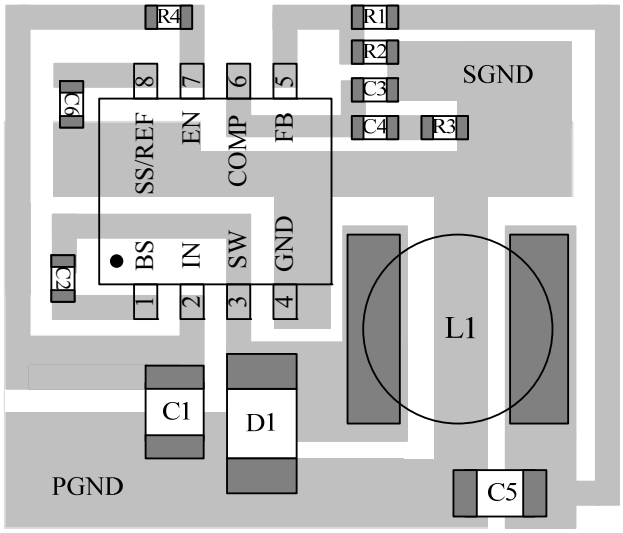
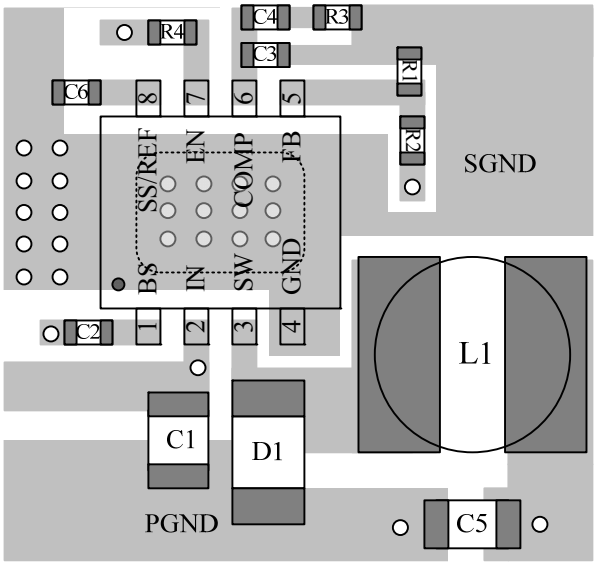
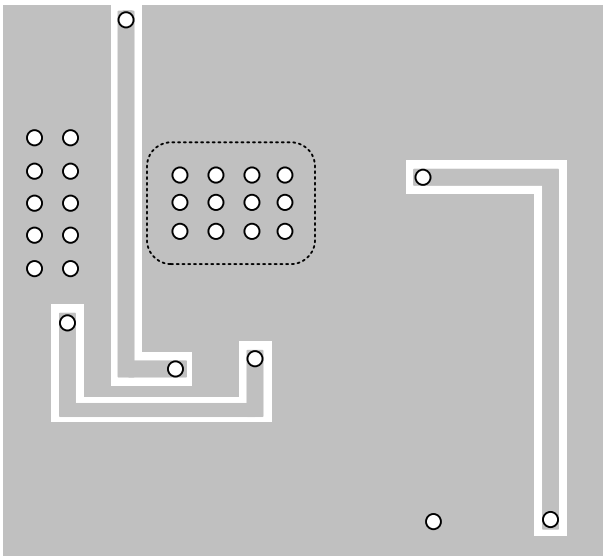


Figure 2—PCB Layout (Single Layer)



Top Layer



Bottom Layer

Figure 3—PCB Layout (Double Layer)

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT}=5V or 3.3V; and
- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Fig.4

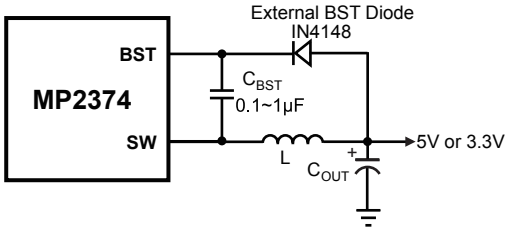


Figure 4—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

TYPICAL APPLICATION CIRCUITS

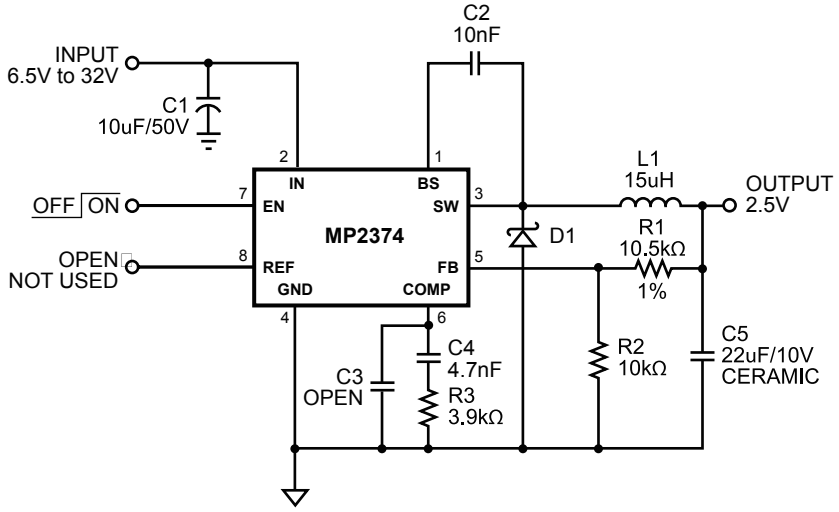


Figure 5—MP2374 with Murata 22µF / 10V Ceramic Output Capacitor

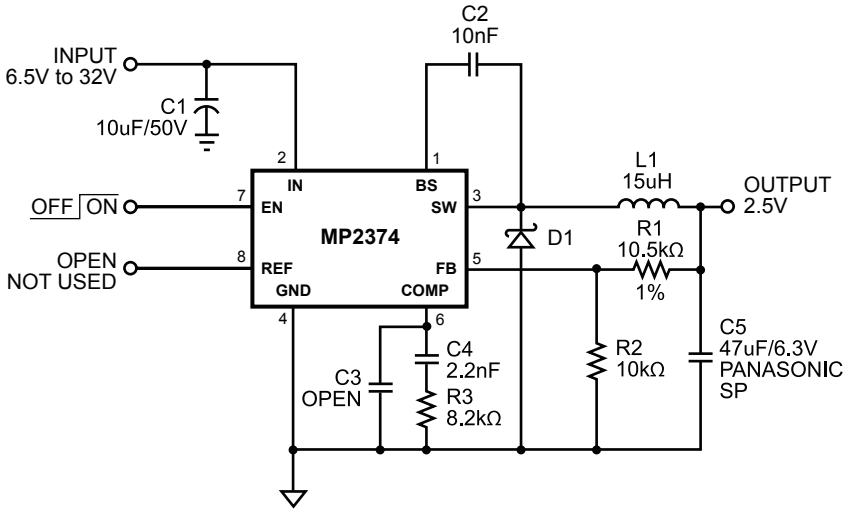
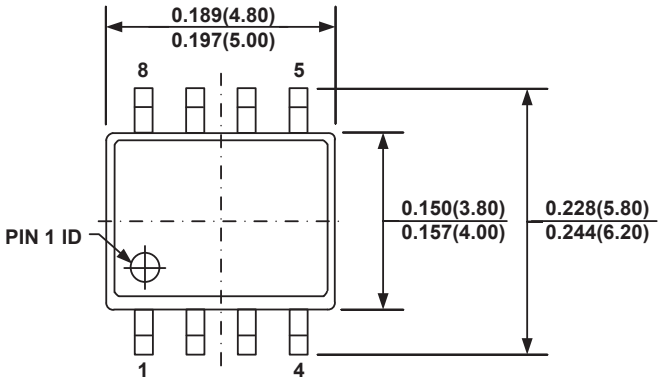


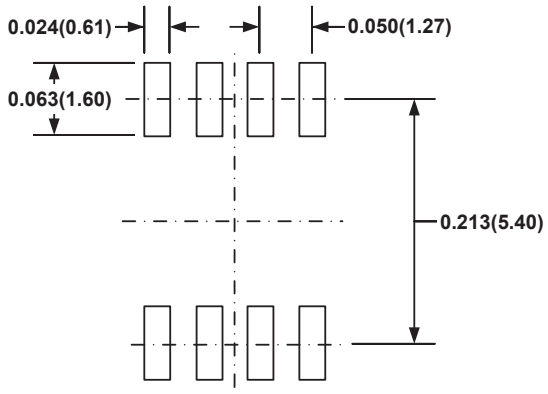
Figure 6—MP2374 with Panasonic 47µF / 6.3V Special Polymer Output Capacitor

PACKAGE INFORMATION

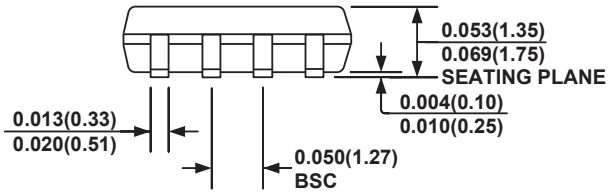
SOIC8



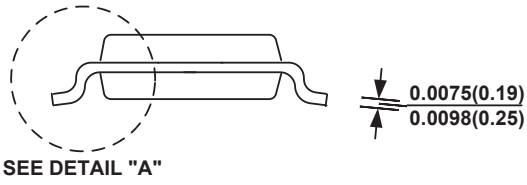
TOP VIEW



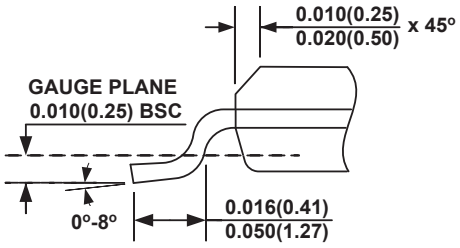
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.