Class AB Stereo Headphone Driver with Mute

Features

- High Signal-to-Noise Ratio
- High Slew Rate
- Low Distortion
- Large Output Voltage Swing
- Flexible Mute Function
- Excellent Power Supply Ripple Rejection
- Low Power Consumption
- Short-circuit Elimination
- Wide Temperature Range
- No Switch ON/OFF Clicks
- Integrated Voltage Divider (V_{DD}/2) to Eliminate External Resistors

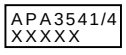
Applications

- Portable Digital Audio

General Description

The APA3541/4 is an integrated class AB stereo headphone driver contained in an SO-8 or a DIP-8 plastic package with Mute feature . Besides the common Mute feature , the APA3541/4 further integrates a voltage divider inside the chip . Thus , the external resistors can be eliminated . The APA3541 has a fixed gain of 0dB and the APA3544 has a fixed gain of 6dB so that external gain setting is unnecessary. The device is fabricated in a CMOS process and has been primarily developed for portable digital audio applications .

Ordering and Marking Information

<table>
<tr><td>APA3541/4 □□-□□
Handling Code
Temp. Range
Package Code</td><td>Package Code
J : PDIP - 8 K : SOP - 8
Y : Chip From
Temp. Range
I : - 40 to 85° C
Handling Code
TU : Tube TR : Tape & Reel</td></tr>
<tr><td>APA3541/4 J :
  </td><td>XXXXX - Date Code</td></tr>
<tr><td>APA3541/4 K :
  </td><td>XXXXX - Date Code</td></tr>
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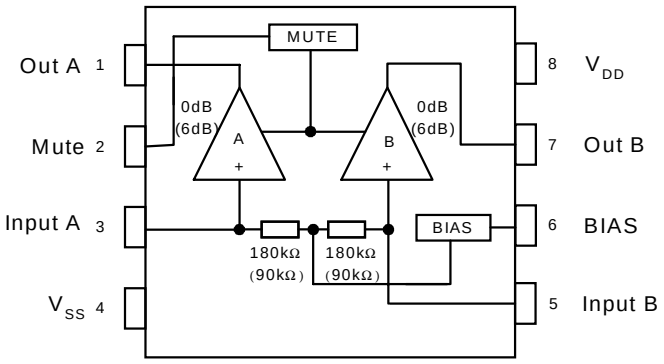
Block Diagram



* The values in parenthessis are for the APA3544.

Function Pin Description

Pin Name	I/O	Function Description
Out A	O	A channel output pin
Mute	I	Chip disable control input, low active and high for normal operating
Input A	I	A channel input terminal
V_{SS}		Power ground pin
Input B	I	B channel input terminal
BIAS	I	Right channel bias input pin
OUT B	O	B channel output pin
V_{DD}		Power input pin

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	7	V
$t_{SC(O)}$	Output Short-circuit Duration, at T_A=25°C, P_{tot}=1W	20	S
T_A	Operating Ambient Temperature range	-40 to 85	°C
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Soldering Temperature,10 seconds	300	°C
V_{ESD}	Electrostatic Discharge	-3000 to 3000 *1	V

Note: 1. Human body model : C=100pF, R=1500Ω, 3 positive pulses plus 3 negative pulses

Thermal Characteristics

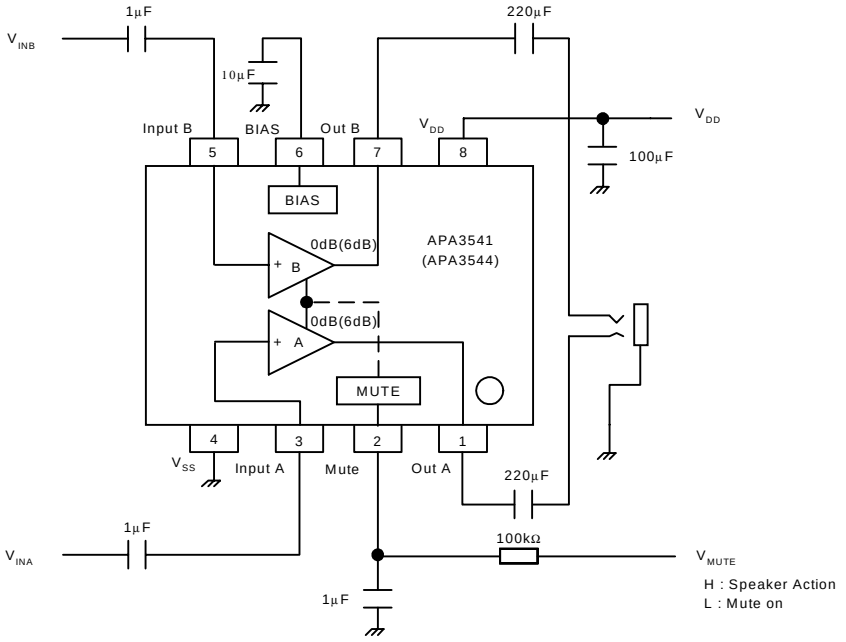
Symbol	Parameter	Rating	Unit
R_{THJA}	Thermal Resistance from Junction to Ambient in Free Air		
	DIP-8	108	K/W
	SOP-8	210	
R_{THJC}	Thermal Resistance from Junction to Case		
	DIP-8	45	K/W
	SOP-8	40	

Electrical Characteristics

V_{IN}=0dBV, V_{CC}=5V, T_A=25°C, f=1kHz, R_L=32Ω (unless otherwise noted)

Symbol	Parameter	Test Condition		APM3541/4			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply Voltage			3.0	5.0	6.0	V
I_Q	Quiescent Current	VIN= 0 Vrms			3.5	5	mA
Imute	Mute Current				200		μA
V_{TM}	Mute Terminal Voltage			0.3	0.7	1.6	V
ΔG_{VCL}	Differential Channel Voltage Gain			-0.5	0	0.5	dB
G_{VCL}	Voltage Gain	Vin=1Vrms,f= 1kHz,RL=32Ω	APA3541	-2	0	2	dB
		Vin=0.5Vrms, f=1kHz,Rl=32Ω	APA3544	4	6	8	
THD	Total Harmonic Channel Distortion Factor	BW<80kHz			0.03	0.1	%
P_{U1}	Rated Output Power1	RL=32Ω,THD+N=0.1%,BW<80kHz	APA3541	50	55		mW
			APA3544	75	80		
P_{U2}	Rated Output Power2	RL=16Ω,THD+N=0.1%,BW<80kHz	APA3541	105	110		mW
			APA3544	140	145		
V_{NO}	Output Noise Voltage	BW=20~20kHz , Vin=0Vrms			-93	-85	dBV
CS	Channel Separation	F=1kHz	APA3541	-90	-95		dB
			APA3544	-65	-70		
ATT	Mute Attenuation	VIN=1Vrms,f=1kHz,Mute=L		65	70		dB
RR	Ripple Rejection	F_{RR}=100Hz,V_{RR}=-20dBV		50	60		dB

Test and Application Circuit



Typical Characteristics

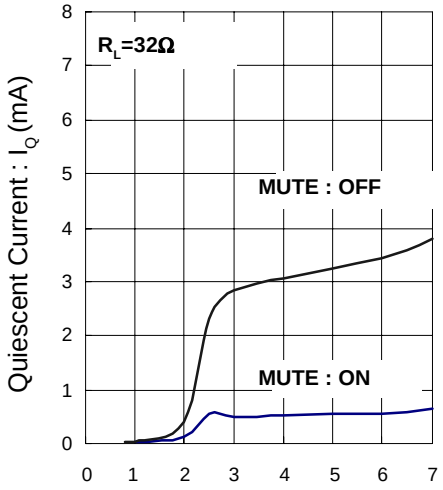


Figure 1 : Supply Voltage : V_{DD} (V)

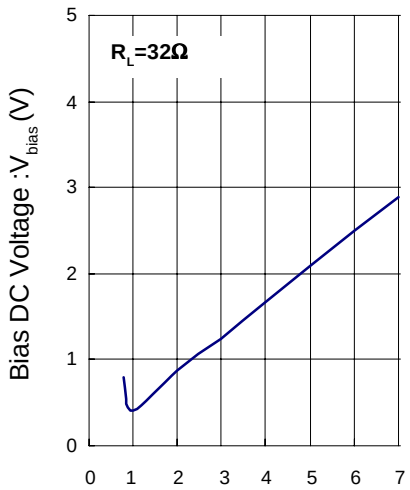


Figure 2 : Supply Voltage : V_{DD} (V)

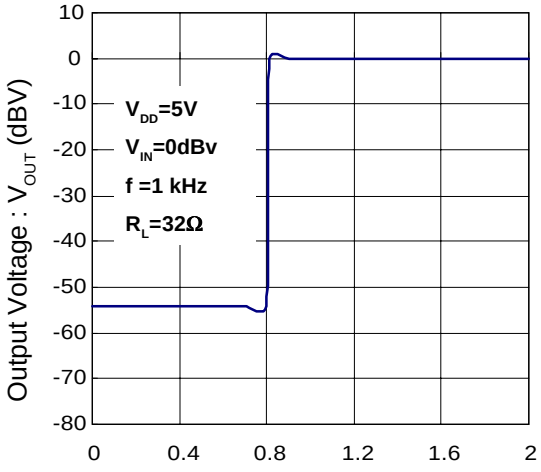


Figure 3 : Mute Control Voltage : V_{TM} (V)

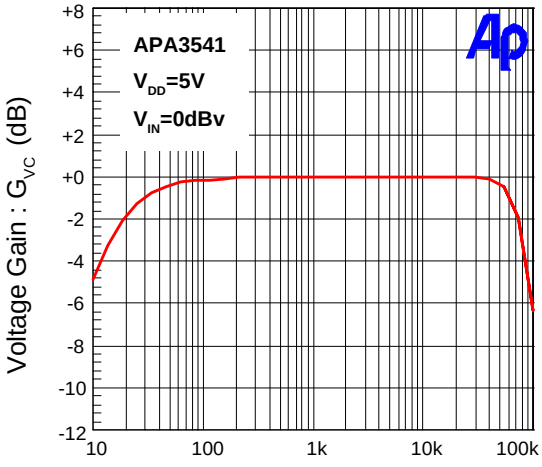


Figure 4 : Frequency :f (Hz)

Typical Characteristics Cont.

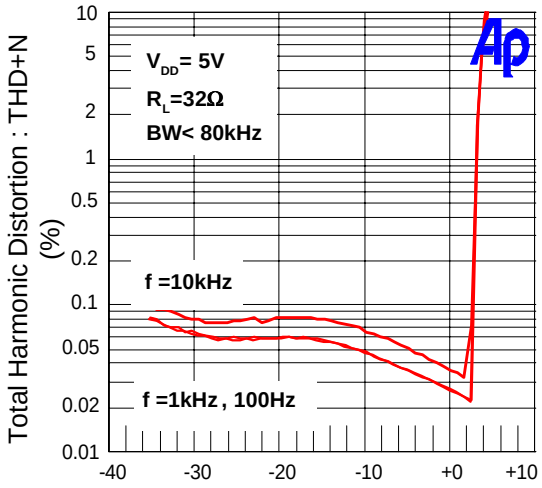


Figure 5 : Output Voltage : V_{OUT} (dBv)

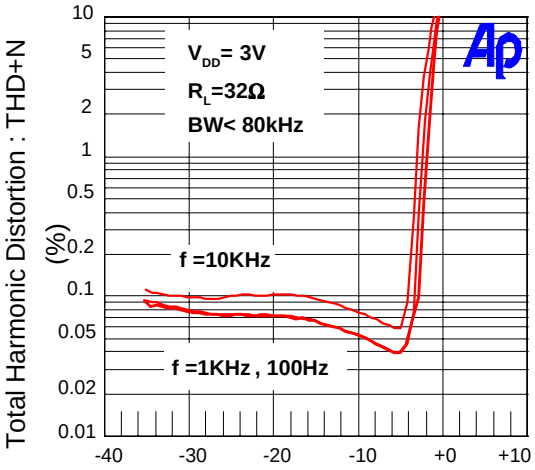


Figure 6 : Output Voltage : V_{OUT} (dBv)

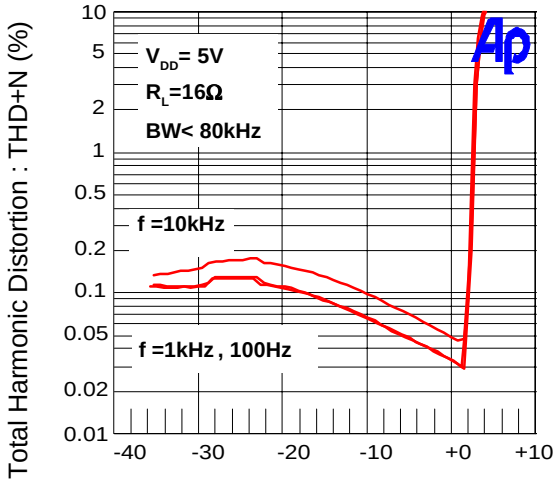


Figure 7 : Output Voltage : V_{OUT} (dBv)

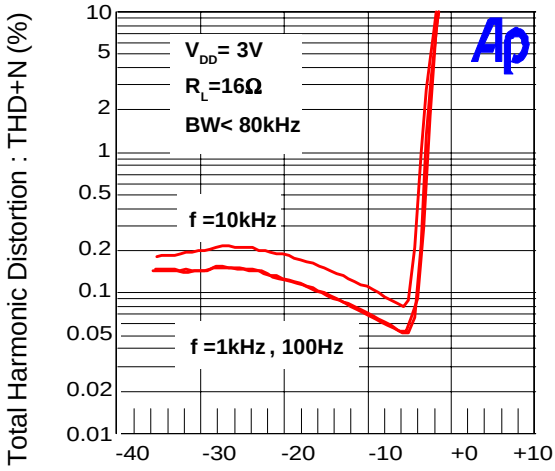


Figure 8 : Output Voltage : V_{OUT} (dBv)

Typical Characteristics Cont.

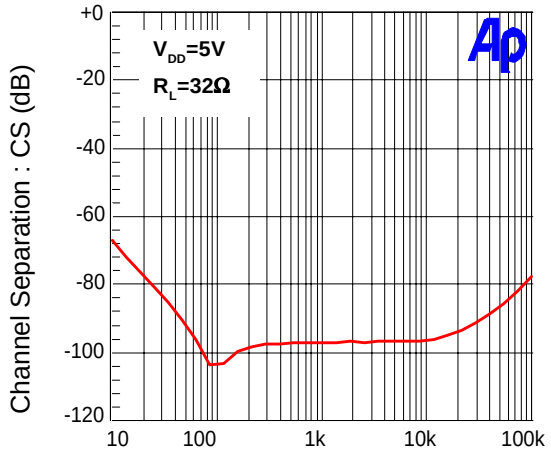


Figure 9 : Frequency :f (Hz)

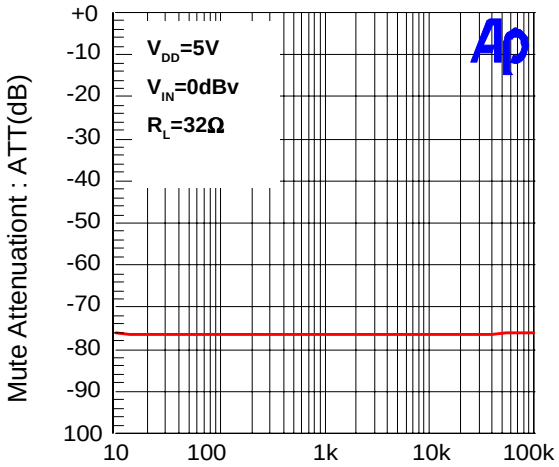


Figure 10 : Frequency :f (Hz)

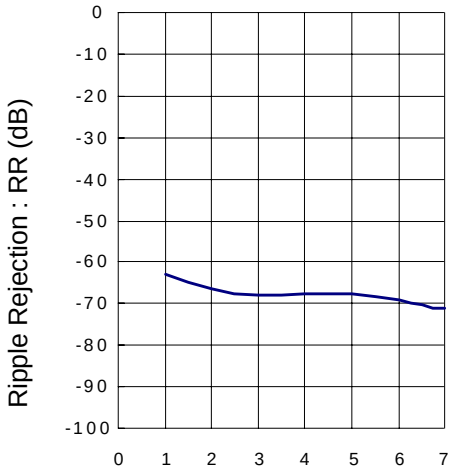


Figure 11 : Supply Voltage : V_{DD} (V)

Application Note

Input Capacitor , Ci

In the typical application an input capacitor , Ci , is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation . In this case , the external capacitor Ci and the internal resistance Ri form a high-pass filter with the corner frequency determined in the follow equation:

$$fc\ (highpass) = 1/(2\pi RiCi) \quad (1)$$

The value of Ci is important to consider as it directly affects the low frequency performance of the circuit. Consider the APA3541 where Ri is 180kΩ and APA3544 is 90kΩ internal fixed . Equation is reconfigured as follow:

$$Ci = 1/(2\pi * 180k\Omega * fc) \text{ for APA3541}$$
$$Ci = 1/(2\pi * 90k\Omega * fc) \text{ for APA3544} \quad (2)$$

And the ceramic capacitor is recommanded.

Bias Capacitor , Cb

As with any power amplifier , proper supply bypassing is critical for low noise performance and high power supply rejection . The capacitor location on both the bypass and power supply pins should be as close to the device as possible . The effect of a larger half supply bias capacitor is improved PSRR due to increased half-supply stability . Typical applications employ a 5V regulator with 10µF and a 0 . 1µF bias capacitors which aid in supply filtering .

This does not eliminate the need for bypassing the supply nodes of the APA3541/4 . The selection of bias capacitors , especially Cb , is thus dependent upon desired PSRR requirements , click and pop performance . The capacitor is fed from a 95kΩ source inside the amplifier . To keep the start-up pop as low as possible , the relationship shown in equation should be maintained .

$$1/(Cb * 95k\Omega) \leq 1/\{Ci * Ri\} \quad (3)$$

As an example , consider a circuit where Cb is 4.7µF, Ci is 1µF and APA3541 Ri is 180kΩ . Inserting these values into the equation we get 2.24≤ 5.55 which satisfies the rule . Bias capacitor , Cb , values of 2.2µF to 10µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance .

Output Coupling Capacitor, Cc

In the typical single-supply SE configuration , an output coupling capacitor (Cc) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load . As with the input coupling capacitor , the output coupling capacitor and impedance of the load form a high-pass filter governed by equation .

$$fc(highpass) = 1/(2\pi R_L Cc) \quad (4)$$

For example , a 220µF capacitor with an 32Ω speaker would attenuate low frequencies below 22Hz . The main disadvantage , from a performance standpoint , is the load impedance is typically small , which drives the low-frequency corner higher degrading the bass response . Large values of Cc are required to pass low frequencies into the load .

Optimizing Depop Circuitry

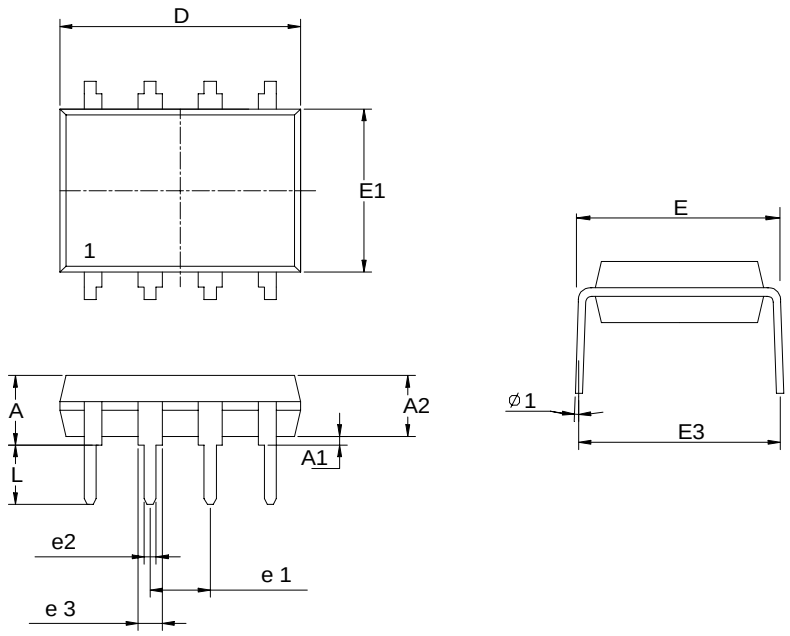
When the amplifier is in mute mode , both of the output stage and input bypass continues to be biased . And no pop noise will be heard during the transition out of mute mode .

Power Supply Decoupling, Cs

APA3541/4 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible . Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker . The optimum decoupling is achieved by using two different type capacitors that target on different type of noise on the power supply leads . For higher frequency transients , spikes , or digital hash on the line , a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device V_{DD} lead works best . For filtering lower-frequency noise signals , a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended .

Packaging Information

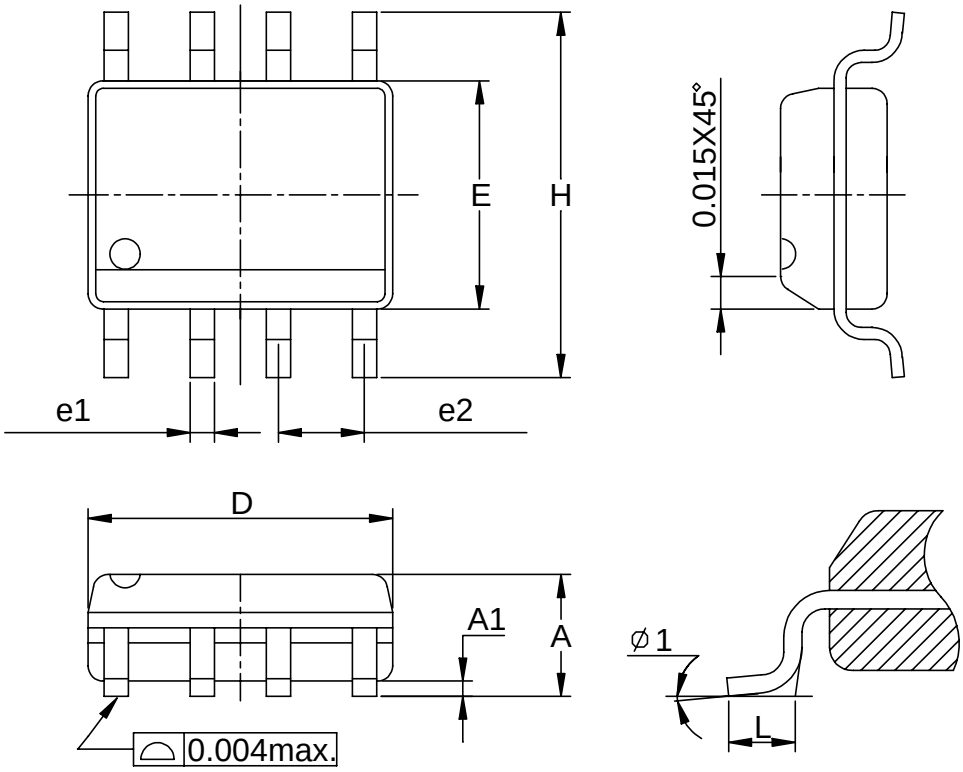
PDIP-8 pin (Reference JEDEC Registration MS-001)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	3.68	0.115	0.145
D	9.02	10.16	0.355	0.400
e1	2.54BSC		0.100BSC	
e2	0.36	0.56	0.014	0.022
e3	1.14	1.78	0.045	0.070
E	7.62 BSC		0.300 BSC	
E1	6.10	7.11	0.240	0.280
E3		10.92		0.430
L	2.92	3.81	0.115	0.150
ϕ 1	15°		15°	

Packaging Information

SOP-8 pin (Reference JEDEC Registration MS-012)



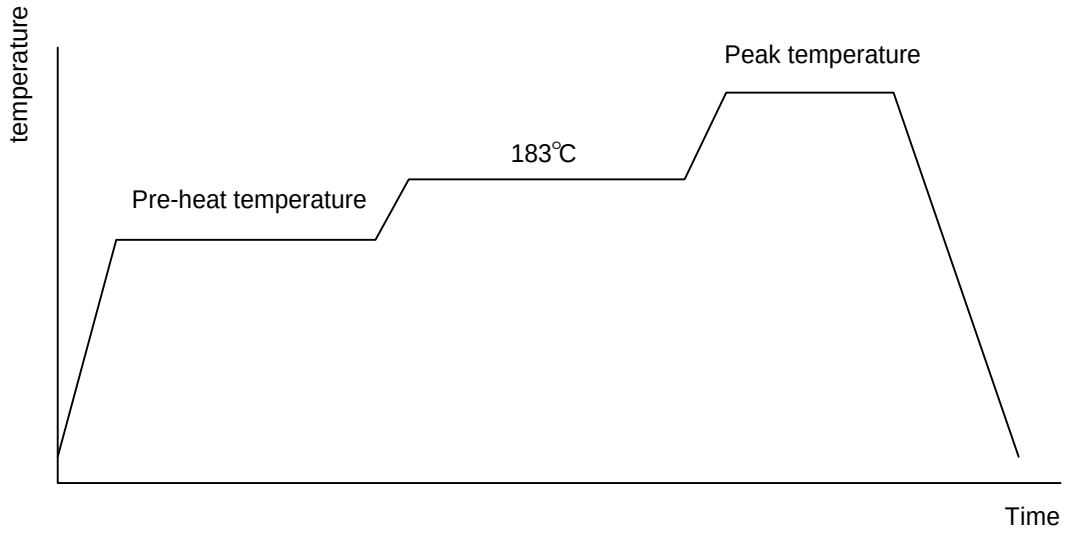
Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	8°		8°	

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A APRIL 1999



Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183°C to Peak)	3°C/second max.	10 °C /second max.
Preheat temperature 125 ± 25°C)	120 seconds max	
Temperature maintained above 183°C	60 – 150 seconds	
Time within 5°C of actual peak temperature	10 –20 seconds	60 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C	215-219°C or 235 +5/-0°C
Ramp-down rate	6 °C /second max.	10 °C /second max.
Time 25°C to peak temperature	6 minutes max.	

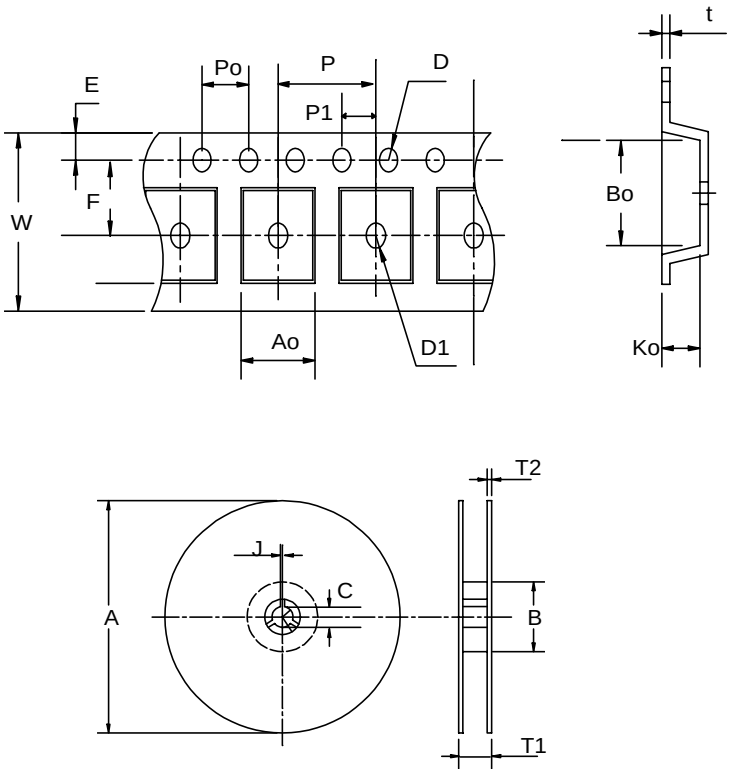
Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bgas	pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm³	pkg. thickness < 2.5mm and pkg. volume < 350mm³
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

Reliability test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245° C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C , 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Carrier Tape & Reel Dimensions



Application	A	B	C	J	T1	T2	W	P	E
SOP- 8	330 ± 1	62 +1.5	12.75+ 0.15	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12± 0. 3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5± 1	1.55 +0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0. 1	2.1± 0.1	0.3±0.013

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8	12	9.3	2500

Customer Service

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Fax : 886-2-89191369