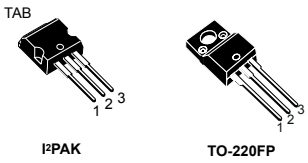
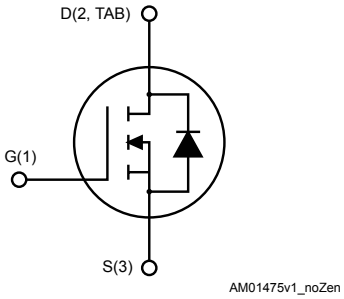
N-channel 600 V, 0.4 Ω typ., 11 A, MDmesh™ II Power MOSFETs in I²PAK and TO-220FP packages





Features

Order codes	V_{DSS} (@ T_{Jmax})	$R_{DS(on)}$ max.	I_D	Package
STB11NM60-1	650 V	0.45 Ω	11 A	I²PAK
STP11NM60FP				TO-220FP

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high-efficiency converters.

Product status link
STB11NM60
STP11NM60FP

Product summary	
Order code	**STB11NM60-1**
Marking	B11NM60
Package	I²PAK
Packing	Tube
Order code	**STP11NM60FP**
Marking	P11NM60FP
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		I²PAK	TO-220FP	
V_{DS}	Gate-source voltage	600		V
V_{GS}	Gate- source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	11	11 (1)	A
I_D	Drain current (continuous) at T_C= 100 °C	7 (1)		
I_{DM} (2)	Drain current (pulsed)	44 (1)		A
P_{TOT}	Total dissipation at T_C = 25 °C	160	35	W
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)		2.5	kV
T_{stg}	Storage temperature range	-65 to 150		°C
T_j	Operating junction temperature range			

1. *Limited by maximum maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 11 A, di/dt ≤ 400 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}.*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		I²PAK	TO-220FP	
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.78	3.57	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5		

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_{jmax})	5.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	350	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±30 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5.5 A		0.4	0.45	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 25 V, f = 1 MHz, V_{GS} = 0 V	-	1000	-	pF
C_{oss}	Output capacitance		-	230	-	pF
C_{rss}	Reverse transfer capacitance		-	25	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	100	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 11 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	30	-	nC
Q_{gs}	Gate-source charge		-	10	-	nC
Q_{gd}	Gate-drain charge		-	15	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 5.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	20	-	ns
t_r	Rise time		-	20	-	ns
$t_{r(Voff)}$	Off-voltage rise time	V_{DD} = 480 V, I_D = 11 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 15. Test circuit for inductive load switching and diode recovery times and Figure 18. Switching time waveform)	-	6	-	ns
t_f	Fall time		-	11	-	ns
t_c	Cross-over time		-	19	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
I_{SDM} (1)	Source-drain current (pulsed)		-		44	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 11 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD} = 100 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	390		ns
Q_{rr}	Reverse recovery charge		-	3.8		µC
I_{RRM}	Reverse recovery current		-	19.5		A
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	570		ns
Q_{rr}	Reverse recovery charge		-	5.7		µC
I_{RRM}	Reverse recovery current		-	20		A

1. *Pulse width is limited by safe operating area*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for I²PAK

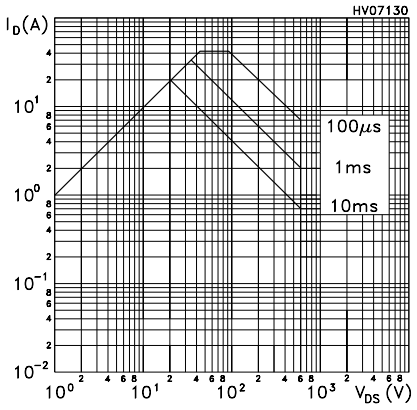


Figure 2. Thermal impedance for I²PAK

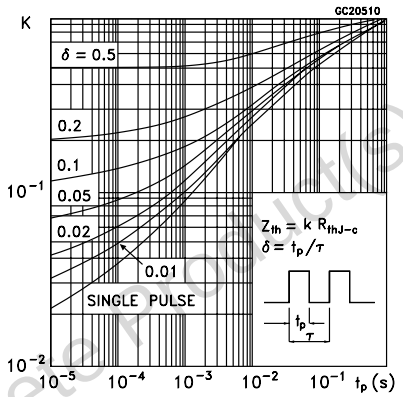


Figure 3. Safe operating area for TO-220FP

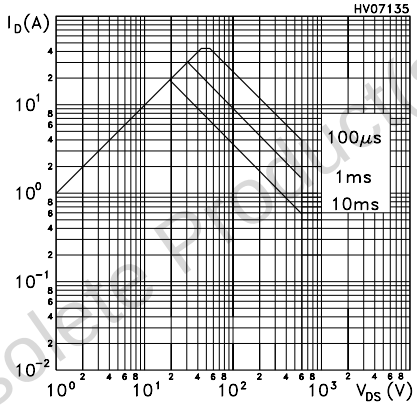


Figure 4. Thermal impedance for TO-220FP

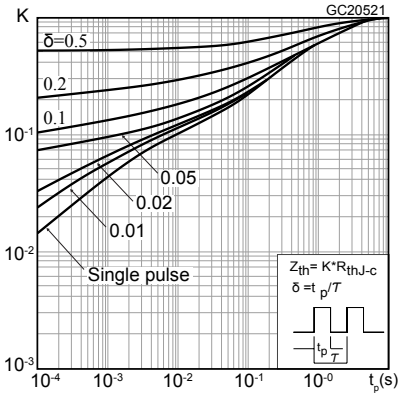


Figure 5. Output characteristics

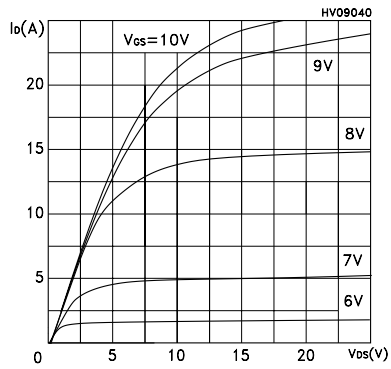


Figure 6. Transfer characteristics

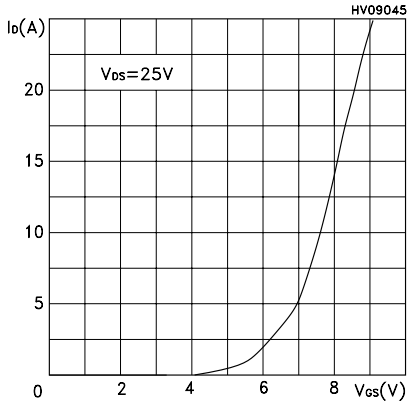


Figure 7. Normalized gate threshold voltage vs temperature

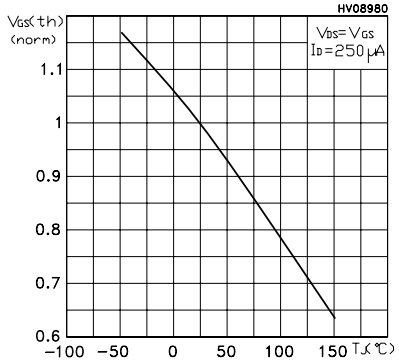


Figure 8. Static drain-source on-resistance

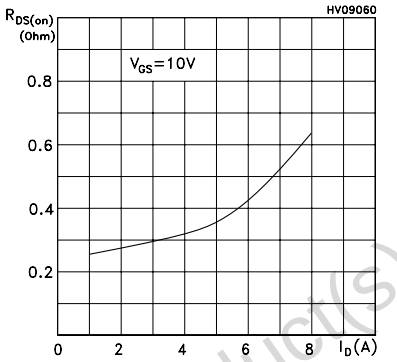


Figure 9. Normalized on-resistance vs temperature

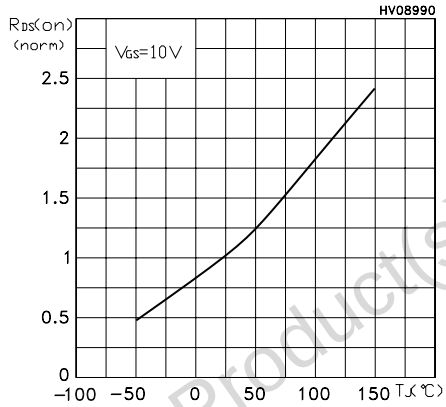


Figure 10. Gate charge vs gate-source voltage

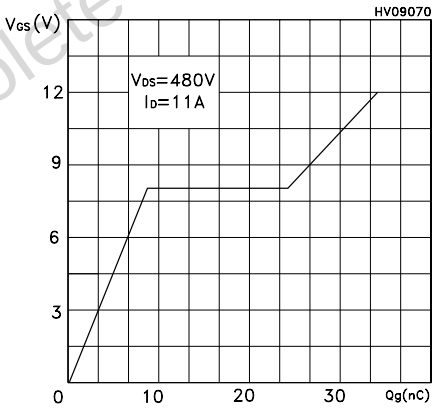


Figure 11. Capacitance variations

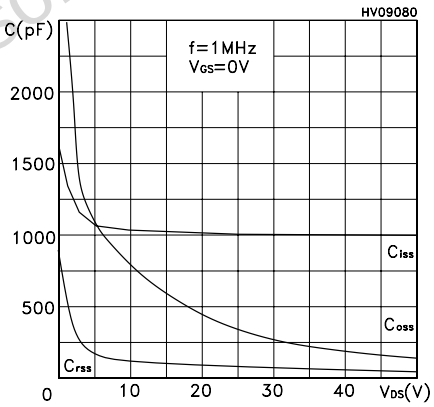
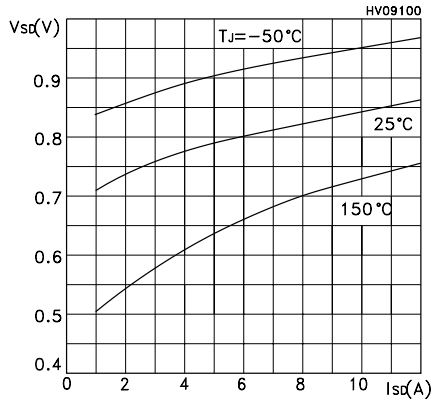


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

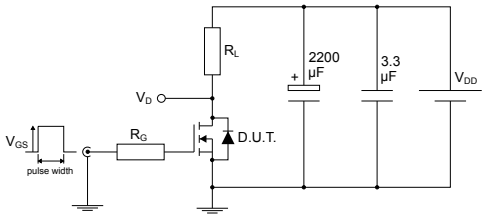


Figure 14. Test circuit for gate charge behavior

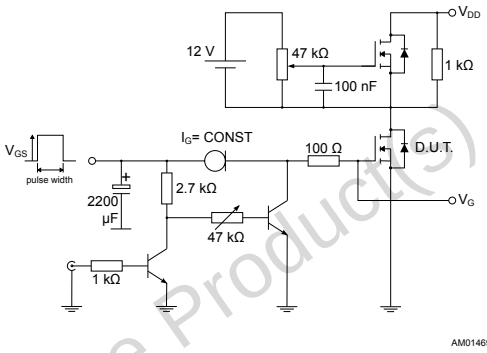


Figure 15. Test circuit for inductive load switching and diode recovery times

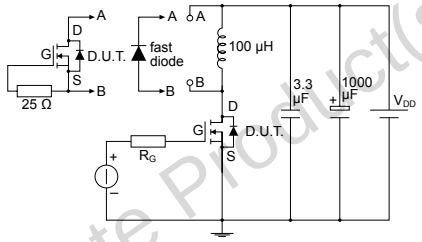


Figure 16. Unclamped inductive load test circuit

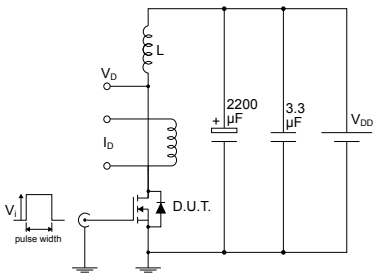


Figure 17. Unclamped inductive waveform

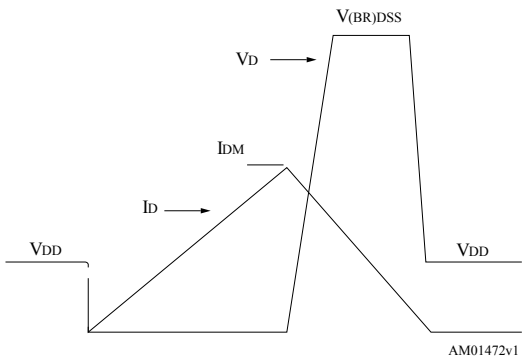
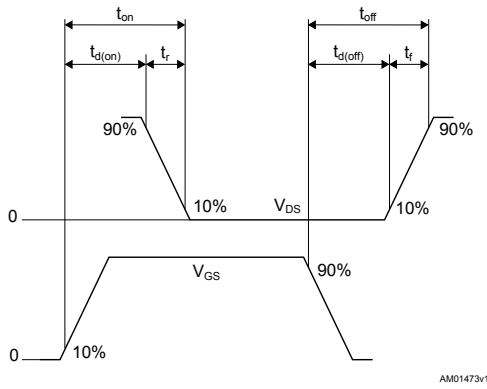


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 I²PAK package information

Figure 19. I²PAK package outline

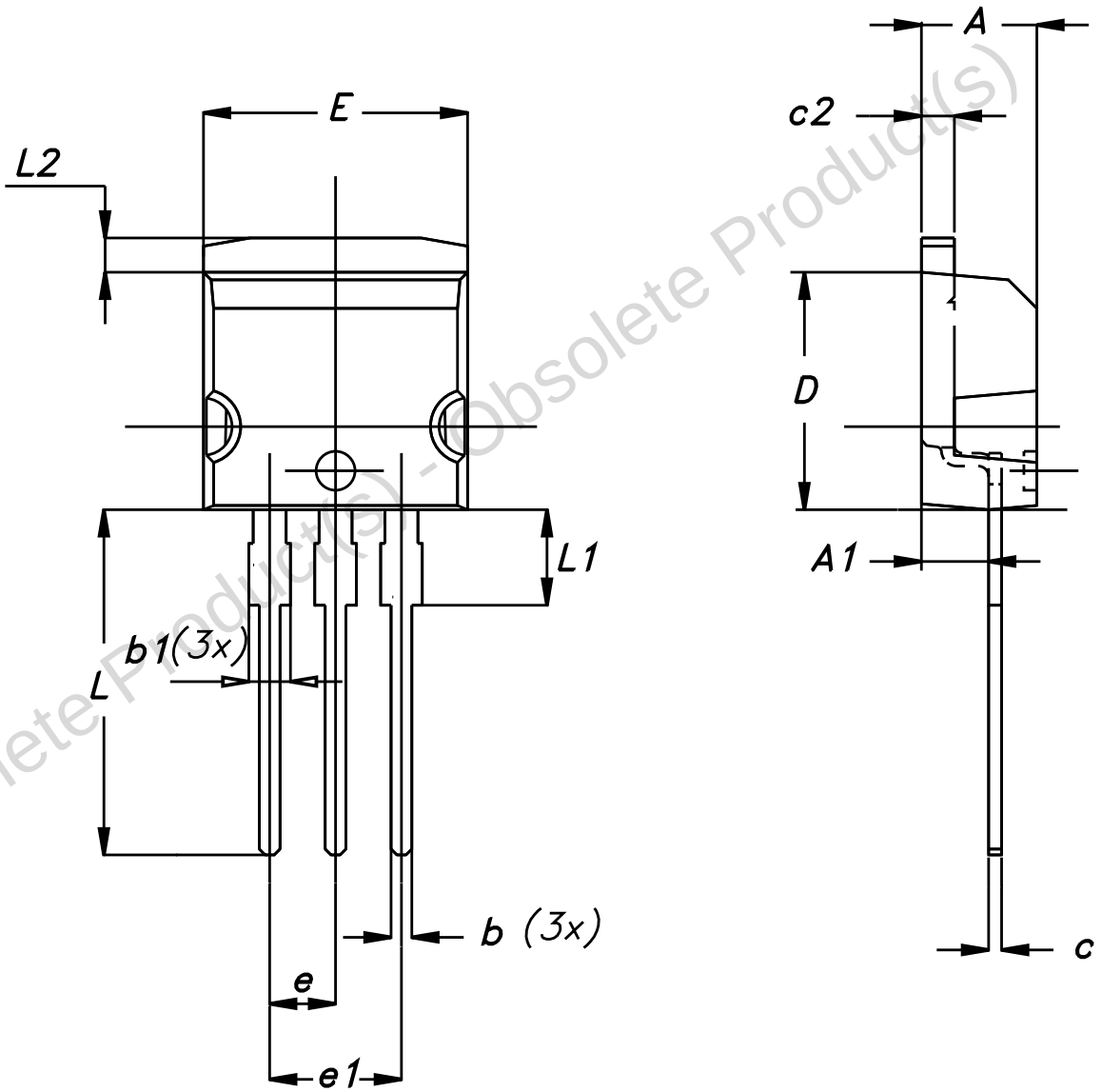


Table 8. I²PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10	-	10.40
L	13	-	14
L1	3.50	-	3.93
L2	1.27	-	1.40

4.2 TO-220FP package information

Figure 20. **TO-220FP package outline**

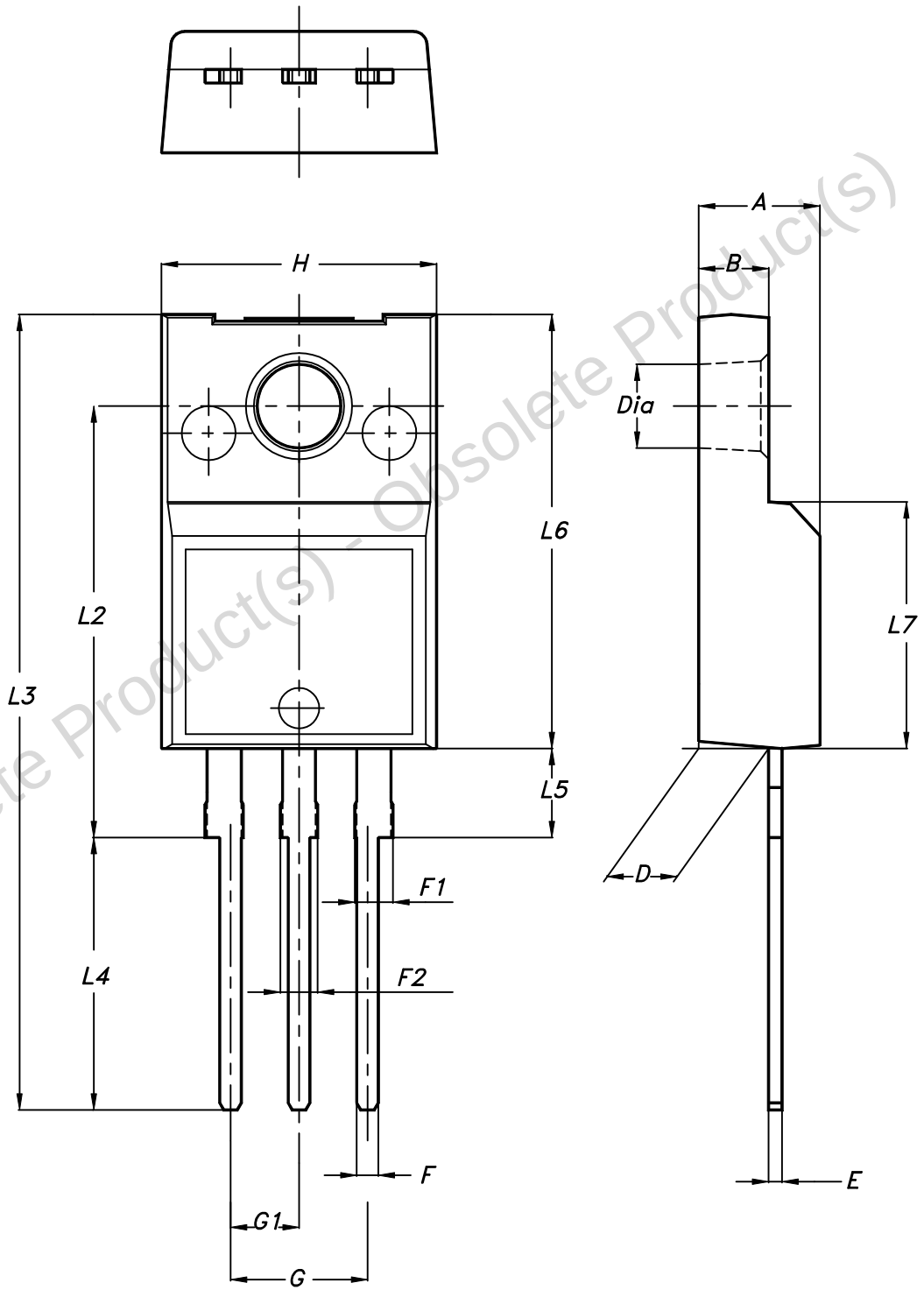


Table 9. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history

Table 10. **Document revision history**

Date	Version	Changes
03-Oct-2018	1	First release. Part numbers previously included in datasheet DocID10135.

Contents

1 **Electrical ratings** 2
2 **Electrical characteristics** 3
2.1 Electrical characteristics (curves) 5
3 **Test circuits** 7
4 **Package information** 8
4.1 I²PAK package information 8
4.2 TO-220FP package information 10
Revision history 13