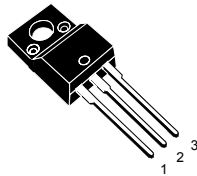
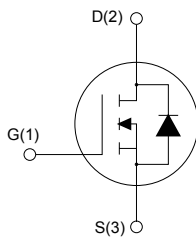


N-channel 800 V, 0.95 Ω typ., 6.5 A MDmesh Power MOSFET in a TO-220FP package



TO-220FP



AM01475v1_noZen_noTab

Features

| Order code | V_{DS} | $R_{DS(on)}$ max. | I_D |
|------------|----------|-------------------|-------|
| STF7NM80 | 800 V | 1.05 Ω | 6.5 A |

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This N-channel Power MOSFET is developed using STMicroelectronics' revolutionary MDmesh technology, which associates the multiple drain process with the company's PowerMESH horizontal layout. This device offers extremely low on-resistance, high dv/dt, and excellent avalanche characteristics. Using STMicroelectronics's proprietary strip technique, this Power MOSFET boasts an overall dynamic performance that is superior to similar products on the market.



Product status link

[STF7NM80](#)

Product summary

| | |
|-------------------|----------|
| Order code | STF7NM80 |
| Marking | F7NM80 |
| Package | TO-220FP |
| Packing | Tube |

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------|------|
| V_{DS} | Drain-source voltage | 800 | V |
| V_{GS} | Gate-source voltage | ±30 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ °C}$ | 6.5 | A |
| | Drain current (continuous) at $T_C = 100\text{ °C}$ | 4 | |
| $I_{DM}^{(1)(2)}$ | Drain current (pulsed) | 26 | A |
| P_{TOT} | Total power dissipation at $T_C = 25\text{ °C}$ | 25 | W |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ °C}$) | 2.5 | kV |
| T_{stg} | Storage temperature range | -55 to 150 | °C |
| T_J | Operating junction temperature range | | °C |

1. This value is limited by maximum junction temperature.
2. Pulse width is limited by safe operating area.

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|------------|---|-------|------|
| R_{thJC} | Thermal resistance, junction-to-case | 5 | °C/W |
| R_{thJA} | Thermal resistance, junction-to-ambient | 62.5 | °C/W |

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AS} | Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.) | 1 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$) | 240 | mJ |

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|---|------|------|-----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$ | 800 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$ | | | 10 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$, $T_C = 125\text{ °C}^{(1)}$ | | | 100 | |
| I_{GSS} | Gate body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 30\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 3.25\text{ A}$ | | 0.95 | 1.05 | Ω |

1. Specified by design, not tested in production.

Table 5. Dynamic

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|---|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 620 | - | pF |
| C_{oss} | Output capacitance | | - | 460 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 15 | - | pF |
| R_g | Gate input resistance | $f = 1\text{ MHz}$ open drain | - | 7 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 640\text{ V}$, $I_D = 6.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior) | - | 18 | - | nC |
| Q_{gs} | Gate-source charge | | - | 4 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 11 | - | nC |

Table 6. Switching times

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 400\text{ V}$, $I_D = 3.25\text{ A}$, | - | 20 | - | ns |
| t_r | Rise time | $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ | - | 8 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform) | - | 35 | - | ns |
| t_f | Fall time | | - | 10 | - | ns |

Table 7. Source-drain diode

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 6.5 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 26 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 6.5 \text{ A}$, $V_{GS} = 0 \text{ V}$ | - | | 1.3 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 6.5 \text{ A}$, $di/dt = 100 \text{ V}$ | - | 460 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 50 \text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times) | - | 4 | | μC |
| I_{RRM} | Reverse recovery current | $V_{DD} = 50 \text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times) | - | 17 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 6.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ | - | 680 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 50 \text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times) | - | 6 | | μC |
| I_{RRM} | Reverse recovery current | $V_{DD} = 50 \text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times) | - | 17 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

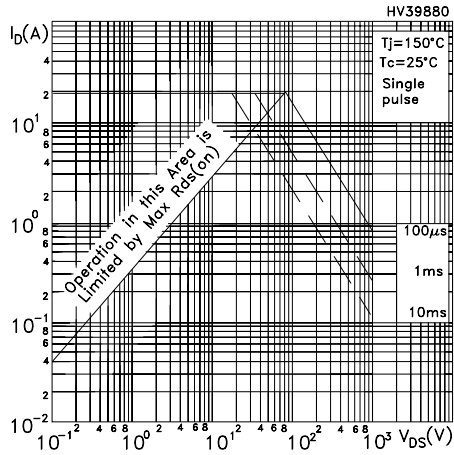


Figure 2. Thermal impedance

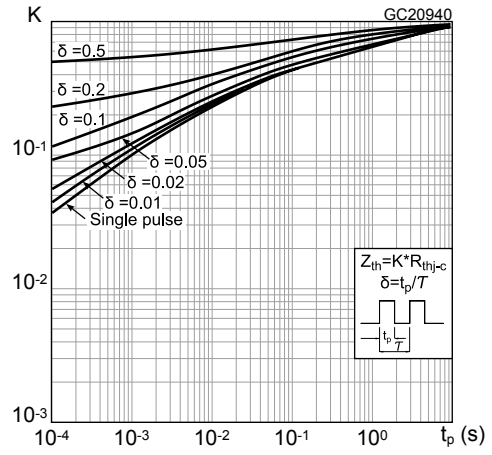


Figure 3. Output characteristics

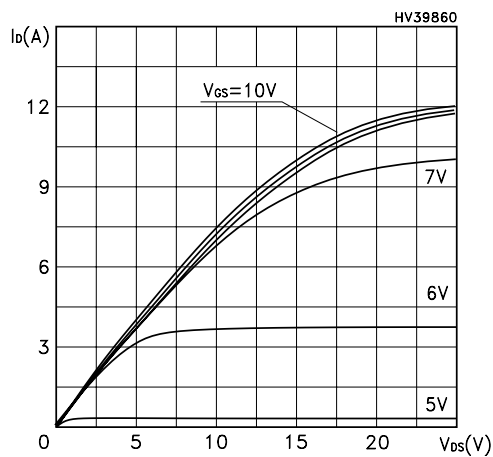


Figure 4. Transfer characteristics

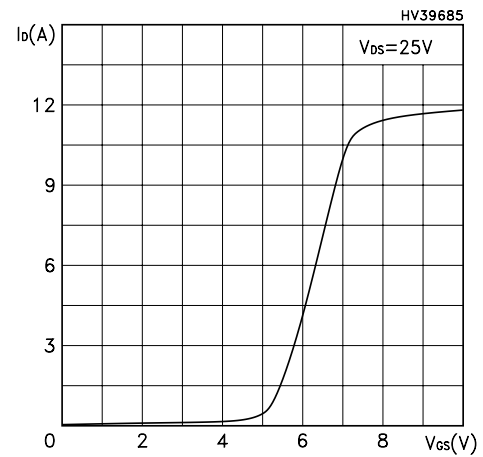


Figure 5. Static drain-source on-resistance

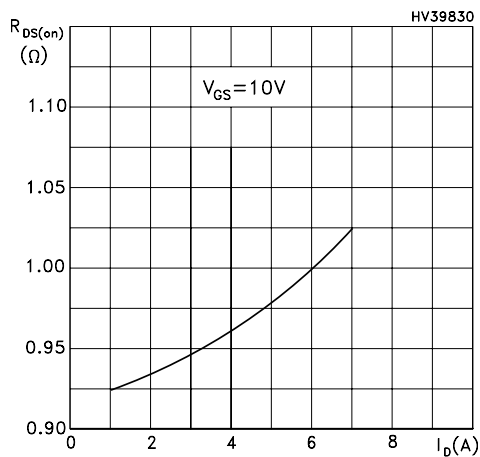


Figure 6. Gate charge vs gate-source voltage

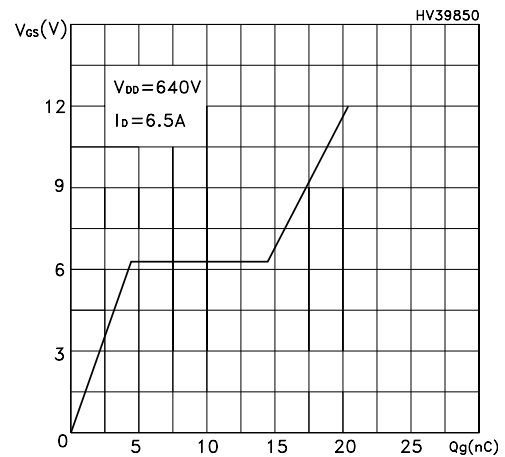


Figure 7. Capacitance variations

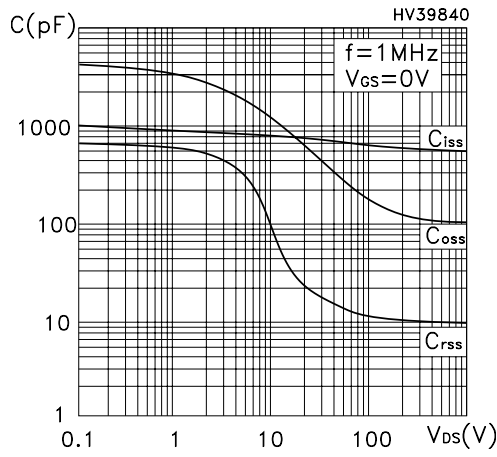


Figure 8. Normalized gate threshold voltage vs temperature

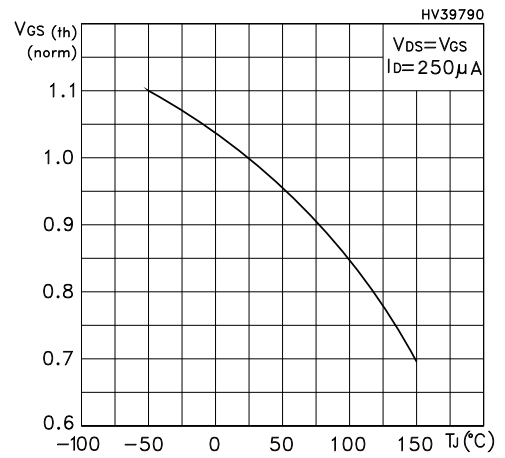


Figure 9. Normalized on-resistance vs temperature

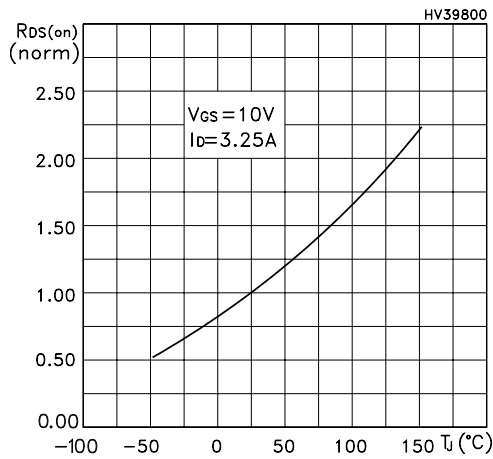


Figure 10. Source-drain diode forward characteristics

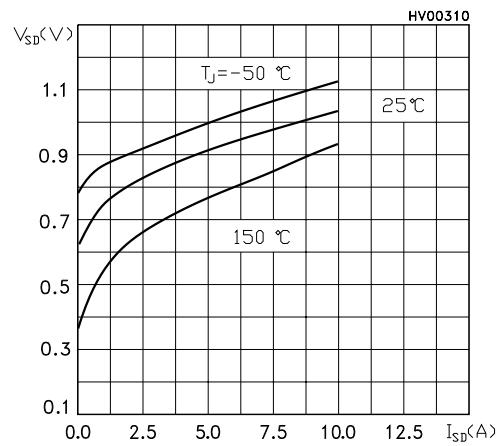
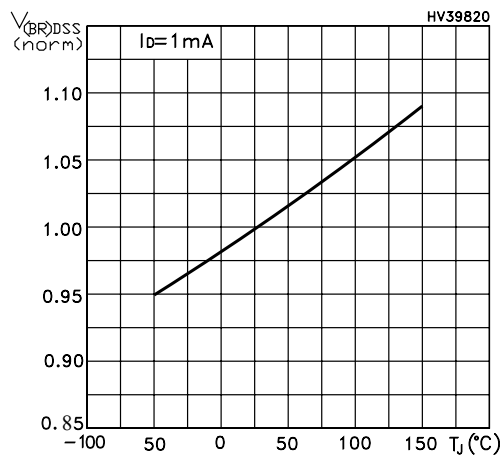


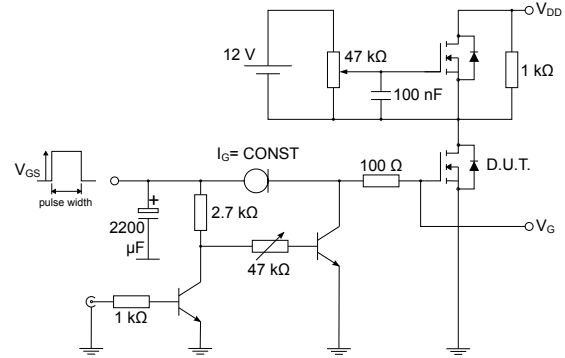
Figure 11. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 12. Test circuit for resistive load switching times

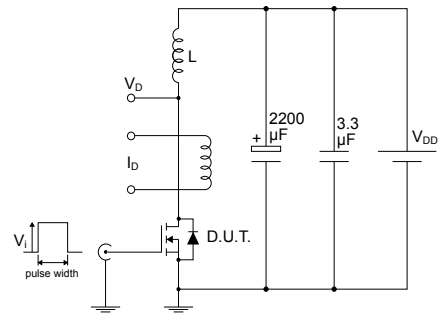

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Figure 13. Test circuit for gate charge behavior


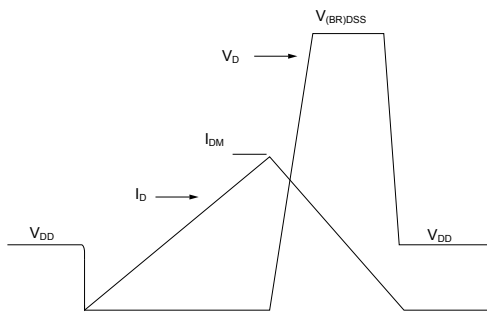
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Figure 14. Test circuit for inductive load switching and diode recovery times


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Figure 15. Unclamped inductive load test circuit


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Figure 16. Unclamped inductive waveform


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Figure 17. Switching time waveform

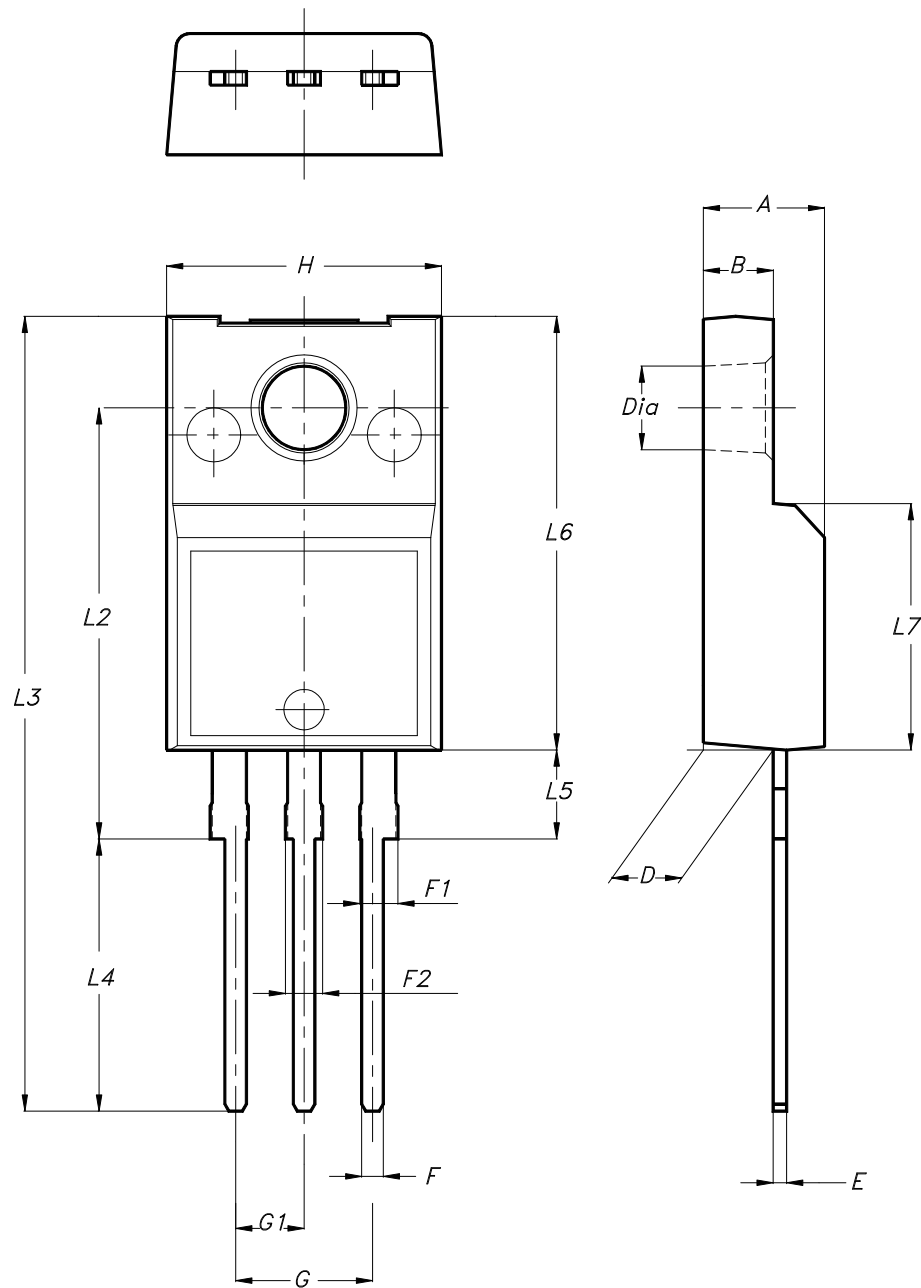

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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 18. TO-220FP type B package outline



7012510_B_rev.14

Table 8. TO-220FP type B package mechanical data

| Dim. | mm | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| B | 2.50 | | 2.70 |
| D | 2.50 | | 2.75 |
| E | 0.45 | | 0.70 |
| F | 0.75 | | 1.00 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.20 |
| G1 | 2.40 | | 2.70 |
| H | 10.00 | | 10.40 |
| L2 | | 16.00 | |
| L3 | 28.60 | | 30.60 |
| L4 | 9.80 | | 10.60 |
| L5 | 2.90 | | 3.60 |
| L6 | 15.90 | | 16.40 |
| L7 | 9.00 | | 9.30 |
| Dia | 3.00 | | 3.20 |

Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 30-May-2023 | 1 | First release. The part number STF7NM80 was previously inserted in the DS4854. |

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