CAT7581

Synchronous Single Buck PWM Controller

CHIP ADVANCED TECHNOLOGY

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Features

- Input Voltage Range from 4.5 V to 13.2 V
- 300 kHz Internal Oscillator
- Voltage Mode PWM Control
- 0.8 V Internal Reference Voltage
- Adjustable Output Voltage
- Internal Soft-Start
- Internal 1.5 A Gate Drivers
- Adaptive Non-Overlap Circuit
- Fast Transient Response, 0~100% Duty Cycle
- Built-in internal compensation
- Input UVLO
- Output Under Voltage Protection and Over Voltage Protection
- Programmable Over Current Protection Monitor $R_{DS(ON)}$ of Low side MOSFET
- SOP8 Package
- RoHS Compliant

Application

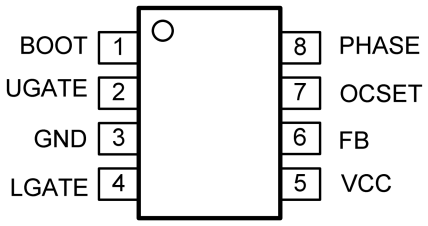
- Graphics Cards
- Desktop Computers
- Servers/Networking
- DSP and FPGA Power Supply
- Telecomm Equipments
- DC-DC Regulator Modules
- LCD Monitor and LCD TV

General Description

The CAT7581 is a voltage mode PWM controller designed to operate from a 4.5 V to 13.2 V supply and produce an output voltage as low as 0.8 V. This 8-pin device provides an optimal level of integration to reduce size and cost of the power supply. The CAT7581 has a fixed 300 kHz oscillator and soft-start function. The CAT7581 provides a 1.5A floating gate driver design to drive N-Channel MOSFETs in a synchronous configuration. The Adaptive non overlap circuitry reduces switching losses by preventing simultaneous conduction of both outputs. Protection features include input Under Voltage LockOut (UVLO), output Under Voltage Protection (UVP), output Over Voltage Protection (OVP), and Over Current Protection (OCP). The OCP monitors the voltage drop across the $R_{DS(ON)}$ of the low side MOSFETs, eliminating the need of a current sensing resistor. The CAT7581 is available in an 8-pin SOIC package.

Pin Configuration

TOP VIEW



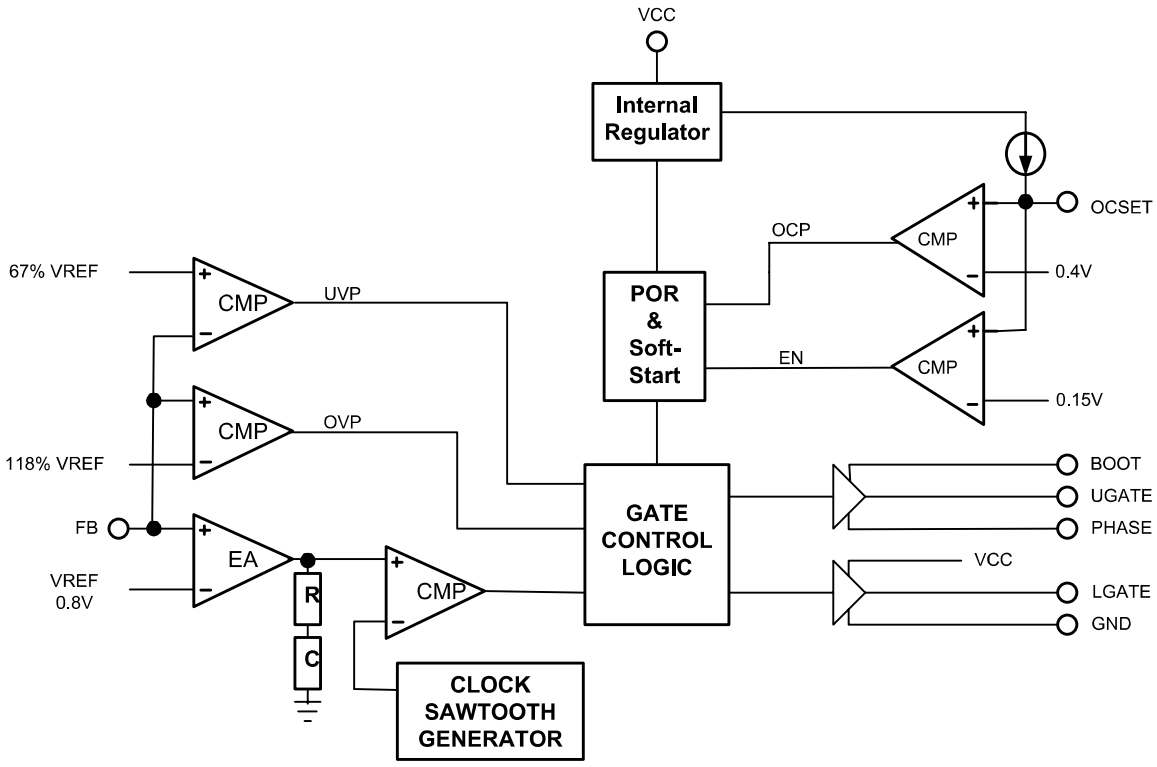
Ordering Information

Part Number	Package	Ship
CAT7581CA	SOP8 (Green)	2500/Tape & Reel

Pin Description

Pin	Symbol	Description
1	BOOT	This pin provides bias voltage to the upper MOSFET driver. A bootstrap circuit may used to generate BOOT voltage suitable to drive a standard N-channel MOSFET.
2	UGATE	Connect UGATE to the upper MOSFET gate. This pin provides the gate drive for upper MOSFET. It is also monitored by the adaptive shoot through protection function to determine when upper MOSFET has turned off.
3	GND	IC ground reference. All control circuits are referenced to this pin.
4	LGATE	Connect UGATE to the lower MOSFET gate. This pin provides the gate drive for lower MOSFET. It is also monitored by the adaptive shoot through protection function to determine when lower MOSFET has turned off.
5	VCC	Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 µF capacitor to GND. Ensure that this decoupling capacitor is placed near the IC.
6	FB	This pin is the inverting input to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage-control feedback loop. Connect this pin to the output resistor divider (if used) or directly to Vout.
7	OCSET	This pin has two functions. One is over current protection. Connecting a resistor (Rocset) between this pin and PHASE pins sets the over-current trip point. The other, pulling this pin to a level below 0.15V nominal disables the chip.
8	PHASE	Switch node pin. Connect this pin to the source of the top MOSFET. A Schottky diode between this pin and ground is recommended to reduce negative transient voltages which are common in a power supply system.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage, VCC 15V
Boot Voltage, V_{BOOT} ..... 15V wrt/PHASE
High Side Driver Output ..... 15V wrt/PHASE
Low Side Driver Output 15V
Feedback 5.5V
COMP 5.5V
ESD Classification (Note 2) ..... Class 2
Junction Temperature ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering 10s) ..... 260°C

Recommended Operating Conditions

Supply Voltage, VCC ..... +12V ±10%
Ambient Temperature Range ..... -30°C to 85°C

Thermal Resistance

	θ_{JA}	θ_{JC}	
SOP8 Package	91	43	(°C/W)

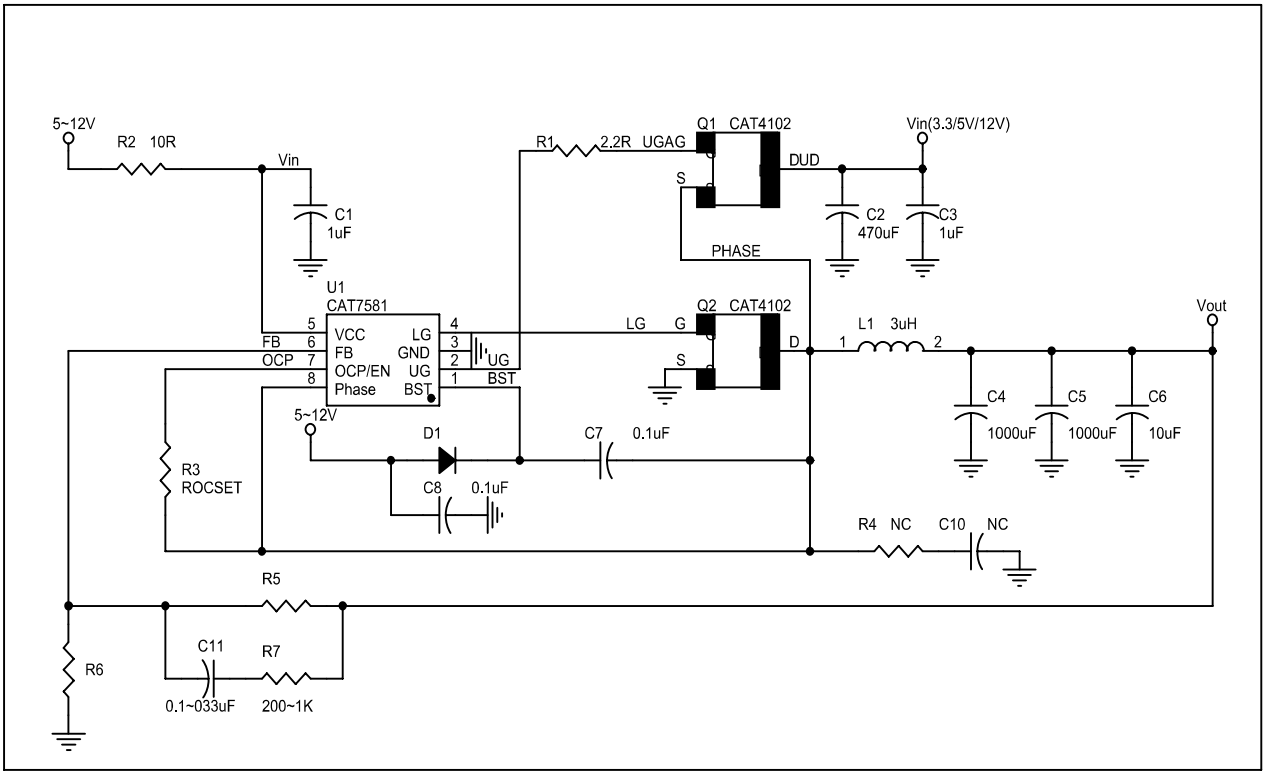
Electrical Characteristic:

(Recommended Operating Conditions, Unless Otherwise Noted; VCC = 12V; Temperature = 0 - 70 °C (typical = 25 °C))

Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage					
Input Voltage Range		4.5		13.2	V
Supply Current					
VCC Nominal Supply Current	Ugate & Lgate Open		2		mA
VCC Undervoltage Lockout					
UVLO Threshold	VCC rising Edge	3.85	4.2		V
UVLO Hysteresis			0.5		V
Switching Regulator					
Reference Voltage	TA = 0℃ to 70℃	0.784	0.800	0.816	V
Oscillator Frequency		250	300	350	KHz
Ramp-Amplitude Voltage			1.5		V
Minimum Duty Cycle			0		%
ERROR Amplifier					
Open Loop DC Gain			90		dB
Transconductance			7.5		μS
FB Bias Current	VFB=1V		0.1		μA
Gate Driver					
UGATE Sink (Note 3)	V_{BOOT}-V_{PHASE}=12V;V_{UGATE}-V_{PHASE} =1V		2.5	5	Ω
UGATE Source (Note 3)	V_{BOOT}-V_{PHASE}=12V;V_{UGATE}-V_{PHASE} =6V	0.8	1.4		A
LGATE Sink (Note 3)	Vcc=12V;V_{LGATE}=1V		1.4	3	Ω
LGATE Source (Note 3)	Vcc=12V;V_{LGATE}=6V	0.5	0.8		A
Internal Soft-Start					
Time	Switching frequency = 300 Khz		2048		cycle
VOUT Under voltage Protection					
UVP Level	Percent of Nominal	64	67	70	%
VOUT Over voltage Protection					
OVP Level	Percent of Nominal	115	118	121	%
Over Current Protection					
OC Current Source		35	40	45	μA
Disable					
OCSET Disable Threshold			0.15		V
OCSET Disable Hysteresis			40		mV

Note:
1. Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Devices are ESD sensitive. Handling precaution recommended.
3. Guaranteed by design; not production tested.

Typical Application:



* Note: The recommended applications shall be customer design-in orientation to fit each customers demand. Based on the nature of customers demand-oriented, please contact CAT or agent for design support service.

FUNCTION DESCRIPTION

OUTPUT REGULATION

The output voltage level setting is

$$V_{OUT} = 0.8V * (1 + \frac{R5}{R6})$$

INPUT VOLTAGE RANGE (VCC AND BOOT)

The input voltage range for both VCC and BOOT is 4.5 V to 13.2 V with respect to GND and PHASE, respectively. Although BOOT is rated at 13.2 V with respect to PHASE, it can also tolerate 26.5 V with respect to GND.

DISABLE CHIP BEHAVIOR

When the voltage level of OCSET pin is below 0.15V, the IC is disable. In this case, switching stops, the internal SS is discharged, and all GATE pins go low. The switch node enters a high impedance state and the output capacitors discharge through the load with no ringing on the output voltage.

INITIALIATION AND POR

The CAT7581 automatically initializes upon application of input power.

The POR function continually monitors the voltage at the VCC pin. When VCC reaches 4.2 V and the OCSET pin is not held below 0.15V, the POR function is enable.

There is 6.4ms delay after POR function enable to avoid V_{IN} (high side MOSFET drain terminal) comes up after VCC. Upon the delay completion, the POR function initiates the Soft Start operation.

INTERNAL SOFT−START

The CAT7581 features an internal Soft Start function, which reduces inrush current and overshoot of the output voltage. Soft start is achieved by ramping up the internal Soft Start voltage (V_{SS}) which is applied to the input of the error amplifier. This sequence begins once VCC surpasses its UVLO threshold. The typical Soft Start time is 6.4ms. The internal Soft Start voltage is held low when the part is in UVLO.

If the output (V_{OUT}) is pre-charged to a voltage less than the expected value, the CAT7581 will detect that condition, and will not turn on the high side or low side MOSFET until the Soft Start ramp voltages exceeds V_{OUT}; V_{OUT} will start ramping from here. If V_{OUT} is pre-charged to a voltage above the expected value, neither MOSFET will turn on until the end of the Soft Start, at which time it will try to pull the output voltage down to where it belongs.

If the VIN to the high side MOSFET drain is not from the same supply as VCC, and if it comes up after VCC and if the CAT7581 is not disabled until the VIN is present, there is 6.4ms delay then the Soft Start could go through its cycle, with no output voltage ramp. When the VIN finally turns on the output would basically follow the ramp of the VIN (at close to 100% duty cycle), from zero up to the final expected voltage. This might be acceptable, if the VIN ramp is slow enough (only the beginning of the ramp, from zero to VOUT matters here), compared to the amount of output capacitance to charge, and the inrush current that results. If this is not acceptable, then consider changing the sequencing of the power supplies, sharing the same supply, or adding sequencing logic to the OCSET pin to delay the Soft Start until the VIN supply is ready.

VCC UNDER VOLTAGE LOCKOUT

Under voltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when VCC is too low to support the internal rails and power the converter. For the CAT7581, the UVLO is set to ensure that the IC will start up when VCC reaches 4.2 V and shutdown when VCC drops below 3.7 V. This permits operation when converting from a 5.0 V input voltage.

VOUT UNDER VOLTAGE PROTECTION

The FB pin is monitored during converter operation by an Under-Voltage (UV) comparator. If the FB voltage drops below 67% of the reference voltage (0.8V), a fault signal is internally generated, and the fault logic shuts down the regulator.

VOUT OVER VOLTAGE PROTECTION

The FB pin is monitored during converter operation by an Over-Voltage (OV) comparator. If the FB voltage is 18% above reference voltage (0.8V), the chip is latched: the lower-side power MOS turns on and higher-side power MOS turns off.

OVER CURRENT PROTECTION

The OCP function protects the converter from a shorted output by using the lower MOSs on-resistance, $R_{DS(ON)}$ to monitor the current. This approach simplifies the implementation and improves efficiency by eliminating the need for a current sense resistor.

A resistor (R_{OCSET}) connected from the OCSET pin to the low side MOSFET's drain, programs the over current trip level. An internal 40uA (typical) current source flowing through the Rocset develops a voltage (V_{OCSET}) across the R_{OCSET}. When the V_{OCSET} is less than the internal over current reference voltage (0.4V, typical), the CAT7581 shuts off and then initiates a new Soft Start process. After 4 over current events are counted, CAT7581 turns off both high-side and low-side MOSFET and the converter's output is latched to be floating.

The V_{OCSET} sensing starts several hundreds nano-seconds after the edge of the internal PWM logic signal. This is done to allow the gate transition noise and ringing on the PHASE pin to settle out before monitoring. The monitoring ends when the PWM edge goes low.

If the regulator is running at high UGATE duty cycles (around 87% duty cycle), then the LGATE pulse width may not be wide enough for the OCP to properly sample the $R_{DS(ON)}$. For those cases, if the LGATE is too narrow (or not there at all) for 3 consecutive pulses, then the third pulse will be inserted and/or stretched to the approximately 400 ns minimum width. This at least allows for OCP monitoring every third pulse under this condition. This can introduce a small pulse-width error on the output voltage, which will be corrected on the next pulse; but the output ripple voltage will have an unusual 3-clock pattern, which may look like jitter. Note that if the OCP is disabled (by choosing a too-high value of R_{OCSET}, or no resistor at all), then the pulse stretching feature is also disabled. The OCP trip level formula is the following:

$$Iocset = \frac{40(uA) * R_{OCSET}(K\Omega) - 0.4(mV)}{R_{DS(ON)\_LOWSIDE}(m\Omega)}$$

The parasitic capacitance on the OCSET pin (including the capacitance inside the OCSET, external PCB trace capacitance, the capacitance of the MOSFETs, and the capacitance of the enable switch) must be minimized to avoid the RC delay effect to influence the OCP function.

DRIVERS

The CAT7581 includes 1.5 A gate drivers to switch external N−Channel MOSFETs. This allows the CAT7581 to address High−Power as well as Low−Power conversion requirements. The gate drivers also include adaptive non−overlap circuitry. The non−overlap circuitry increases efficiency, which minimizes power dissipation, by minimizing the body diode conduction time.

Careful selection and layout of external components is required, to realize the full benefit of the onboard drivers. The capacitors between VCC and GND and between BOOT and PHASE must be placed as close as possible to the IC. The current paths for the UGATE and LGATE connections must be optimized. A ground plane should be placed on the closest layer for return currents to GND in order to reduce loop area and inductance in the gate drive circuit.

INPUT CAPACITOR SELECTION

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$I_{IN(RMS)} = I_{OUT}\sqrt{D*(1-D)}$$

where D is the duty cycle, $I_{IN(RMS)}$ is the input RMS current, and I_{OUT} is the load current. The equation reaches its maximum value with D = 0.5. Losses in the input capacitors can be calculated with the following equation:

$$P_{CIN} = ESR_{CIN} * I_{IN(RMS)}^{2}$$

where P_{CIN} is the power loss in the input capacitors and ESR_{CIN} is the effective series resistance of the input capacitance. Due to large $\frac{di}{dt}$ through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must be surge protected. Otherwise, capacitor failure could occur.

CALCULATING INPUT STARTUP CURRENT

To calculate the input startup current, the following equation can be used.

$$I_{INRUSH} = \frac{C_{OUT} * V_{OUT}}{t_{SS}}$$

where I_{INRUSH} is the input current during startup, C_{OUT} is the total output capacitance, V_{OUT} is the desired output voltage, and t_{SS} is the internal soft−start interval. If the inrush current is higher than the steady state input current during max load, then the input fuse should be rated accordingly, if one is used.

OUTPUT INDUCTOR SELECTION

The output inductor is selected to meet the output voltage ripple requirements and affects the load transient response. Higher inductance reduces the inductor's ripple current and induces lower output ripple voltage. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_S * L} * \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V_{OUT} = \Delta I * ESR$$

Although increase the inductance reduce the ripple current and voltage, but the large inductance reduces the regulator's response time to load transient. Increasing the switching frequency (Fs) for a given inductor also reduces the ripple current and voltage but it will increase the switching loss of the power MOS.

To select the inductor value, a guideline is to choose the ripple current (ΔI) to be approximately

10%~50% of the maximum output current. Once the inductor value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. It is also important to have the inductance tolerance specified to keep the accuracy of the system controlled. Using 20% for the inductance (at room temperature) are reasonable tolerances that most manufacturers can meet. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

OUTPUT CAPACITORS SELECTION

An output capacitor is required to filter the output and supply the load transient current. Higher Capacitor value and lower ESR reduce the output ripple and the load transient drop. These requirements are met with a mix of capacitors and careful layout.

In typical switching regulator design, the ESR of the output capacitor bank dominates the transient response. The number of output capacitors can be determined by using the following equations:

$$ESR_{MAX} = \frac{\Delta V_{ESR}}{\Delta I_{OUT}}$$

$$Number\_of\_Capacitors = \frac{ESR_{CAP}}{ESR_{MAX}}$$

$\triangle V_{ESR}$ = change in output voltage due to ESR (assigned by the designer).

$\triangle I_{OUT}$ = load transient.

ESR_{CAP} = maximum ESR per capacitor (specified in manufacturer's data sheet).

ESR_{MAX} = maximum allowable ESR.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Consult the capacitors manufacturer to make sure the decoupling requirements.

THERMAL CONSIDERATIONS

The power dissipation of the CAT7581 varies with the MOSFETs used, VCC, and the boost voltage (V_{BOOT}). The average MOSFET gate current typically dominates the control IC power dissipation. The IC power dissipation is determined by the formula:

$$P_{IC} = (I_{CC} * VCC) + P_{UGATE} + P_{LGATE}$$

Where:

P_{IC} = Control IC power dissipation,

I_{CC} = IC measured supply current,

VCC = IC supply voltage,

P_{UGATE} = Top gate driver losses,

P_{LGATE} = Bottom gate driver losses.

The high side (switching) MOSFET gate driver losses are:

$$P_{UGATE} = Q_{UGATE} * F_{SW} * V_{BOOT}$$

Where:

Q_{UGATE} = Total upper MOSFET gate charge at V_{BOOT}.

F_{SW} = The switching frequency,

V_{BOOT} = The BOOT pin voltage.

The lower (synchronous) MOSFET gate driver losses are:

$$P_{LGATE} = Q_{LGATE} * F_{SW} * V_{CC}$$

Where:

Q_{LGATE} = total lower MOSFET gate charge at VCC.

The junction temperature of the control IC can then be calculated as:

$$T_J = T_A + P_{IC} + \theta_{JA}$$

Where:

T_J = The junction temperature of the IC,

T_A = The ambient temperature,

θ_{JA} = The junction−to−ambient thermal resistance of the IC package.

The package thermal resistance ($R_{\theta_{JA}}$) can be obtained from the specifications section of this data

sheet and a calculation can be made to determine the IC junction temperature. In addition, a thermal resistance (Junction – to – Ambient / Safe Operating Area) curve has been included below to further aid design. However, it should be noted that the physical layout of the board, the proximity of other heat sources such as MOSFETs and inductors, and the amount of metal connected to the IC, impact the temperature of the device. Use these calculations as a guide, but measurements should be taken in the actual application.

POWER MOS SELECTION

CAT7581 requires 2 N-channel POWER MOSs for each PWM output. These should be selected base on $R_{DS(ON)}$, gate supply voltage, gate charge (capacitance) and thermal management requirements. In general, the upper power MOS should be chosen to minimize the gate charge, since switching loses dominate. Since the lower power MOS is on most of the time, low $R_{DS(ON)}$ should be the main consideration.

It can be advantageous to use multiple POWER MOSs to reduce power consumption. By placing a number of MOSs in parallel, the effective $R_{DS(ON)}$ is reduced, thus reducing the Ohmic power loss. However, placing MOSs in parallel increases the gate capacitance so that switching losses increase. As long as adding another parallel MOS reduces the Ohmic power loss more than the switching losses increase, there is some advantage to doing so.

The following equations can be used to calculate power dissipation in the power MOSs

$$P_{UPPER} = Io^2 * R_{DS(ON)} * D + \frac{1}{2} I_O * V_{IN} * t_{SW} * F_S$$

$$P_{LOWER} = Io^2 * R_{DS(ON)} * (1 - D)$$

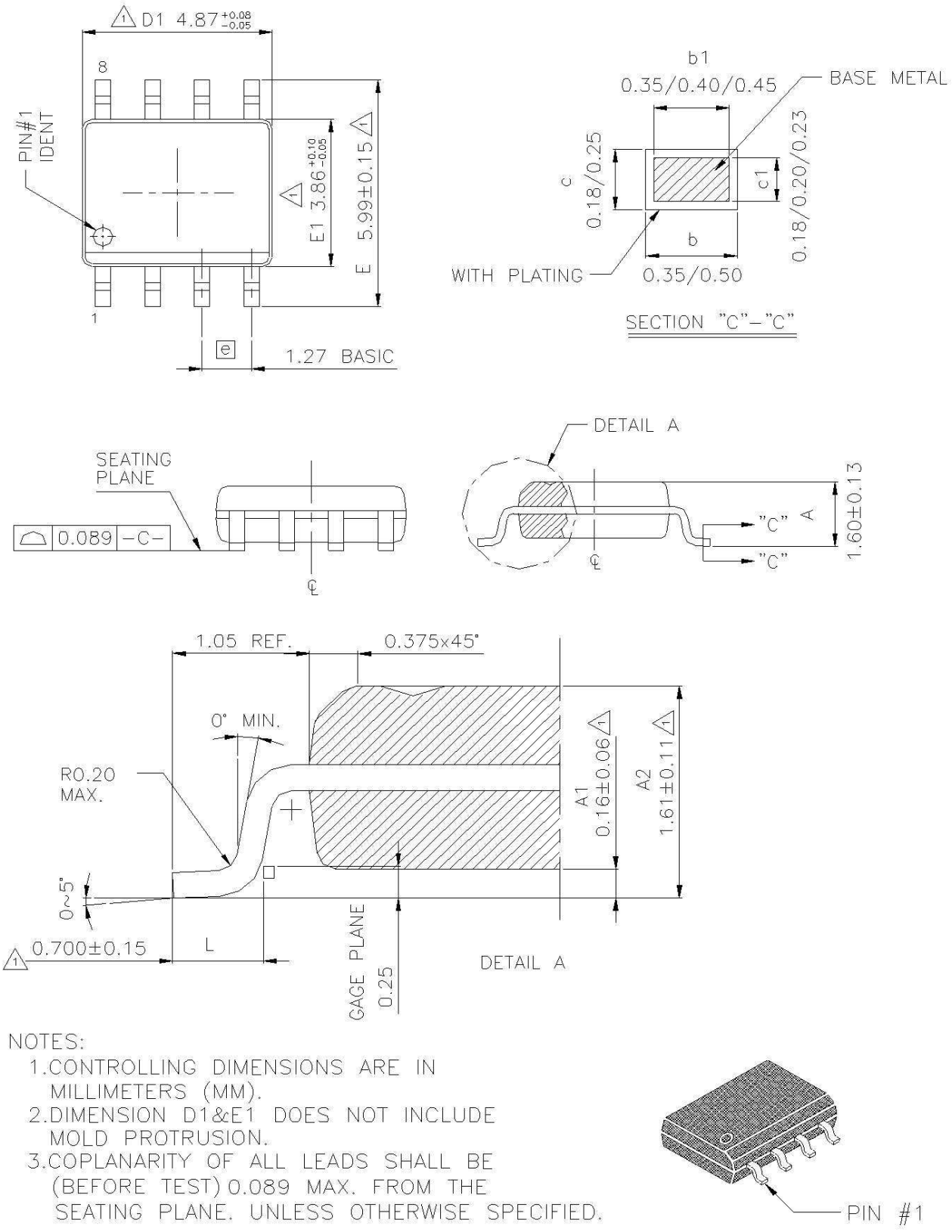
Where,

D is the duty cycle = $\frac{V_{OUT}}{V_{IN}}$.

t_{SW} is the switching interval.

Fs is the switching frequency.

Package Dimensions



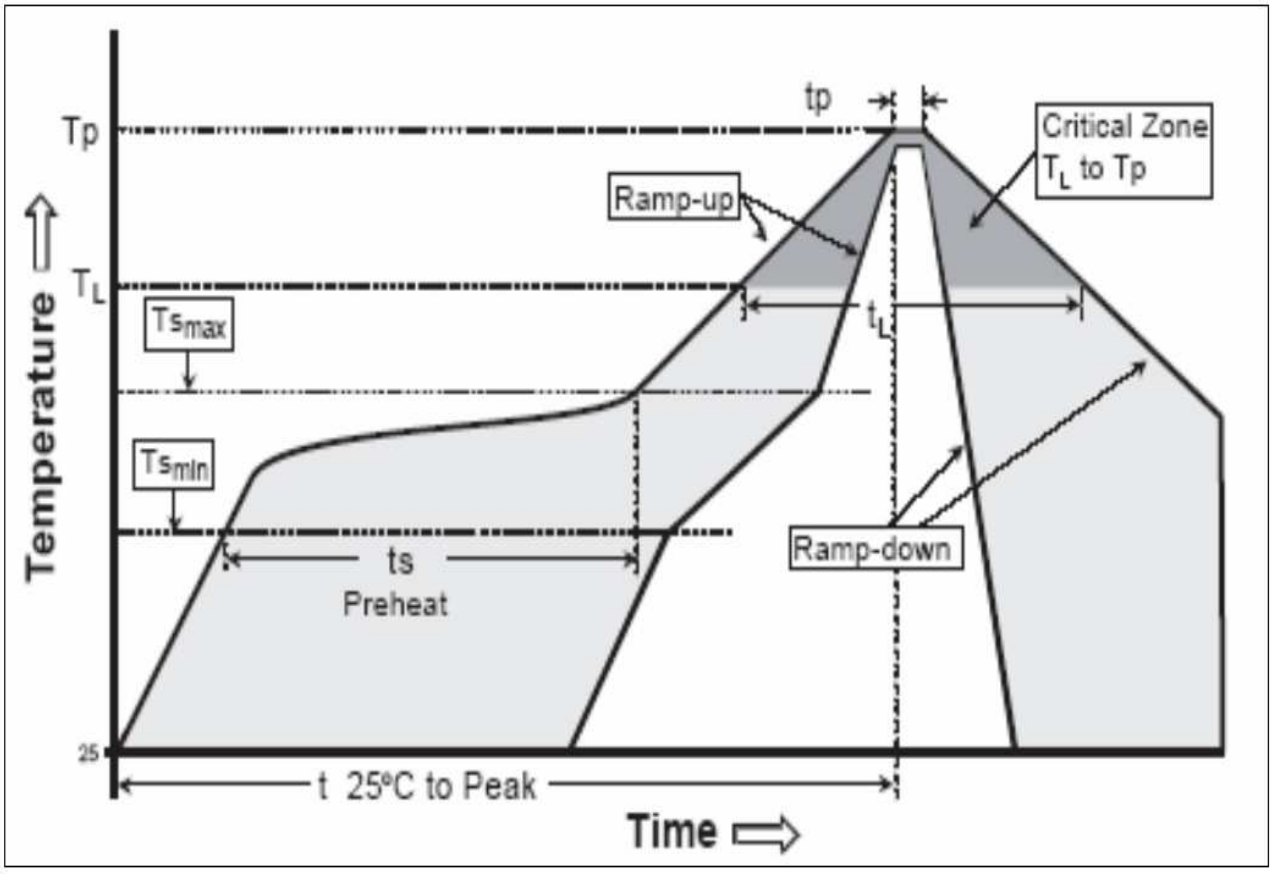
NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (MM).
2. DIMENSION D1&E1 DOES NOT INCLUDE MOLD PROTRUSION.
3. COPLANARITY OF ALL LEADS SHALL BE (BEFORE TEST) 0.089 MAX. FROM THE SEATING PLANE. UNLESS OTHERWISE SPECIFIED.

Classification Reflow Profiles

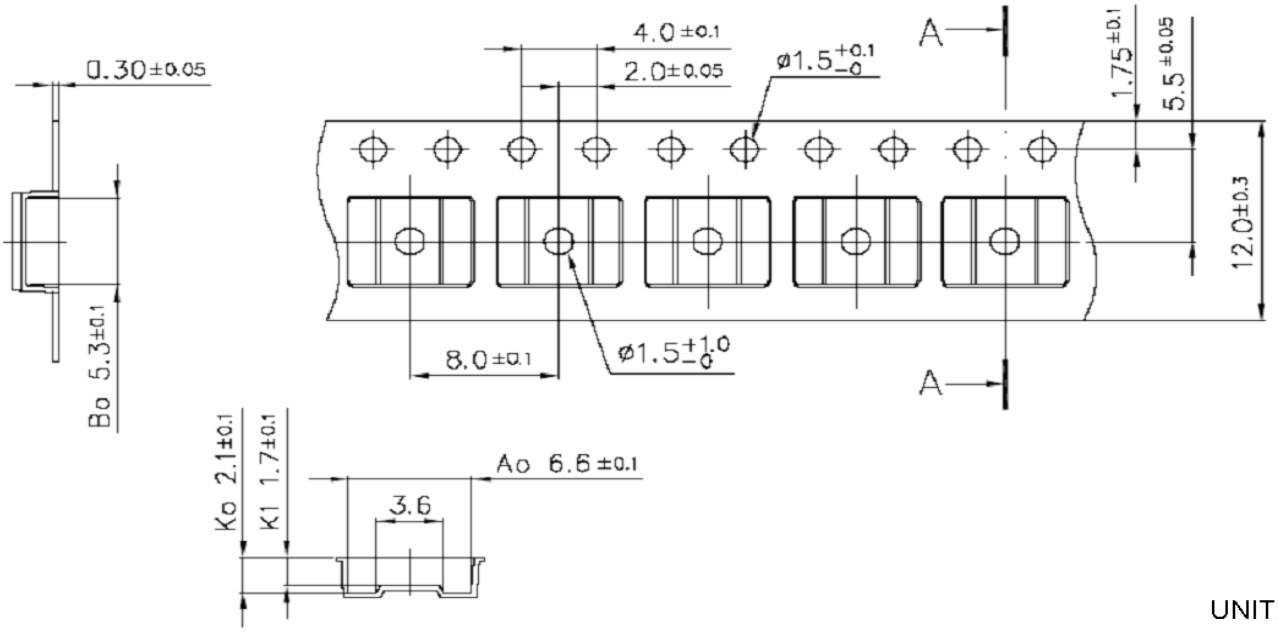
Reflow Profile	Green Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3℃/second max.
Preheat -Temperature Min(Ts_{min}) -Temperature Max(Ts_{max}) -Time(ts_{min} to ts ts_{max})	 150℃ 200℃ 60-180 seconds
Time maintained above: -Temperature(T_L) -Time(t_L)	 217℃ 60-150 seconds
Peak Temperature(Tp)	260 +0/-5 ℃
Time within 5 ℃ of actual Peak Temperature(tp)	20-40 seconds
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

Note: All Temperature refer to topside of the package, measured on the package body surface.



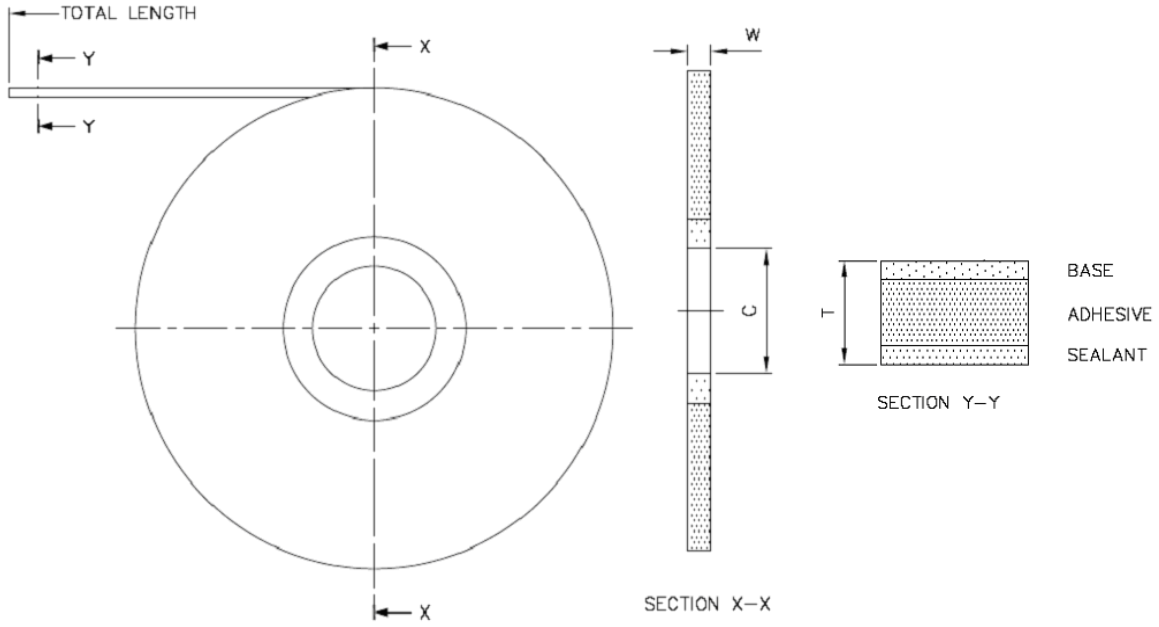
Carrier Tape & Reel Dimensions

Carrier Tape



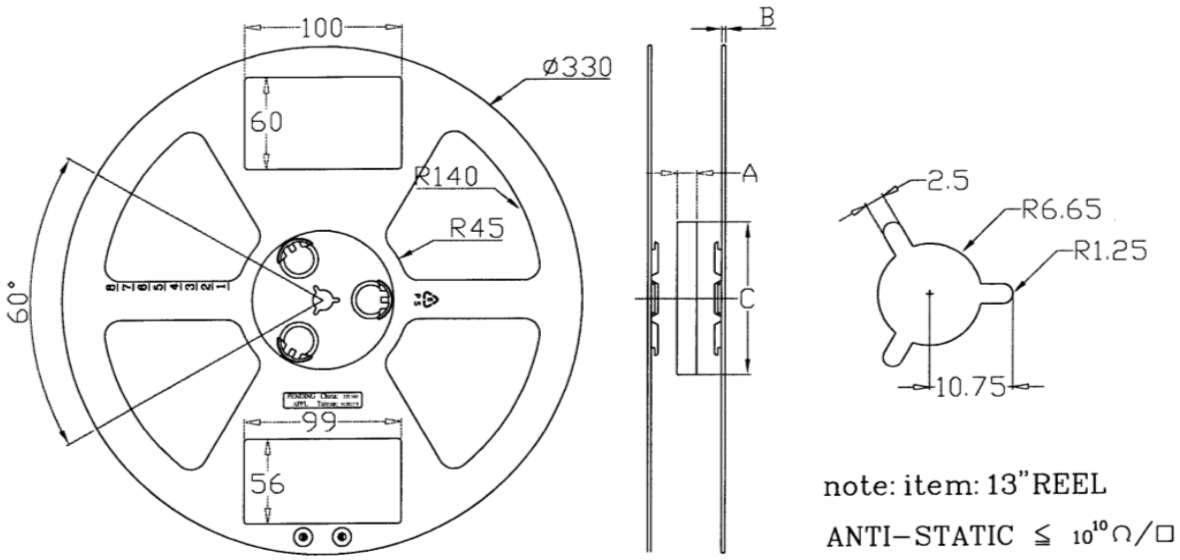
UNIT: mm.

Cover Tape



CARRIER TAPE WIDTH	C NOMINAL	T	W	TOTAL LENGTH
12mm	76.2mm	0.06±0.01mm	9.3±0.1mm	300M

Reel Outline



note: item: 13"REEL

ANTI-STATIC ≦ $10^{10}\Omega/\square$

material: P.S

SPEC	12	16	24	32	44	56	72
DIM A $^{+1.5}_{-0.5}$	12.5	16.5	24.5	32.5	44.5	57	73
DIM B ±0.2	2.3	2.3	2.3	2.3	2.3	2.3	2.3
DIM C ±1.5	99	99	99	99	99	99	99

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