

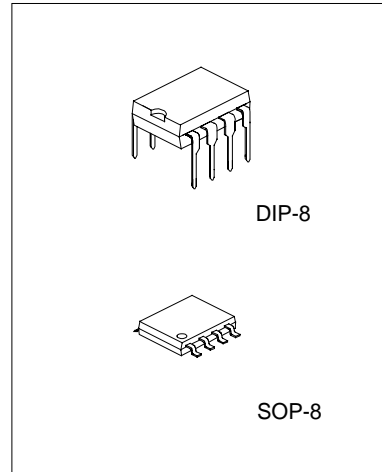
DUAL OPERATIONAL AMPLIFIER

DESCRIPTION

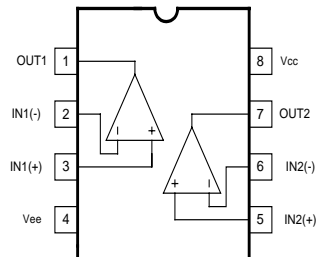
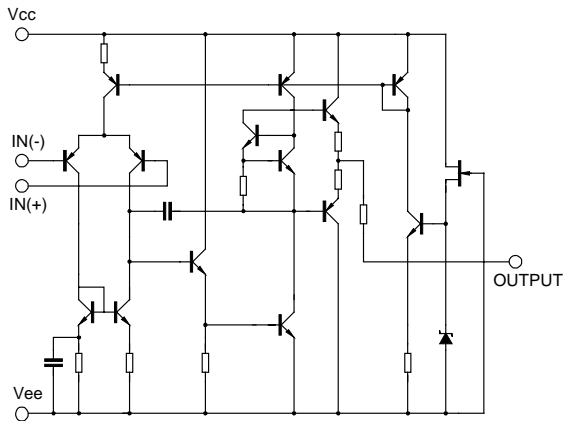
The UTC4558 is a monolithic integrated circuit designed for dual operational amplifier.

FEATURES

- *No frequency compensation required.
- *No latch-up
- *Large common mode and differential voltage range
- *Parameter tracking over temperature range
- *Gain and phase match between amplifiers
- *Internally frequency compensated
- *Low noise input transistors



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V _{CC}	±22	V
Differential input voltage	V _{I(DIFF)}	±18	V
Power Dissipation	P _D	400	mW
Input Voltage	V _I	±15	V
Operating Temperature	T _{OPR}	0~+70	°C
Storage Temperature	T _{STG}	-65~+150	°C

ELECTRICAL CHARACTERISTICS(Ta=25°C ,Vcc=15V,Vee=-15V)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Supply Current	I _{cc}			3.5	5.6	mA
Input offset voltage	V _{IO}	R _s <10kΩ		2	6	mV
Input offset current	I _{IO}			5	200	nA
Input bias current	I _{BIAS}			30	500	nA
Large signal voltage gain	G _v	V _o (p-p)=10V,R _L <2kΩ	20	200		V/mV
Common Mode Input Voltage Range	V _{I(R)}		±12	±13		V
Common Mode Rejection Ratio	CMRR	R _s <10kΩ	70	90		dB
Supply Voltage Rejection Ratio	PSRR	R _s <10kΩ	76	90		dB
Output Voltage swing	V _o (p-p)	R _L >10kΩ		±12	±14	V
Power Consumption	P _c			70	170	mV
Slew Rate	SR	V _i =10V,R _L >2kΩ,C _L <100pF	1.2			V/μs
Rise Time	T _{RIS}	V _i =20mV,R _L >2kΩ,C _L <100pF		0.3		μs
Overshoot	OS	V _i =20mV,R _L >2kΩ,C _L <100pF		15		%

TYPICAL PERFORMANCE CHARACTERISTICS

Fig.1 Positive output voltage swing vs Load resistance

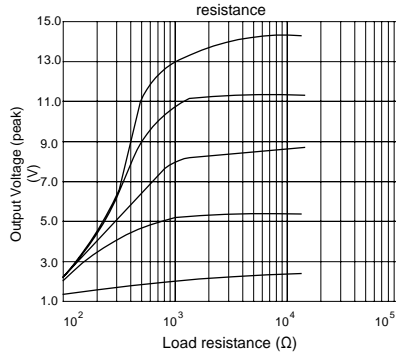


Fig.2 Positive output voltage swing vs Load resistance

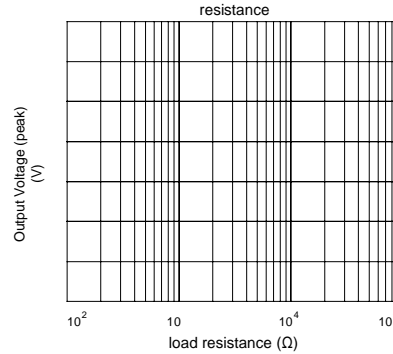


Fig.3 Power bandwidth (large signal swing vs frequency)

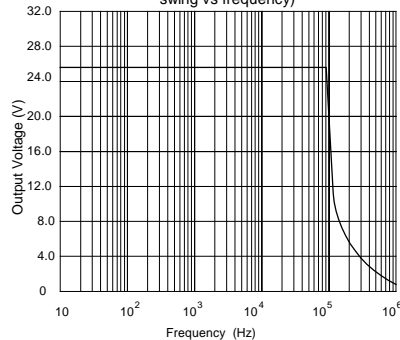


Fig. 4 Burst Noise vs Rs

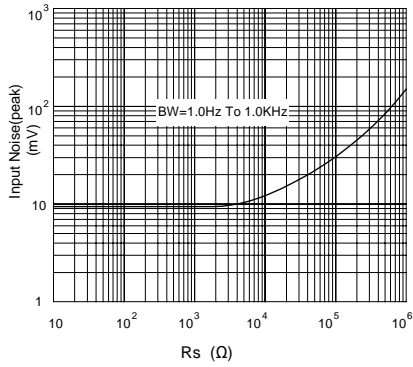


Fig. 5 RMS Noise vs Rs

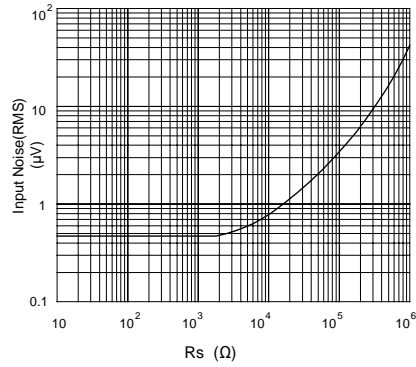


Fig. 6 Output Noise vs Rs

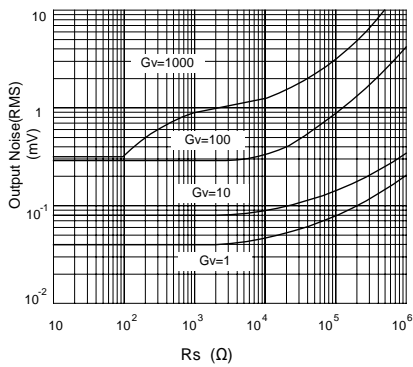


Fig. 7 Spectral Noise Density

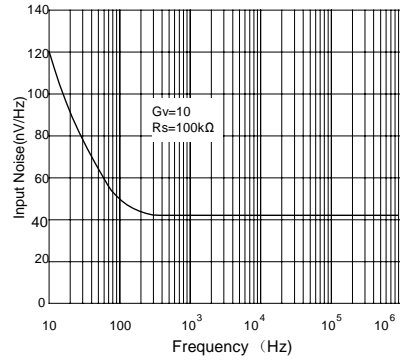


Fig. 8 Open loop frequency response

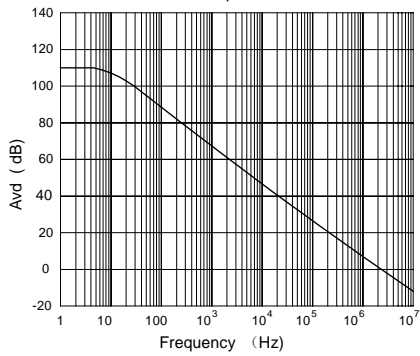
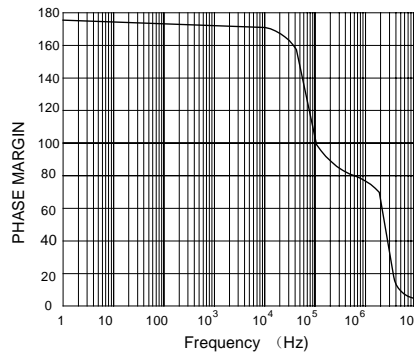
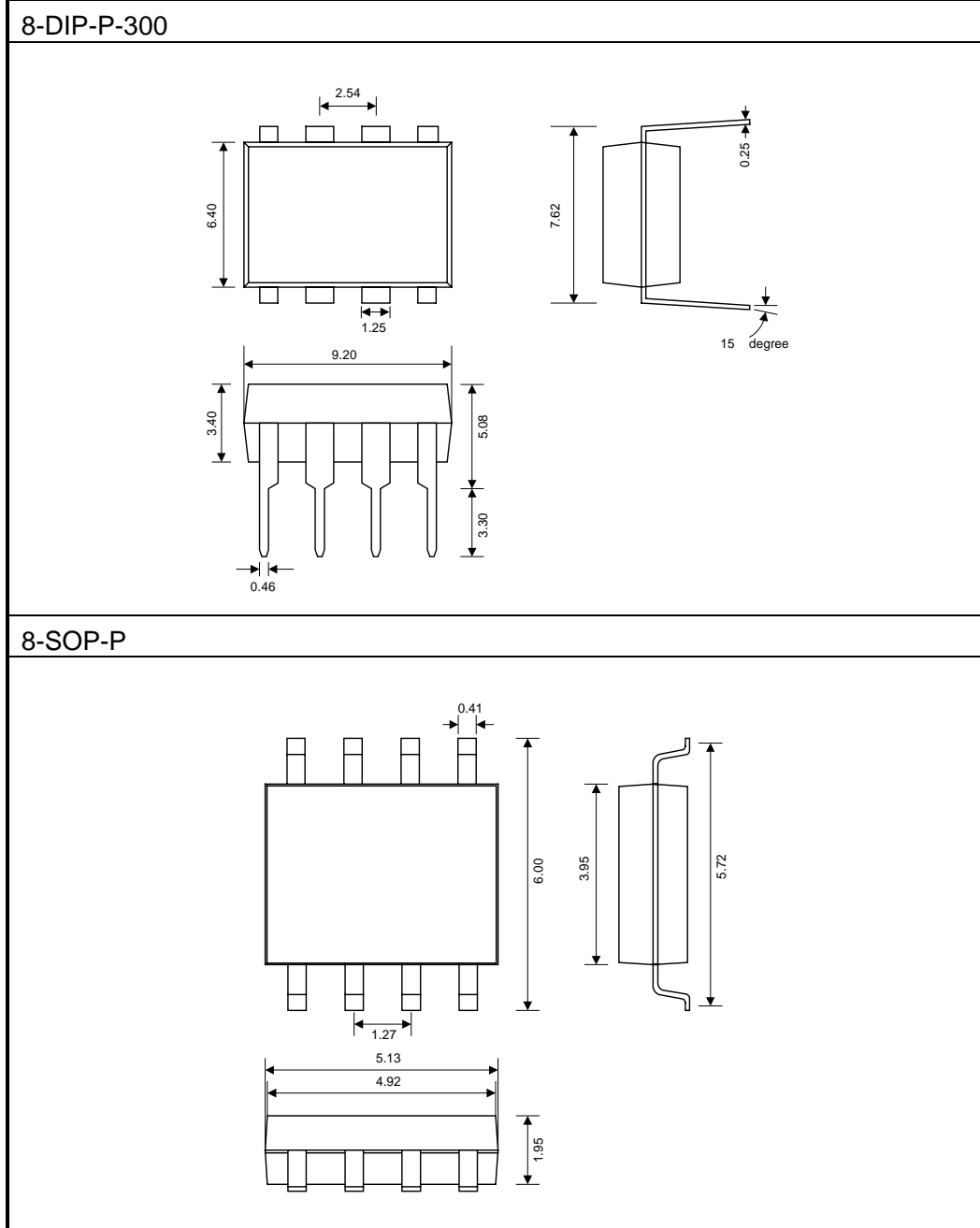


Fig. 9 PHASE MARGIN vs FREQUENCY



PACKAGE DIMENSIONS



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