

GENERAL DESCRIPTION

The OB3340 is a high power factor and high constant current precision LED driver for LED lighting applications. An analog multiplier for power factor correction (PFC), zero current detector (ZCD) to ensure TM operation and a feedback circuit to achieve constant LED current, a current sensing comparator with built-in leading-edge blanking ensures safe operation during short-circuit at the output, and a totem pole output ideally suited for driving a power MOSFET. OB3340 provides comprehensive protection features including system VCC under voltage lockout (UVLO), Output short/open protection, Cycle by cycle current limiting, and gate drive output clamping for external power MOSFET protection.

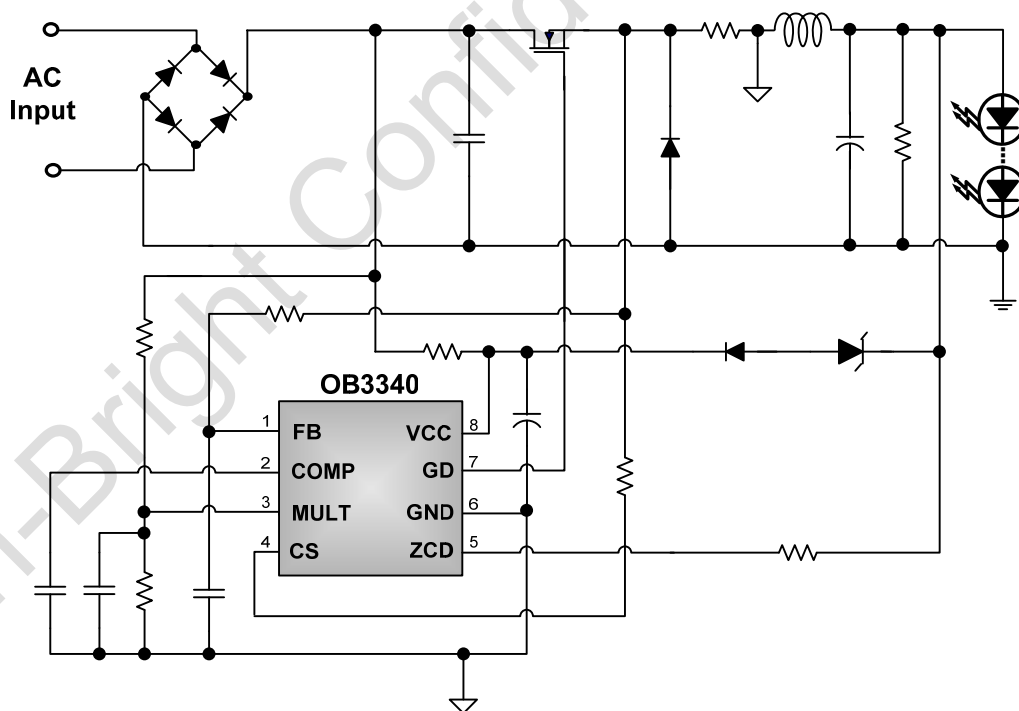
FEATURES

- High Precision Constant Output Current
- Analog multiplier for High Power Factor Correction
- Low Start-up Current and Operating Current
- Internal Startup Timer for Stand-alone Applications
- Transition Mode (TM) Operation
- Internal Leading Edge Blanking
- Cycle-by-Cycle Current Limiting
- Totem Pole Output with High State Clamping
- Under Voltage Lockout with Hysteresis
- VCC over voltage protection
- Output short/open protection
- Audio Noise Free
- 11V to 32V wide range of VCC voltage

APPLICATIONS

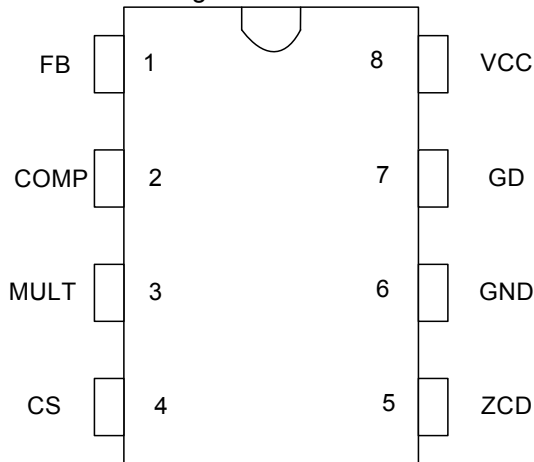
- LED Lighting Power

TYPICAL APPLICATION



GENERAL INFORMATION

Terminal Assignment
In SOP8 Package.



Ordering Information

Part Number	Description
OB3340CP	8 Pin SOP, Pb-free in Tube
OB3340CPA	8 Pin SOP, Pb-free in T&R

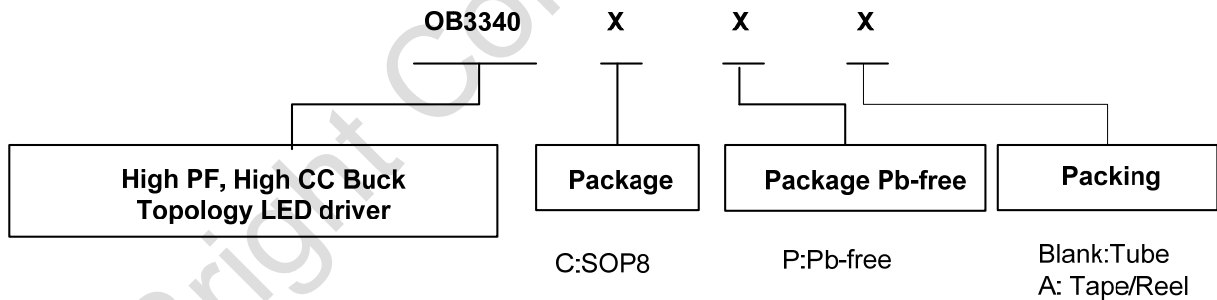
Package Dissipation Rating

Package	R θ JA (°C/W)
SOP8	150

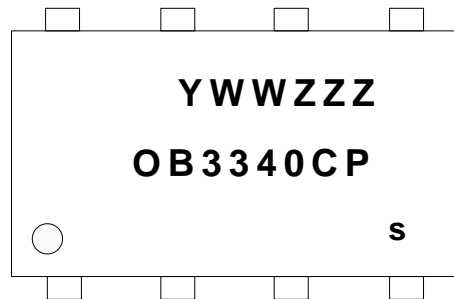
Absolute Maximum Ratings

Symbol	Parameter	Value
VCC	DC Supply voltage	Vz
I_ZCD	Zero Current Detector Max. Current	50mA(source) -10mA(sink)
CS FB COMP MULT	Analog inputs & outputs	-0.3 to 7V
Tj	Min/Max Operating Junction Temperature	-40 to 150 °C
Tstg	Min/Max Storage Temperature	-55 to 150 °C
Lead Temperature	(Soldering, 10secs)	260 °C

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



Marking Information

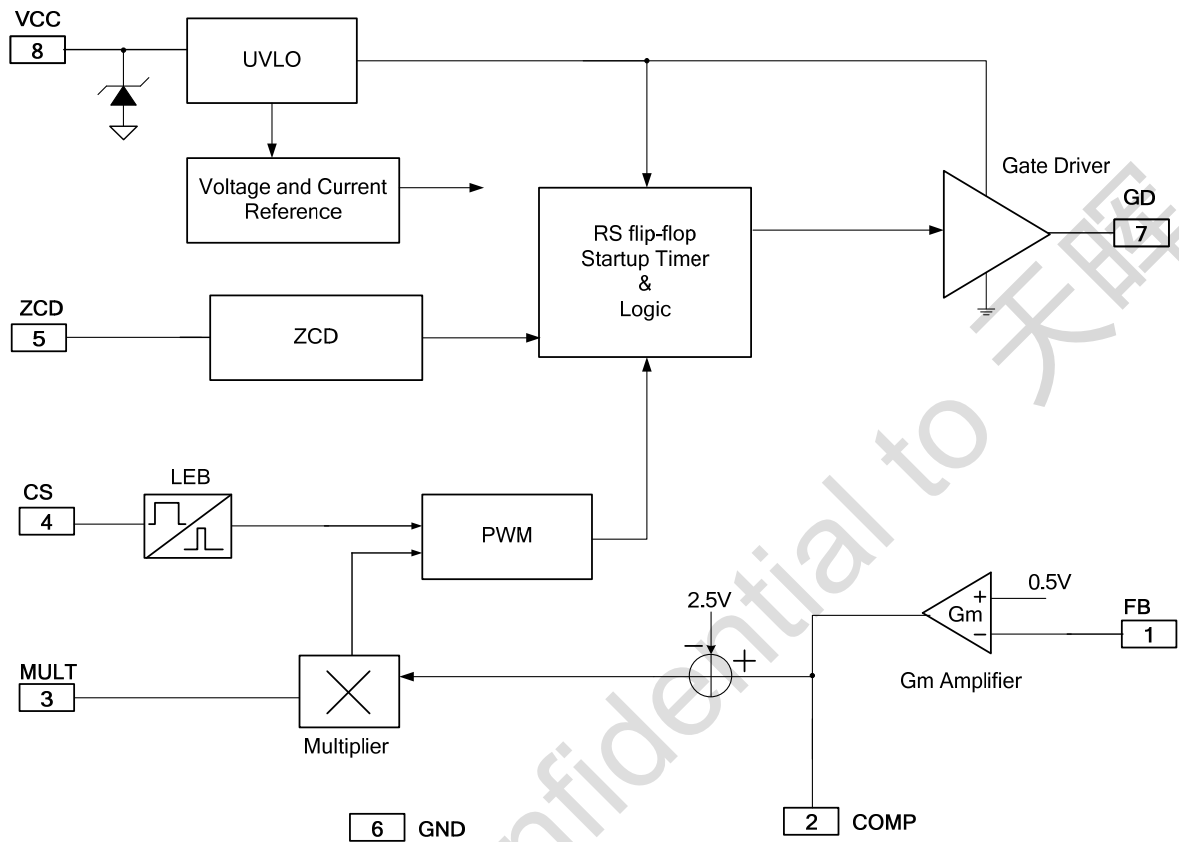


Y: Year Code
 WW: Week Code (01-52)
 ZZZ: Lot Code
 C: SOP8
 P:Pb-free
 s: internal code

TERMINAL DESCRIPTIONS

Pin Num	Pin Name	I/O	Description
1	FB	I	Input of error amplifier.
2	COMP	O	Output of error amplifier. A compensation network is placed between COMP and the GND pin. The voltage between COMP and GND pin generate PWM duty cycle.
3	MULT	I	Input of multiplier. Connected to line voltage after bridge diodes via a resistor divider to provide sinusoidal reference voltage to the current loop.
4	CS	I	Current sense input pin. Connected to MOSFET current sensing node.
5	ZCD	I	Zero Current Detection input. When activated, A new switching cycle starts.
6	GND	P	Ground pin
7	GD	O	Gate driver output. Drive power MOSFET.
8	VCC	P	DC supply voltage.

BLOCK DIAGRAM

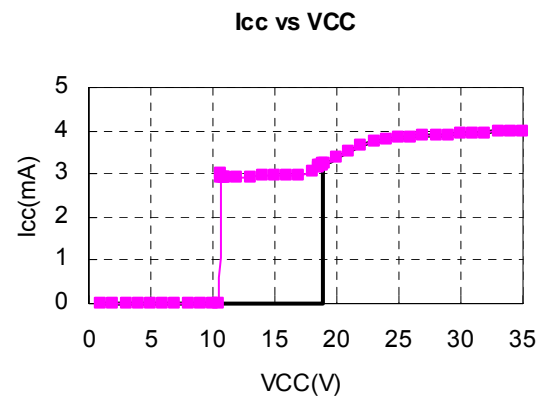
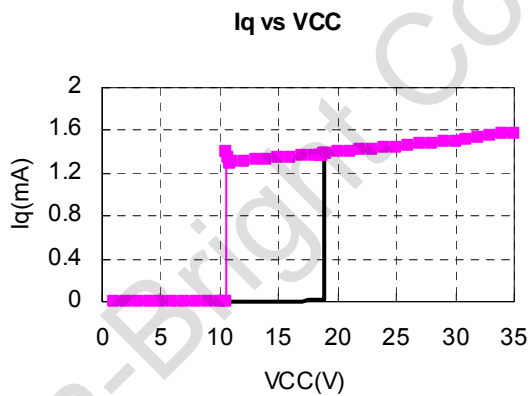
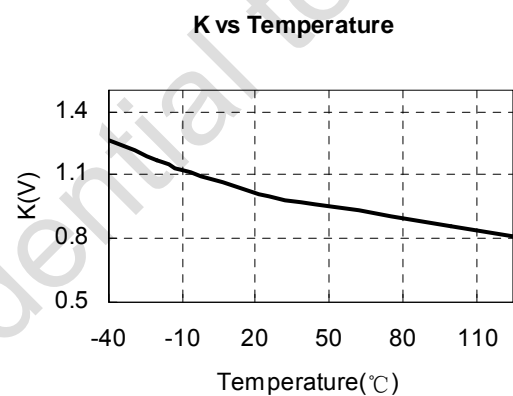
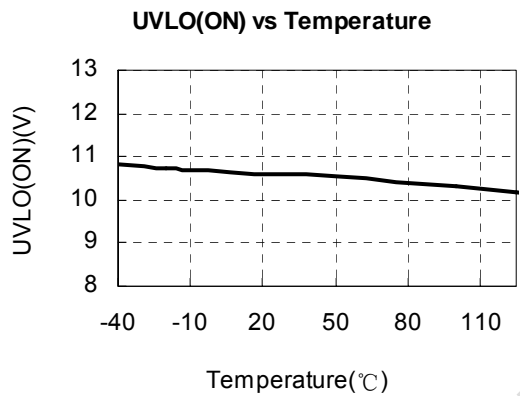
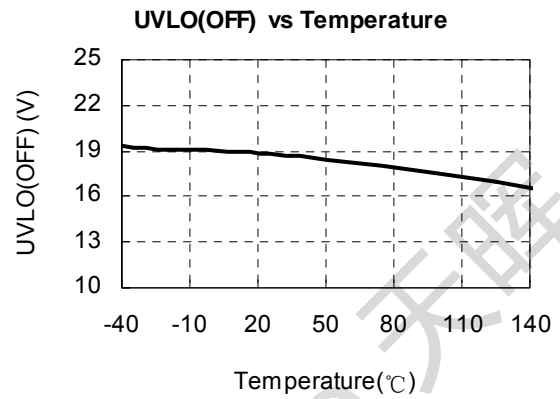
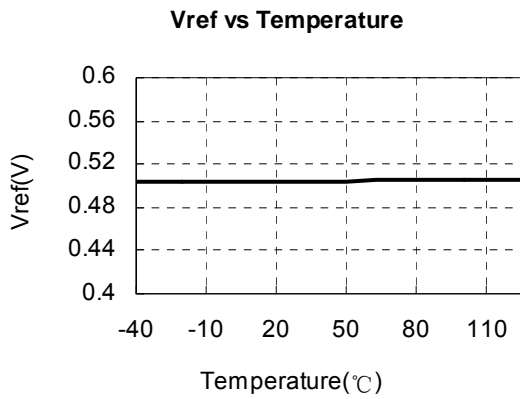


ELECTRICAL CHARACTERISTICS

(T_A = 25°C if not otherwise noted)

Symbol	Pin	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE SECTION							
V _{cc}	8	Operating Range	After Turn On	11		32	V
UVLO(OFF)	8	VCC under voltage lockout exit		17.5	19.0	20.5	V
UVLO(ON)	8	VCC under voltage lockout enter		8.8	10.0	11.2	V
Hys	8	Hysteresis			9.0		V
V _z	8	VCC Zener Clamp Voltage	I _{cc} =5mA		38		V
V _{cc_ovp}	8	VCC OVP threshold			36.5		V
SUPPLY CURRENT SECTION							
I _{cc-start}	8	Start-up Current	V _{cc} =11V		5	15	uA
I _q	8	Quiescent Current, No Switching	V _{cc} =14.5V		1.5	2.5	mA
I _{cc}	8	Operating Supply Current	GD=1nF @ 70kHz		3.2	6	mA
ERROR AMPLIFIER SECTION							
VREF	1	EA Reference	V _{cc} =14.5V	0.49	0.5	0.51	V
G _m		EA transconductance		40	60	80	uS
I _{COMP}	2	Source Current	COMP=3.5V, FB=0.4V		-6		uA
		Sink Current	COMP=3.5V, FB=0.6V		6		uA
V _{COMP}	2	Upper Clamp Voltage	FB=0.4V, Comp floating		5.5		V
		Lower Clamp Voltage	I _{sink} =0.2mA		2.35		V
MULTIPLIER SECTION							
V _{mult}	3	Linear Operating Range	COMP=3.0V	0 to 3.8			V
K		Gain	V _{mult} =1V, COMP=3.5V		0.95		1/V
CURRENT SENSE COMPARATOR							
V _{cs}	4	Current Sense Reference Clamp	V _{mult} =2.5V, COMP=5V	2.35	2.5	2.65	V
T _{d(H-L)}	4	Delay to Output			200	450	ns
ZERO CURRENT DETECTOR							
V _{zcd}	5	Input Threshold Voltage Trigger level			0.25		V
V _{zcd_hys}		ZCD trigger Hysteresis			0.75		V
V _{zcd}	5	Upper Clamp Voltage	I _{zcd} =2.5mA	5.1	5.7	6.3	V
V _{zcd}	5	Lower Clamp Voltage	I _{zcd} =-2.5mA		0		V
I _{zcd}	5	Source Current Capability		-3		-5	mA
I _{zcd}	5	Sink Current Capability		3		10	mA
TIMER							
T _{start}		Re-Start Timer Period		38	55	72	us
T _{on_max}		Maximum Ton		30	46	68	us
GATE DRIVE SECTION							
V _{oL}	7	Low Output Voltage	V _{cc} =14.5V, I _o =100mA			1.5	V
V _{oH}	7	High Output Voltage	V _{cc} =14.5V, I _o =100mA	8			V
T _r	7	Rising Time	CI=1000pF, 10~90%		80	150	ns
T _f	7	Falling Time	CI=1000pF, 10~90%		30	70	ns
V _{oclamp}	7	Output Clamp Voltage	V _{cc} =28V		15	17	V

CHARACTERIZATION PLOTS



OPERATIONAL DESCRIPTION

The OB3340 is a high power factor and high constant current precision LED driver for LED lighting applications. The transition mode control greatly reduces the switch turn-on loss, improves the conversion efficiency and provides very good power factor correction.

- **Startup Current and Start up Control**

The typical startup current of OB3340 is 5uA when the VCC pin is lower than the UVLO threshold so that VCC could be charged up and starts up the device. A high value, low wattage startup resistor can therefore be used to minimize the power loss during the normal operation.

- **PWM Modulator**

OB3340 employs peak current control with power factor correction. The PWM stage compares the COMP signal (EA output) with CS pin voltage to generate PWM duty cycle. A new PWM cycle is always triggered by the Zero Current Detection (ZCD) block, and exits whenever the CS voltage exceeds COMP voltage.

- **Gm Amplifier**

The inverting input of the Gm Amplifier (E/A) is compared to an internal reference voltage (0.5V) to determine COMP voltage. An external loop compensation network is placed between COMP and GND. COMP is subtracted by 2.5V and then is internally connected to the multiplier input, as shown in figure 1.

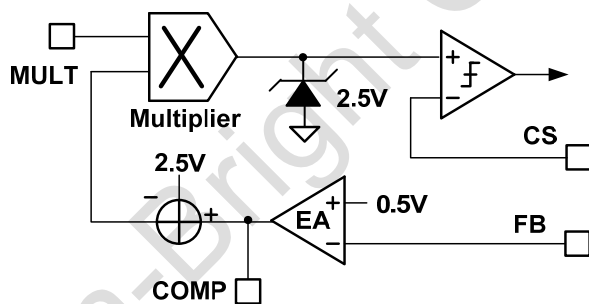


Fig.1

- **Analog Multiplier for Power Factor Correction**

The built-in analog multiplier output limits the MOSFET peak current with respect to the AC half wave rectified input voltage. Through controlling the CS comparator threshold as the AC line voltage traverses sinusoidally from zero to peak line voltage, the load appears to be resistive to the AC line and near to unity power factor can be achieved. In OB3340, the two inputs for the multiplier are designed to achieve good linearity

over a wide dynamic range to represent an AC line free from distortion. Special efforts have been made to assure universal line applications with respect to a 90 to 264VAC range. The multiplier output is internally clamped to 2.5V, as shown in Fig.1.

- **Current Sensing Comparator and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in OB3340. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to demagnetize diode reverse recovery. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and COMP pin voltage.

- **Zero Current Detection**

OB3340 performs zero current detection (ZCD) by monitoring the voltage activity on the output voltage through ZCD pin in series with an external resistor. When the stored energy of the buck inductor is fully released to the output, the voltage at ZCD pin decreases. When ZCD pin voltage falls below 0.25V, an internal ZCD comparator is triggered and a new PWM switching cycle is initiated following the ZCD triggering. If no zero current triggering signal is detected on ZCD pin, the "Startup Timer" block in OB3340 will generate a restart signal in 55usec (typ.) after the last PWM signal. The maximum and minimum voltage of ZCD pin is internally clamped to 5.8V and 0V respectively.

- **Gate Drive Output**

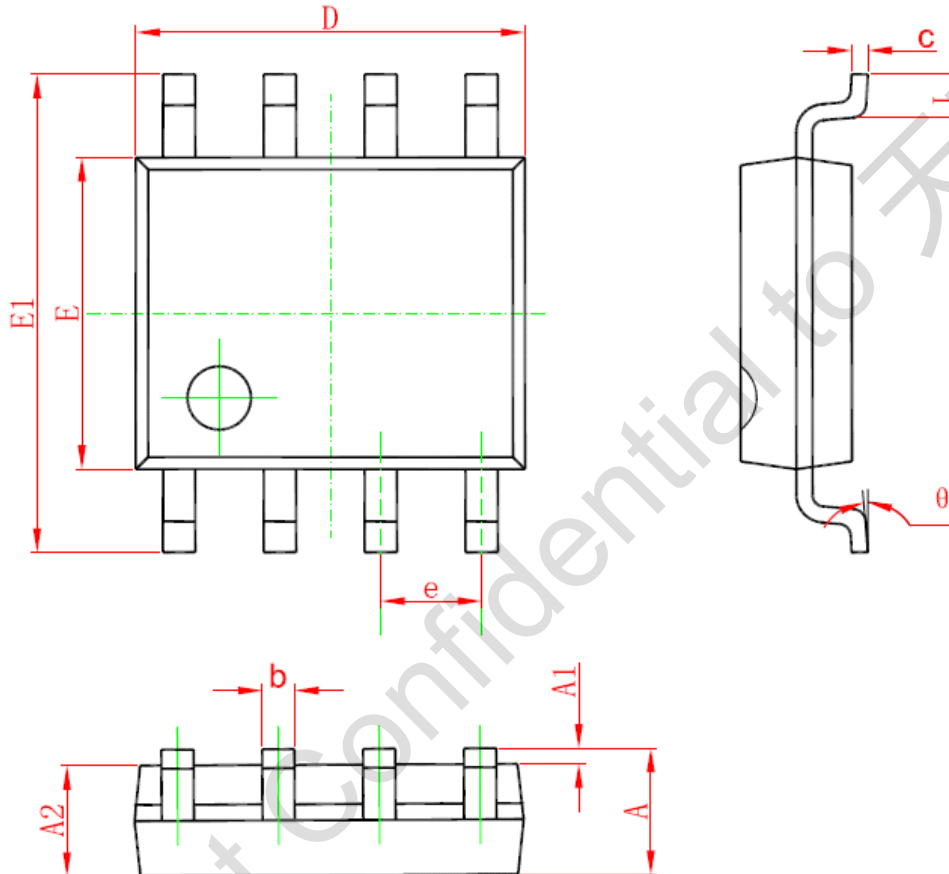
The output stage is designed to ensure zero cross-conduction current. This minimizes heat dissipation, increase efficiency, and enhance reliability. The output driver is also slew rate controlled to minimize EMI. The built-in 15V clamp at the gate output protects the MOSFET gate from high voltage stress.

- **Protection Controls**

OB3340 ensures good reliability design through its good protection coverage. VCC under voltage lockout (UVLO), Output short and open protection, VCC over voltage protection(auto recovery), Cycle-by-cycle current limiting and output gate clamp are standard features provided.

8-Pin Plastic SOP

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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