16-CHARACTER 1-LINE DOT MATRIX VFD CONTROLLER DRIVER

■ GENERAL DESCRIPTION

The NJU3430 is a Dot Matrix VFD (Vacuum Fluorescent Display) Controller Driver for 16-character 1-line with Icon display.

It contains character generator ROM/RAM, address counter, oscillation circuit, command register, Icon display RAM, high voltage drivers, and serial interface circuit.

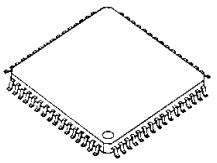
The display data or the command data is transmitted with the serial interface circuits.

The character generator consists of 8,400 bits ROM and 35 x 8 bits RAM. The CG RAM stores 8 kinds of character by 5 x 7dots maximum.

The 16-common and 37-segment (35 for character, 2 for icon) drivers operated up to 45V drive the display of 16-character 1-line with 32-Icon.

Furthermore, the NJU3430 incorporates one Output port which drives the LED.

■ PACKAGE OUTLINE



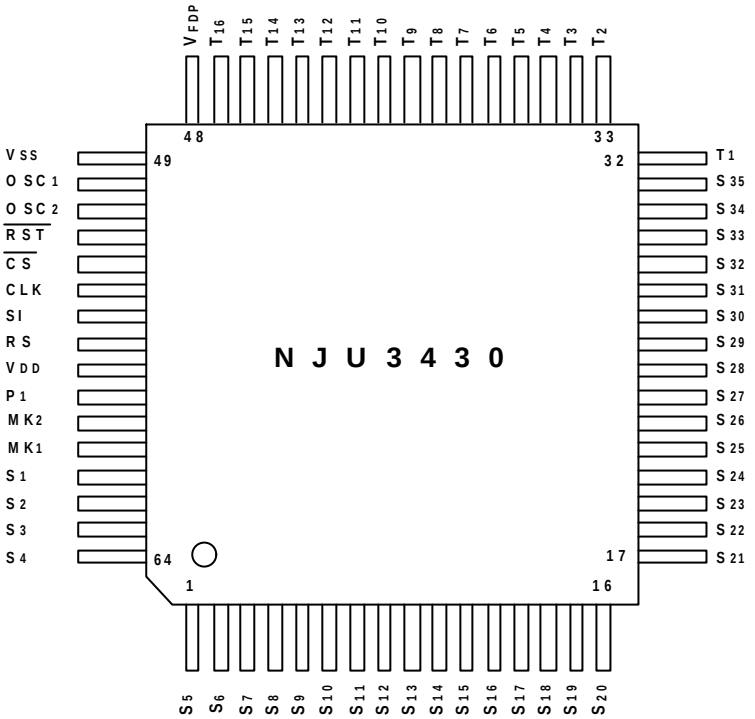
NJU3430FG1

■ FEATURES

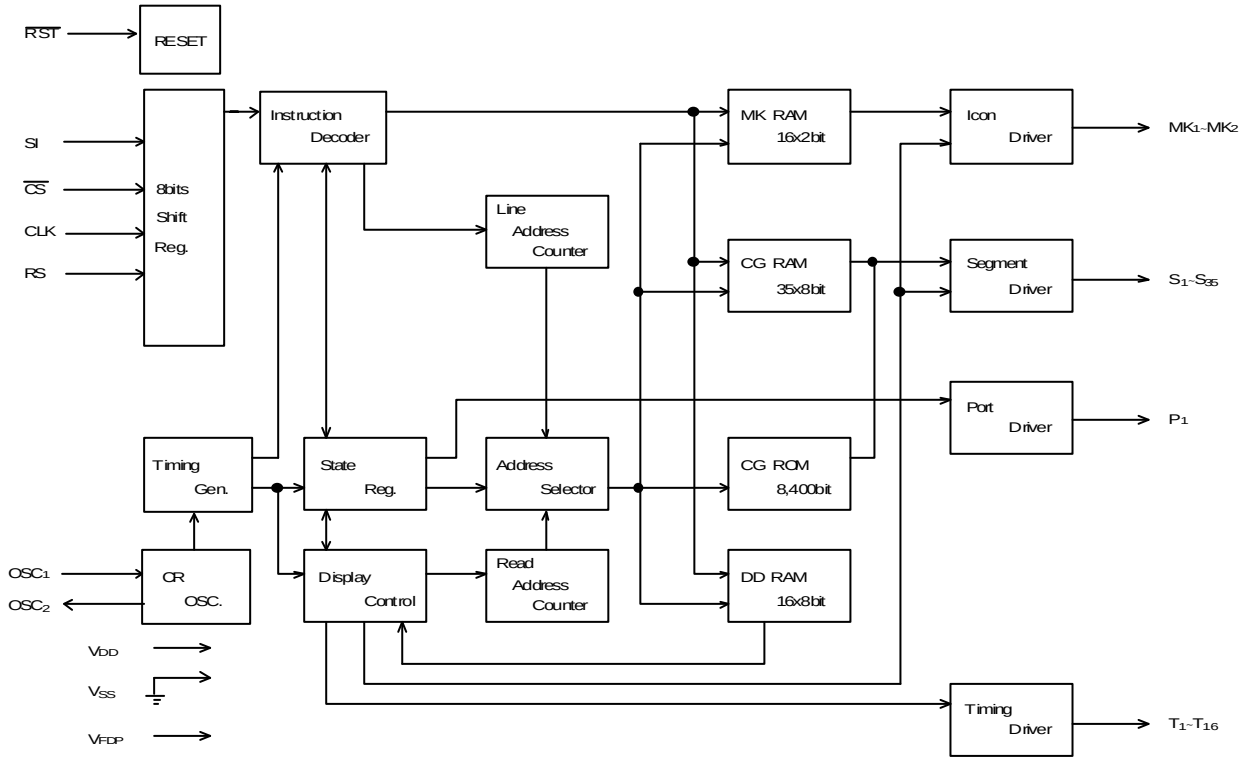
- 16-character 1-line Dot Matrix VFD Controller Driver
- Serial Interface with Microprocessor
- Display Data RAM 16 x 8 bits : 16-character 1-line Display
- Character Generator ROM 8,400 bits : 240 Characters for 5 x 7 Dots
- Character Generator RAM 35 x 8 bits : 8 Patterns (5 x 7 Dots)
- Icon Display RAM 16 x 2 bits : Maximum 32 Icon
- VFD Driving Voltage $|V_{DD}-V_{FDP}| \leq 45V$
  - Timing Signal : 16
  - Segment Signal : 35 (Except for Icon Segment Signal)
- Output Port for LED : 1
- Display ON/OFF Function
- Digit Scan Function
- Display Duty (Contrast Control) : 8-step (8/16 to 15/16)
- Character / Icon Shift Function
- Display Mode (9 to 16 Digits)
- Oscillation Circuit on-chip (External Resistor and Capacitor Required)
- Operating Voltage 3.0V to 5.5V (Except VFD Driving Voltage)
- Package Outline QFP 64
- C-MOS Technology

Jul. 2003
Ver. 3

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	F U N C T I O N
57	V_{DD}	-	Power Source : V_{DD}=+3.0 to 5.5V
49	V_{SS}	-	GND : V_{SS}=0V
48	V_{FDP}	-	VFD Driving Power Sourse V_{DD}-20V to V_{DD}-45V
50	OSC_1	I	CR Oscillation Terminal External R and C connect to these terminals. (Target f_{OSC}=360kHz)
51	OSC_2	O	
54	CLK	I	Serial Clock Input Terminal The serial data input synchronizing the rise edge of this terminal.
53	$\overline{CS}$	I	Chip Select Terminal When the CS terminal is "H" the serial data input is not available.
55	SI	I	Serial Data Input Terminal The data input is MSB first.
56	RS	I	Register Selection Signal Input Terminal RS="0" : Instruction Register RS="1" : Data Register
52	$\overline{RST}$	I	Reset Terminal RST="L" : Reset -Each Address : $(00)_H$ -Each RAM Data : Unfixed -Display Digits : 16-digit -Contrast Control : 8/16 Dury -All Display Off -All Outputs are "L"
61 to 64, 1 to 31	S_1 to S_{35}	O	Segment Output Terminals (Internal Pull-down Resistance)
32 to 47	T_1 to T_{16}	O	Timing Output Terminals (Internal Pull-down Resistance)
60 59	MK_1 MK_2	O	Icon Output Terminals (Internal Pull-down Resistance)
58	P_1	O	Output Port Terminal This terminal is suitable for LED.

■ FUNCTION DESCRIPTION

(1)CG RAM data and Character Dot Matrix

The character generator RAM (CG RAM) stores any kinds of character pattern by 5 x 7 dots written by the user program to display user's original character pattern. The CG RAM stores 8 kinds of character by 5 x 7 dots maximum.

To display user's original character pattern stored in the CG RAM, the address data (00)H - (07) should be written to the DD RAM as shown in Table 2.

Table 1.Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern(5 x 7 dots).

Character Code (DD RAM Data)	CG RAM Address						Correspondence of CG RAM Data and SEG Terminal				
	AC5	AC4	AC3	AC2	AC1	AC0	SC4	SC3	SC2	SC1	SC0
(00)H	0	0	0	0	0	0	S1	S2	S3	S4	S5
				0	0	1	S6	S7	S8	S9	S10
				0	1	0	S11	S12	S13	S14	S15
				0	1	1	S16	S17	S18	S19	S20
				1	0	0	S21	S22	S23	S24	S25
				1	0	1	S26	S27	S28	S29	S30
				1	1	0	S31	S32	S33	S34	S35
				1	1	1	Invalid Address				
(01)H	0	0	1	0	0	0	S1	S2	S3	S4	S5
				0	0	1	S6	S7	S8	S9	S10
				0	1	0	S11	S12	S13	S14	S15
				0	1	1	S16	S17	S18	S19	S20
				1	0	0	S21	S22	S23	S24	S25
				1	0	1	S26	S27	S28	S29	S30
				1	1	0	S31	S32	S33	S34	S35
				1	1	1	Invalid Address				
:	:			:			:				
(07)H	1	1	1	0	0	0	S1	S2	S3	S4	S5
				0	0	1	S6	S7	S8	S9	S10
				0	1	0	S11	S12	S13	S14	S15
				0	1	1	S16	S17	S18	S19	S20
				1	0	0	S21	S22	S23	S24	S25
				1	0	1	S26	S27	S28	S29	S30
				1	1	0	S31	S32	S33	S34	S35
				1	1	1	Invalid Address				

* When the data is written to CG RAM successively, the invalid address is skipped automatically.

(Ex.)CG RAM Address : (06)H → CG RAM Address : (08)H

After data writing operation

Table 2.CG ROM Character Pattern (ROM version -02)

Lower 4bit (Hexadecimal) \ Upper 4bit (Hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

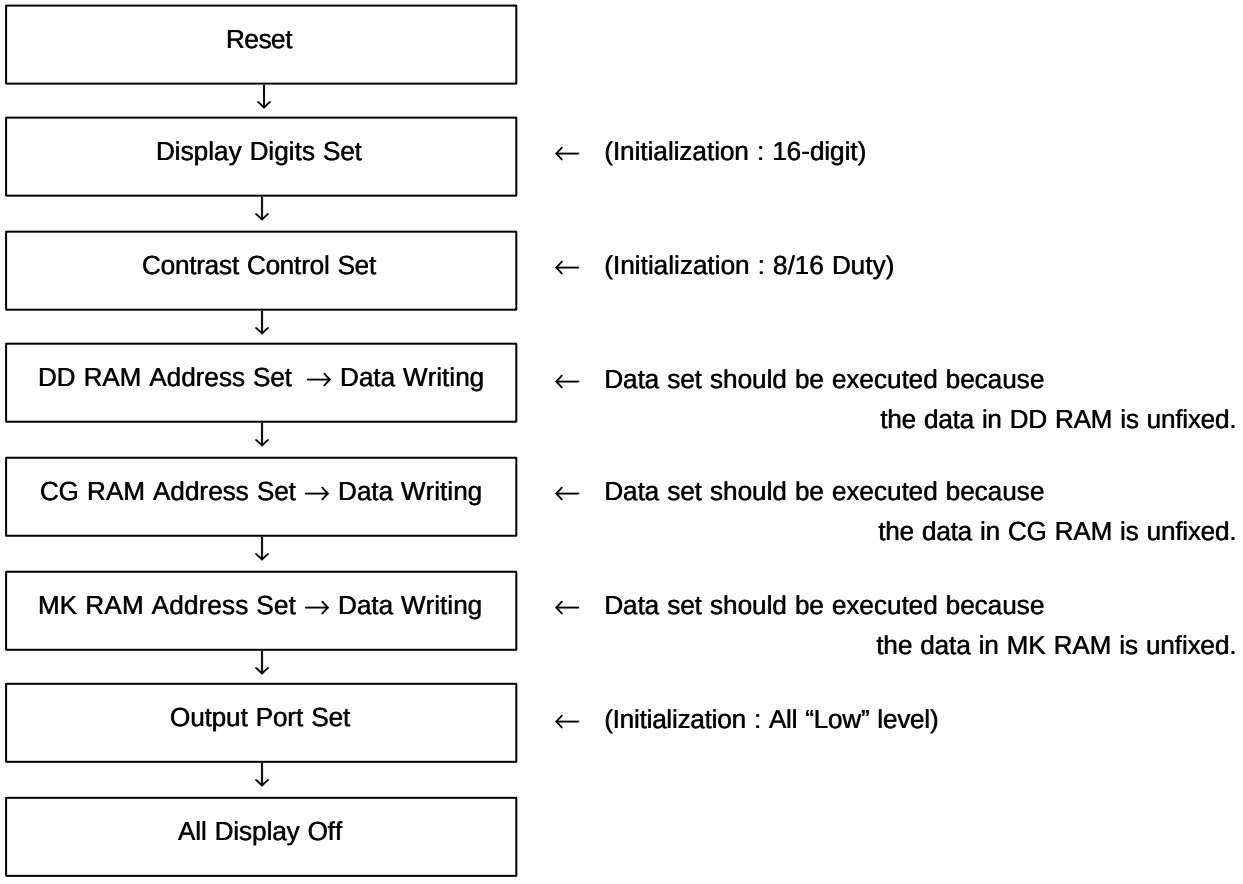
(2)Reset Function

(2-1)Initialization by Reset Terminal

The NJU3430 incorporates $\overline{RST}$ terminal to initialize the all system. When the "L" level is input over 1us to the $\overline{RST}$ terminal, the reset sequence is executed. The Initialization flow is shown below :

Each RAM Address	--- (00)H
Each RAM Data	--- Unfixed
Output Port	--- "L" Level (VSS)
Display Digits	--- 16-digit
Contrast Control	--- 8/16 Duty
All Display ON/OFF	--- All Display OFF

(2-2)Initialization (After the Reset)



(3)Instruction

Each instruction is shown in the Table 3. The data should be written to the RAM continuously after the RAM address set. The order of data writing is MSB first.

Table 3. Table of Instruction

INSTRUCTION	RS	MSB Serial Data LSB								DESCRIPTION
		B7	B6	B5	B4	B3	B2	B1	B0	
Maker Test	0	0	0	0	0	0	0	0	0	
Output Port Set	0	0	0	0	0	0	0	1	P1	Output Port Control
Display On/Off	0	0	0	0	0	0	1	M	D	Set the Display On/Off (Character and Icon)
Display Duty Set	0	0	0	0	0	1	D2	D1	D0	Set the Contrast Control
Display Shift	0	0	0	0	1	0	LR	M	D	Set the Display Shift (Character and Icon)
Display Blink Set	0	0	0	1	B2	B1	B0	M	D	Set the Blink Interval (Character and Icon)
Display Digits Set	0	0	1	0	0	0	C2	C1	C0	Set the Display Digits (9 to 16 degits)
RAM Address Set	0	1	0	0	0	AD3	AD2	AD1	AD0	Set the RAM Address (AD0 to AD3 : DD RAM) (AM0 to AM3 : MK RAM) (AC0 to AC5 : CG RAM)
			0	0	1	AM3	AM2	AM1	AM0	
			1	AC5	AC4	AC3	AC2	AC1	AC0	
Write Data to RAM	1	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	After the RAM Address Set, the data should be written to RAM (SD0 to SD7 : DD RAM) (SM0 to SM1 : MK RAM) (SC0 to SC4 : CG RAM)
		0	0	0	0	0	0	SM1	SM0	
		0	0	0	SC4	SC3	SC2	SC1	SC0	

*Instruction is executed within 32uS from the rise edge of the Chip Select CS Signal. (at fOSC=250kHz)

(3-1)Description of each Instruction

(a)Maker Testing

RS	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	0	0

Set the test mode.

(b)Output Port Set

RS	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	0	1	P1

Set the Output Port (1 bit static operation)."P1" is Output Port name.
*P1 does not drive VFD.

P1	FUNCTION
0	"L" level is output.
1	"H" level is output.

(c)Display On/Off

RS	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	0	1	M	D

Set the Display On/Off (Character and Icon). All Display are Off after Reset.

M	D	FUNCTION
0	0	Icon Display "Off", Character Display "Off"
0	1	Icon Display "Off", Character Display "On"
1	0	Icon Display "On", Character Display "Off"
1	1	Icon Display "On", Character Display "On"

(d)Display Duty Set

RS	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	1	D2	D1	D0

One duty is selected from among eight kinds of duty by Display Duty Set. 8/16 Duty (lowest contrast) is set after reset, an optional duty should be selected before display operation.

B2	B1	B0	Duty
0	0	0	8/16
0	0	1	9/16
:	:	:	:
1	1	0	14/16
1	1	1	15/16

(e)Display Shift

RS	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	1	0	LR	M	D

The display positions of Character and Icon are shifted by Display Shift instruction. When the codes of "LR", "M" and "D" mentioned below are written into "B2", "B1" and "B0", the display positions are shifted individually.

LR	FUNCTION
0	Shift the display position to the right.
1	Shift the display position to the left.

M	FUNCTION
0	The shift operation is not available.
1	The shift oparation is selected for Icon.

D	FUNCTION
0	The shift operation is not available.
1	The shift oparation is selected for Character.

16-digit Display Example

[Input Data] [Correspondence of DD RAM, MK RAM Address and Display]

	1-digit								8-digit							16-digit	
00010001	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← MK RAM
(DD RAM right shift)	0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	← DD RAM
00010010	0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	← MK RAM
(MK RAM right shift)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM
00010011	0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	← MK RAM
(DD,MK RAM right shift)	0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	← DD RAM

9-digit Display Example

[Input Data] [Correspondence of DD RAM, MK RAM Address and Display]

	1-digit							8-digit		
00010001	00	01	02	03	04	05	06	07	08	← MK RAM
(DD RAM right shift)	0F	00	01	02	03	04	05	06	07	← DD RAM
00010010	0F	00	01	02	03	04	05	06	07	← MK RAM
(MK RAM right shift)	00	01	02	03	04	05	06	07	08	← DD RAM
00010011	0F	00	01	02	03	04	05	06	07	← MK RAM
(DD,MK RAM right shift)	0F	00	01	02	03	04	05	06	07	← DD RAM

*In spite of display digits, the data of 16-digit is required to write into DD RAM.

(f)Display Blink Set

RS	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	1	B2	B1	B0	M	D

One blink state of Character and Icon is selected from among eight-step blink state by Display Blink Set. Non-Blink is selected after Reset. The optional blink state should be selected before display operation.

B2	B1	B0	STATUS
0	0	0	Non-Blink
0	0	1	Blink at about 0.1s
:	:	:	:
1	1	0	Blink at about 0.6s
1	1	1	Blink at about 0.7s

M	FUNCTION
0	The blink operation is not available.
1	The blink oparation is selected for Icon.

D	FUNCTION
0	The blink operation is not available.
1	The blink oparation is selected for Character.

*At f_{OSC}=360kHz

(g)Display Digits Set

RS	B7	B6	B5	B4	B3	B2	B1	B0
0	0	1	0	0	0	C2	C1	C0

The number of display digits is selected from among 9-digit to 16-digit by Display Digits Set. 16-digit is selected after Reset. The optional number of display digits should be selected before display operation.

C2	C1	C0	Display Digits
0	0	0	16-digit display
0	0	1	9-digit display
:	:	:	:
1	1	0	14-digit display
1	1	1	15-digit display

(h)RAM Address Set

RS	B7	B6	B5	B4	B3	B2	B1	B0	
0	1	0	0	0	AD3	AD2	AD1	AD0	← DD RAM Addredd Set:(00)H to (0F)H
	1	0	0	1	AM3	AM2	AM1	AM0	← MK RAM Address Set:(00)H to (0F)H
	1	1	AC5	AC4	AC3	AC2	AC1	AC0	← CG RAM Address Set:(00)H to (3F)H

The DD RAM, MK RAM and CG RAM Address are set by RAM Address Set. Correspondences of each RAM address and Display position are shown below :

Correspondence of DD RAM Address and Timing terminals (Not shift)

DD RAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Digits	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Correspondence of MK RAM Address and Timing terminals (Not shift)

MK RAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Digits	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

About the detail of CG RAM Address, refer to "(1)CG RAM data and Character Dot Matrix".

(i)Write Data to RAM

RS	B7	B6	B5	B4	B3	B2	B1	B0	
1	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0	← DD RAM Data Set:(00)H to (FF)H
	0	0	0	0	0	0	SM1	SM0	← MK RAM Data Set:(00)H to (03)H
	0	0	0	SC4	SC3	SC2	SC1	SC0	← CG RAM Data Set:(00)H to (1F)H

The data are written into DD RAM, MK RAM and CG RAM by Write Data to RAM. The writing data address is used that is set the address just before writing data. Therefore, when the new data writing, the address set should be executed before writing data. The address is increased by 1 automatically after writing data, therefore, the MPU writes the data into the each RAM without any address setting after the start address.

(Writing example)

1Byte	2Byte	3Byte	4Byte
10000011	01010101	11111000	00110101
DD RAM Address set(03)H	DD RAM Address(03)H set CG ROM(55)H	DD RAM Address(04)H set CG ROM(F8)H	DD RAM Address(05)H set CG ROM(35)H

The writing data in the each RAM are shown below.

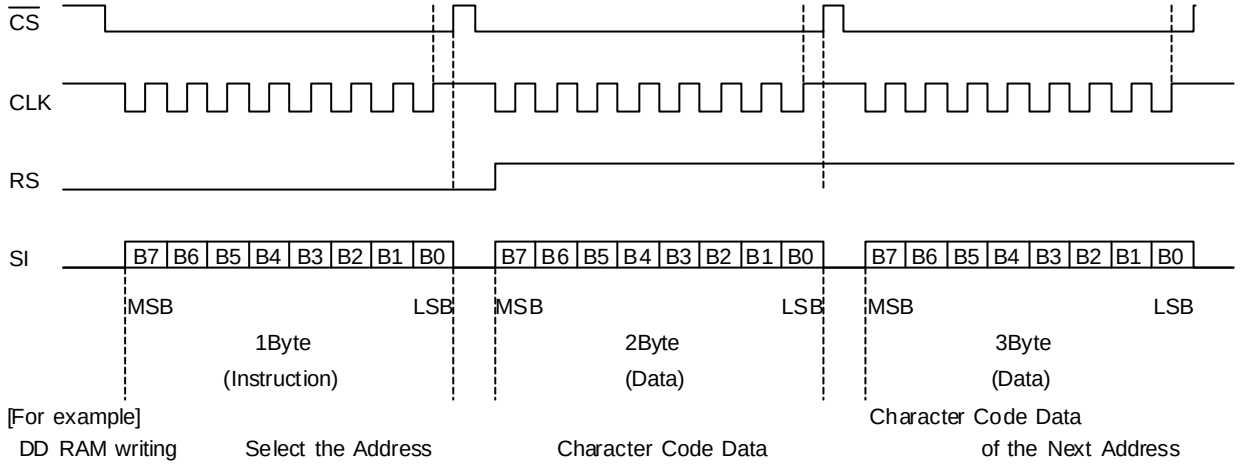
DD RAM Data[SD7 to SD0] --- Character code of each digit : (00)H to (FF)H
MK RAM Data[SM1 to SM0] --- Icon display of each digit : SM1→MK2, SM0→MK1
CG RAM Data[SC4 to SC0] --- Character code : (00)H to (0F)H Dot Data
(About the detail, refer to "(1)CG RAM data and Character Dot Matrix".)

■ Interface with MPU

The instruction and RAM data are input through the serial port. The data form is 8-bit per word, and data transfer is performed by synchronizing clock. The shift clock is input from external, and the data is loaded at the rising edge of the shift clock.

One time transfer is executed by 8-bit unit. The transfer period is from falling edge to rising of the CS signal from external. Therefore, when the rising edge of the CS signal is input, the operation is started. When more than 8-bit data is input, the last 8-bit data is valid.

The input data is judged as instruction or RAM data by the RS signal at the rising edge of the CS signal (RS="H" : RAM data, RS="L" : Instruction). When the input data is RAM data, the RAM address is increased one by one automatically after data writing.



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT	CONDITIONS
Supply Voltage (1)	V_{DD}	-0.3 to 6.5	V	
Supply Voltage (2)	V_{FDP}	-40 to V_{DD}+0.3	V	
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V	
Power Dissipation	P_D	800	mW	Ta≤25°C QFP-64
Storage Temperature	Tstg	-55 to 125	°C	
Operating Temperature	Topr	-40 to 85	°C	
Output Current	I_{O1}	-40	mA	T1 - T16
	I_{O2}	-20	mA	MK1 - MK2
	I_{O3}	-10	mA	S1 - S35
	I_{O4}	-4.0	mA	P1(LED drive is available)
Total Output Current	ΣI_{OH}	-100	mA	All Terminals at "H" level
	ΣI_{OL}	100	mA	All Terminals at "L" level

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) Decoupling capacitor should be connected between V_{DD} and V_{SS}, V_{FDP} and V_{SS} due to the stabilized operation for the LSI.

Note 3) All voltage values are specified as V_{SS} = 0V.
The relation : $V_{DD} > V_{SS}$, $V_{DD} > V_{SS} \geq V_{FDP}$, V_{SS}=0V must be maintained.

■ ELECTRICAL CHARACTERISTICS (V_{DD}=5.0V ± 10%, V_{FDP}=V_{DD}-40V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Input Voltage	V_{IH}			0.8V_{DD}			V	4
	V_{IL}					0.2V_{DD}		
Input Leakage Current	I_{IH}	V_{IH}=V_{DD}		-1.0		1.0	uA	4
	I_{IL}	V_{IL}=0V		-1.0		1.0		
Output Voltage	V_{OH1}	I_{OH1}=-30mA		V_{DD}-1.5			V	5
	V_{OH2}	I_{OH2}=-15mA		V_{DD}-1.5				6
	V_{OH3}	I_{OH3}= -6mA		V_{DD}-1.5				7
	V_{OH4}	I_{OH4}= -2mA		V_{DD}-1.0				8
	V_{OL1}	I_{LO1}= 2mA				1.0		8
Pull-down Resistance	R_{DT}			125	220	300	kΩ	5
Current	R_{DS}			180	310	420	kΩ	9
Operating Current (Only Logic circuit)	I_{SS1}	fosc=360kHz No load	Duty=15/16, Digit=1-16 All Output ON			3	mA	10
	I_{SS2}		Duty= 8/16, Digit=1-9 All Output OFF			2	mA	

(V_{DD}=3.3V ± 10%, V_{FDP}=V_{DD}-40V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Input Voltage	V_{IH}			0.8V_{DD}			V	4
	V_{IL}					0.2V_{DD}		
Input Leakage Current	I_{IH}	V_{IH}=V_{DD}		-1.0		1.0	uA	4
	I_{IL}	V_{IL}=0V		-1.0		1.0		
Output Voltage	V_{OH1}	I_{OH1}=-20mA		V_{DD}-2.0			V	5
	V_{OH2}	I_{OH2}=-10mA		V_{DD}-2.0				6
	V_{OH3}	I_{OH3}= -6mA		V_{DD}-2.0				7
	V_{OH4}	I_{OH4}= -2mA		V_{DD}-1.0				8
	V_{OL1}	I_{LO1}= 2mA				1.0		8
Pull-down Resistance	R_{DT}			125	220	300	kΩ	5
Current	R_{DS}			180	310	420	kΩ	9
Operating Current (Only Logic circuit)	I_{SS1}	fosc=360kHz No load	Duty=15/16, Digit=1-16 All Output ON			3	mA	10
	I_{SS2}		Duty= 8/16, Digit=1-9 All Output OFF			2	mA	

Note 4) Apply to the RS, $\overline{CS}$, CLK, SI, $\overline{RST}$ terminals.

Note 5) Apply to the T1 - T16 terminals.

Note 6) Apply to the MK1 - MK2 terminal.

Note 7) Apply to the S1 - S35 terminals.

Note 8) Apply to the P1 terminal.

Note 9) Apply to the MK1 - MK2 and S1 - S35 terminals.

Note 10) Measurement at the V_{SS} terminal.

■ AC CHARACTERISTICS (VDD=5.0V ± 10%, VFDP=VDD-40V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Oscillation Frequency	fOSC	R=68kΩ,C=390pF	250	360	470	kHz
Serial Clock Cycle Time	tCYCE	Fig.1	1			uS
Serial Clock Width	tSC		300			nS
Chip Select Pulse Width	PWCS		32			uS
Chip Select Set Up Time	tCSU		300			nS
Chip Select Hold Time	tCH		300			nS
Serial Input Data Set Up Time	tSISU		300			nS
Serial Input Data Hold Time	tSIH		300			nS
RS Set Up Time	tRS		300			nS
RS Hold Time	tRH		300			nS
$\overline{RST}$ Pulse Width	tRSL	Fig.2	1			uS
VDD-$\overline{RST}$ Input Timing	tRSON		50			uS
$\overline{RST}$-SI Input Timing	tRSOFF		50			uS
VDD Rise Time	tPRZ				50	uS

(VDD=3.3V ± 10%, VFDP=VDD-40V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Oscillation Frequency	fOSC	R=20kΩ,C=200pF	250	360	470	kHz
Serial Clock Cycle Time	tCYCE	Fig.1	1			uS
Serial Clock Width	tSC		300			nS
Chip Select Pulse Width	PWCS		32			uS
Chip Select Set Up Time	tCSU		300			nS
Chip Select Hold Time	tCH		300			nS
Serial Input Data Set Up Time	tSISU		300			nS
Serial Input Data Hold Time	tSIH		300			nS
RS Set Up Time	tRS		300			nS
RS Hold Time	tRH		300			nS
$\overline{RST}$ Pulse Width	tRSL	Fig.2	1			uS
VDD-$\overline{RST}$ Input Timing	tRSON		50			uS
$\overline{RST}$-SI Input Timing	tRSOFF		50			uS
VDD Rise Time	tPRZ				50	uS

- Timing Chart

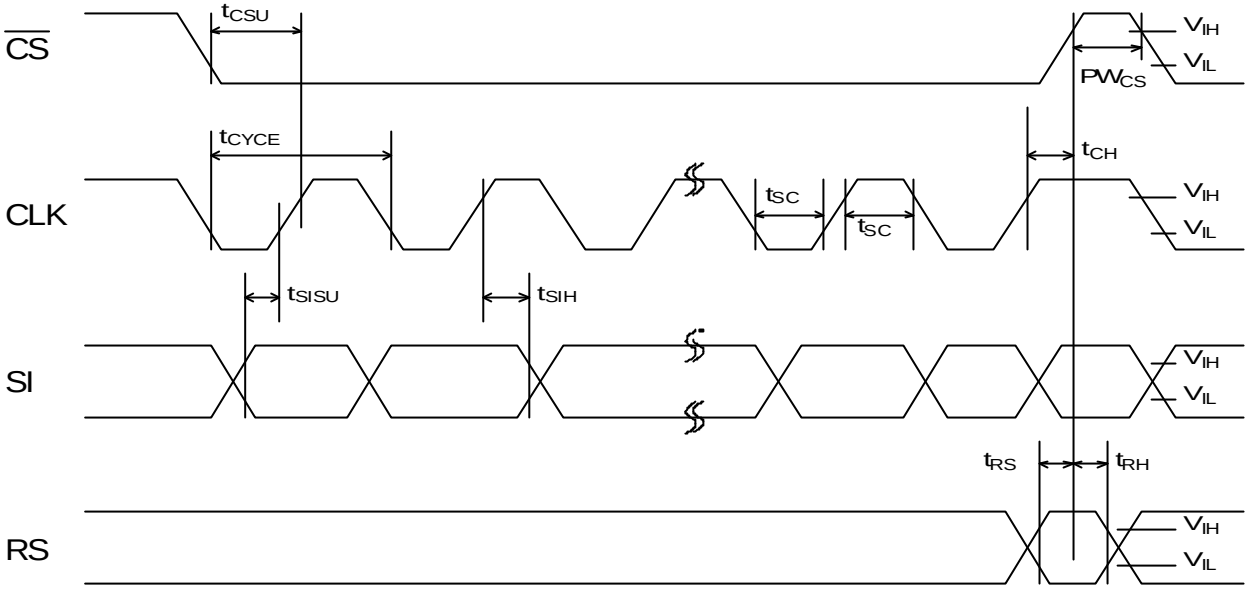


Fig.1 Data Input Timing

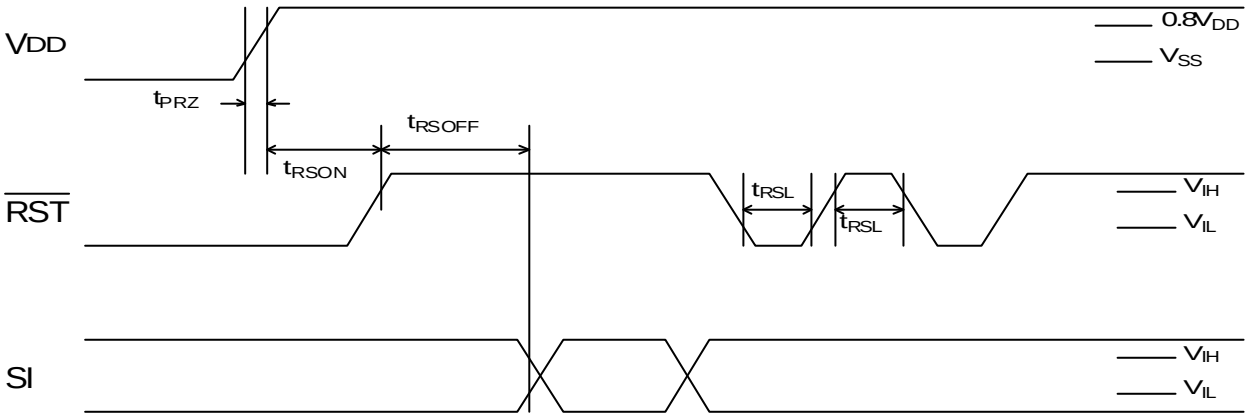


Fig.2 Reset Timing

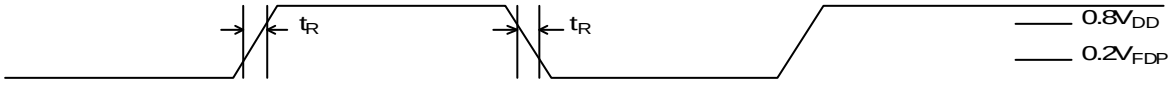
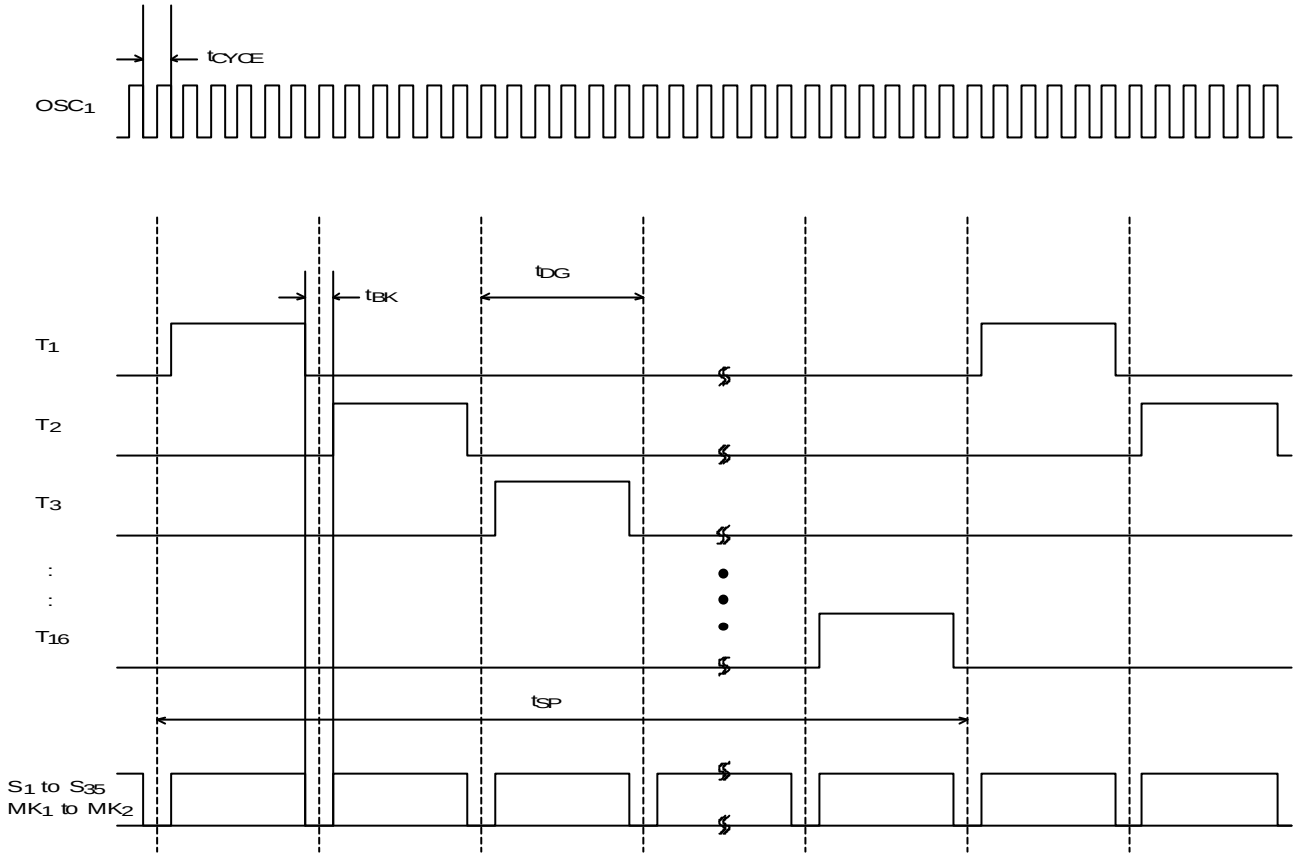


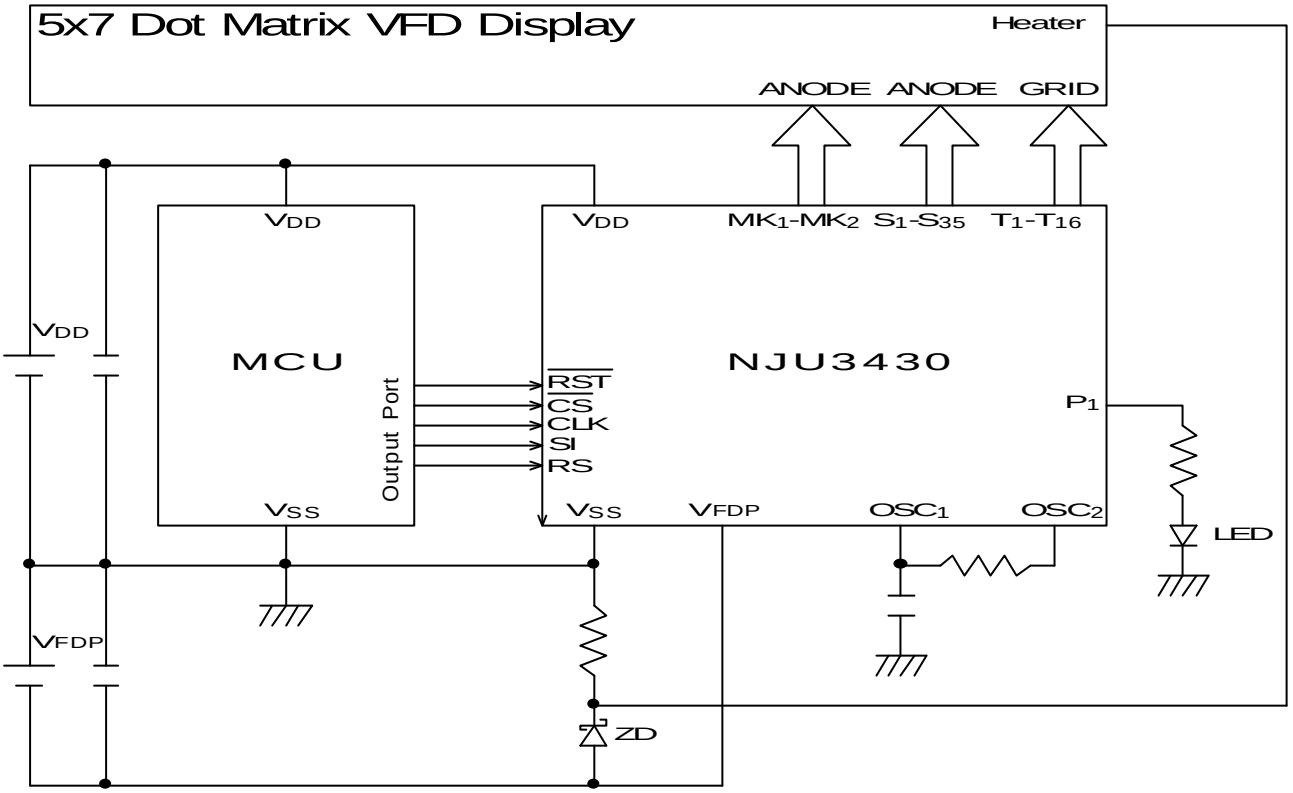
Fig.3 Output Timing (CL=100pF, tR=20 to 80% or 80 to 20%)

■ VFD DRIVING WAVE FORM



Oscillation Frequency	: t_{CYCE}
Minimum Blanking Time (Duty15/16)	: $t_{BK}=t_{CYCE} \times 4$
1-character Display Time	: $t_{DG}=t_{BK} \times 16$
1-cycle Display Time	: $t_{SP}=t_{DG} \times$ Digits

■ APPLICATION CIRCUIT



MEMO

[CAUTION]
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