



STF10NK50Z

N-channel 500 V, 0.55 Ω , 9 A Zener-protected SuperMESH™
Power MOSFET in TO-220FP package

Datasheet — production data

Features

Order code	V _{DSS}	R _{DS(on)} max	I _D	P _{TOT}
STF10NK50Z	500 V	< 0.7 Ω	9 A	30 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance

Applications

- Switching application

Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

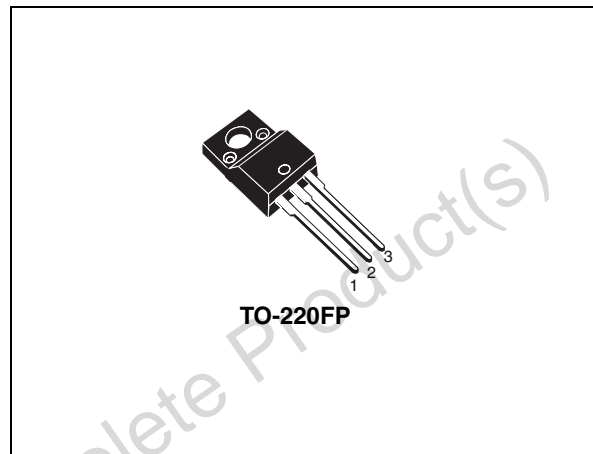


Figure 1. Internal schematic diagram

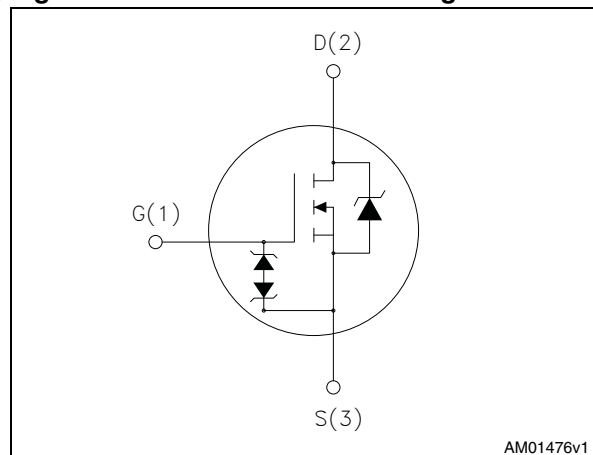


Table 1. Device summary

Order code	Marking	Package	Packaging
STF10NK50Z	F10NK50Z	TO-220FP	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuit	8
4	Package mechanical data	9
5	Revision history	12

Obsolete Product(s) - Obsolete Product(s)



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	9 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C=100\text{ }^\circ\text{C}$	5.7 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	36 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	30	W
	Derating factor	0.24	W/ $^\circ\text{C}$
ESD	Gate-source human body model ($C=100\text{ pF}$, $R=1.5\text{ k}\Omega$)	4	kV
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{ s}$; $T_C=25\text{ }^\circ\text{C}$)	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 9\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	4.2	$^\circ\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	9	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25\text{ }^\circ\text{C}$, $I_D=I_{AR}$, $V_{DD}=50\text{ V}$)	230	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 500 \text{ V}$ $V_{DS} = 500 \text{ V}, T_C = 125^{\circ}\text{C}$			1 50	μA μA
$V_{(BR)GSO}$	Gate-source breakdown voltage ($I_D = 0$)	$I_{GS} = \pm 1 \text{ mA}$	± 30			V
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100 \mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 4.5 \text{ A}$		0.55	0.7	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$		1219		pF
C_{oss}	Output capacitance		-	159	-	pF
C_{rss}	Reverse transfer capacitance				40	
$C_{oss \text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0 \text{ to } 400 \text{ V}$	-	806	-	pF
Q_g	Total gate charge	$V_{DD} = 400 \text{ V}, I_D = 9 \text{ A}$		39.2		nC
Q_{gs}	Gate-source charge	$V_{GS} = 10 \text{ V}$	-	7.42	-	nC
Q_{gd}	Gate-drain charge	See Figure 15		20.7		nC

1. $C_{oss \text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=250\text{ V}$, $I_D=4.5\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ See Figure 16	-	19	-	ns
t_r	Rise time		-	17	-	ns
$t_{d(off)}$	Turn-off delay Time		-	43	-	ns
t_f	Fall time		-	15	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=9\text{ A}$, $V_{GS}=0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD}=9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=35\text{ V}$	-	268		ns
Q_{rr}	Reverse recovery charge		-	1.83		μC
I_{RRM}	Reverse recovery current		-	13.7		A
t_{rr}	Reverse recovery time	$I_{SD}=9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=35\text{ V}$, $T_j=150\text{ }^\circ\text{C}$	-	343		ns
Q_{rr}	Reverse recovery charge		-	2.6		μC
I_{RRM}	Reverse recovery current		-	15.15		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS}=\pm 1\text{ mA}$ (open drain)	30	-	-	V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

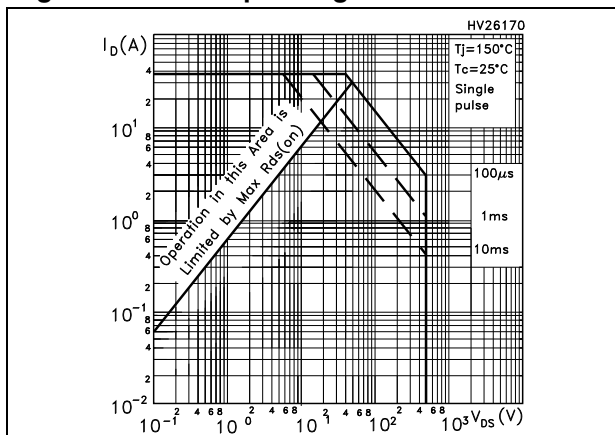


Figure 3. Thermal impedance

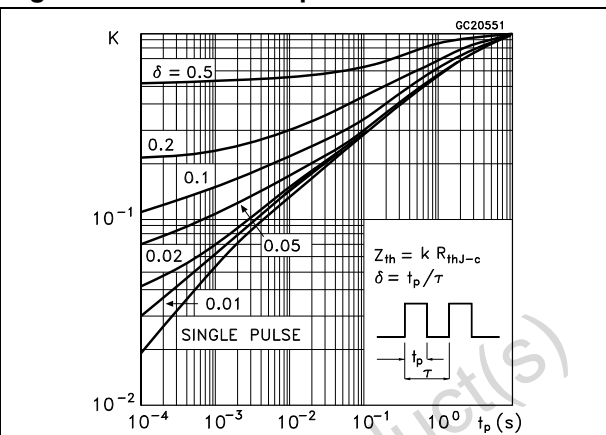


Figure 4. Output characteristics

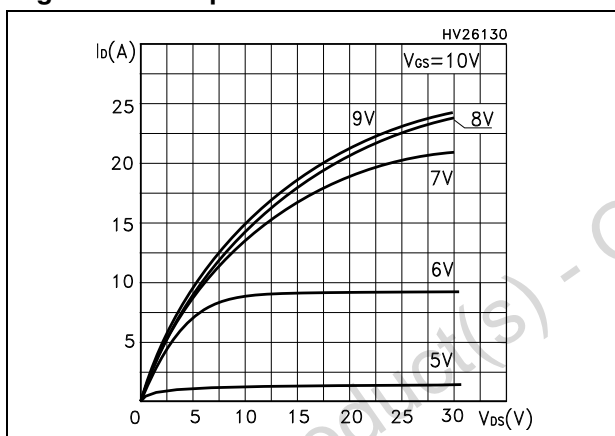


Figure 5. Transfer characteristics

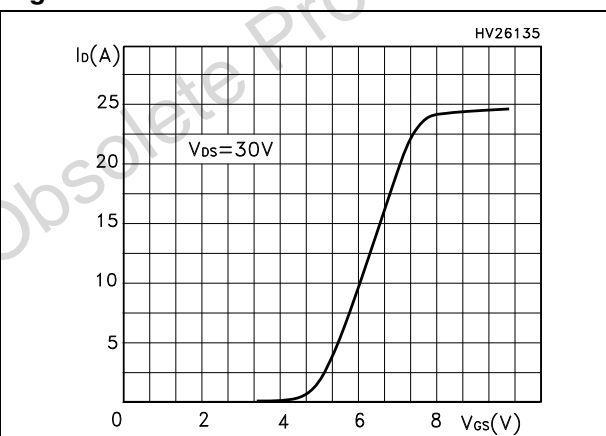


Figure 6. Normalized BV_{DSS} vs temperature

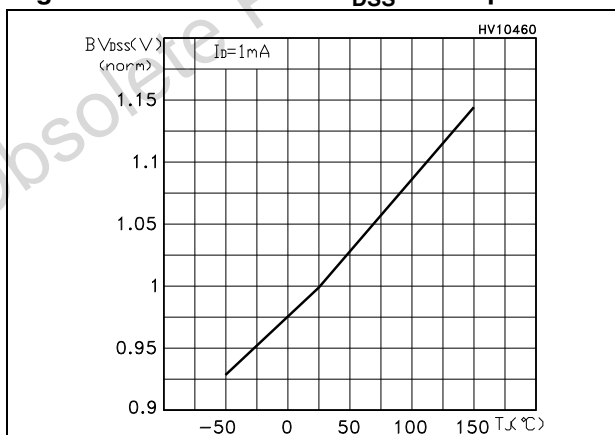


Figure 7. Static drain-source on-resistance

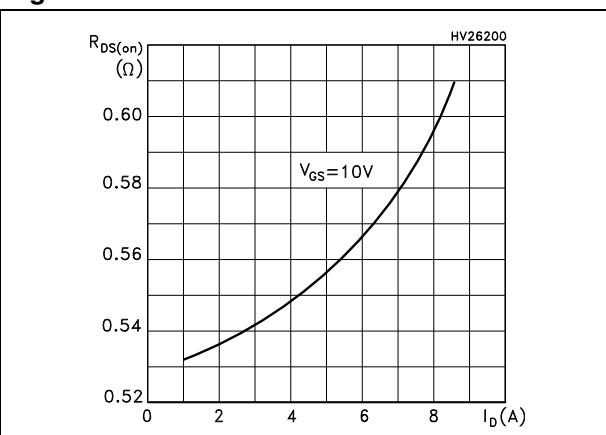


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

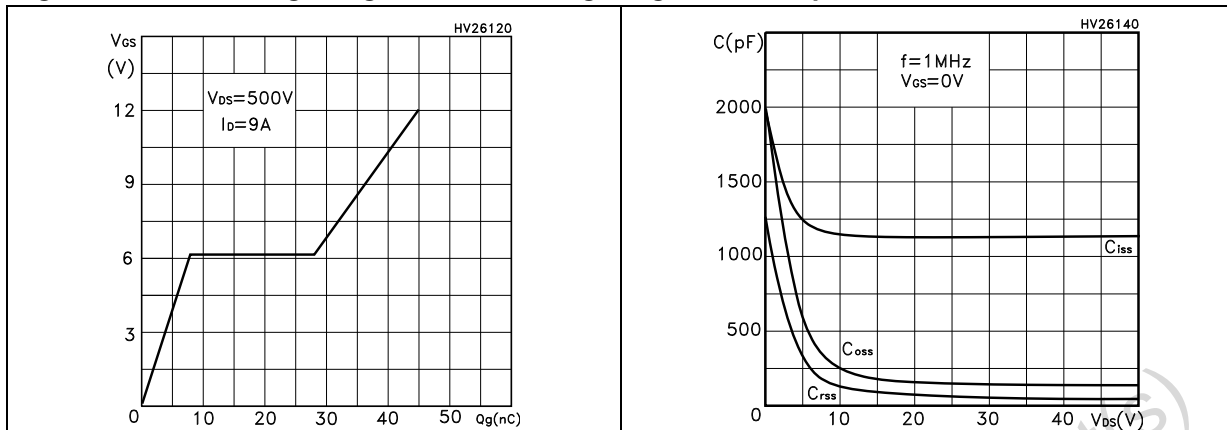


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

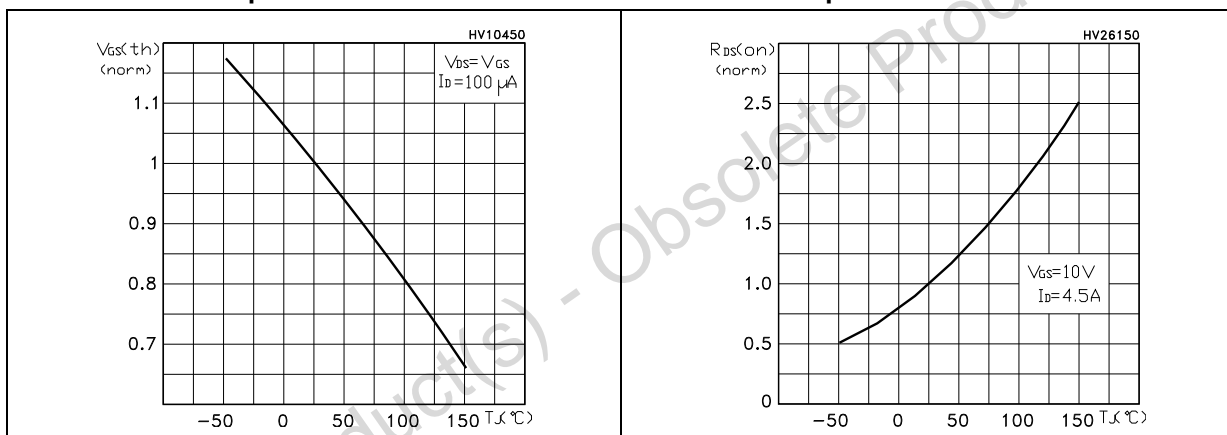
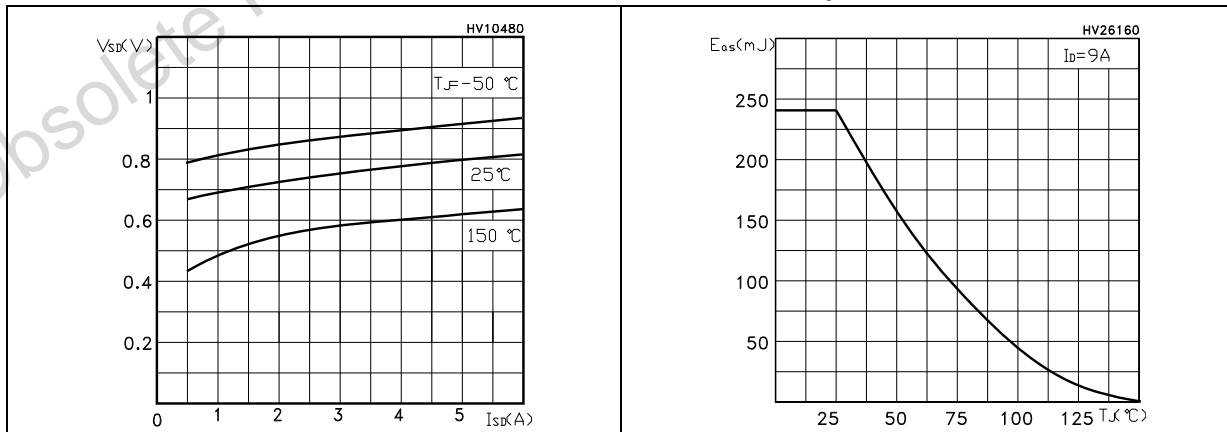
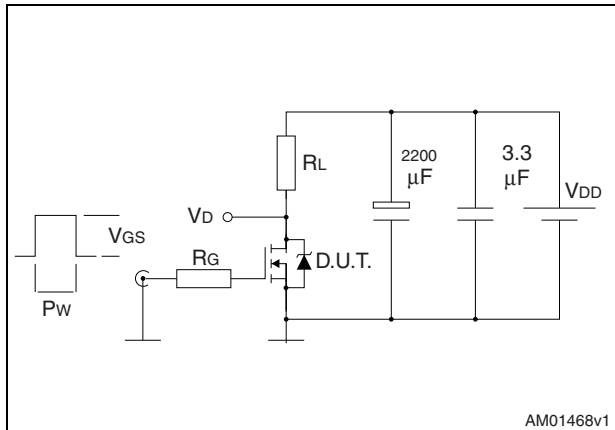


Figure 12. Source-drain diode forward characteristics Figure 13. Maximum avalanche energy vs temperature



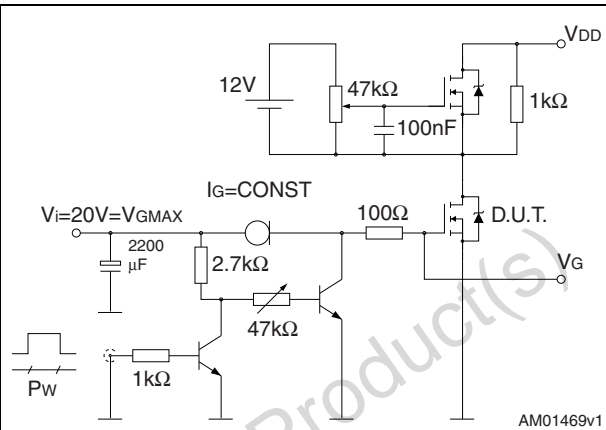
3 Test circuit

Figure 14. Switching times test circuit for resistive load



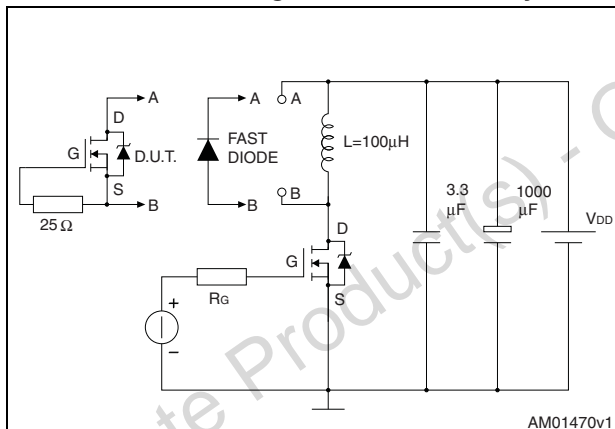
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Figure 15. Gate charge test circuit



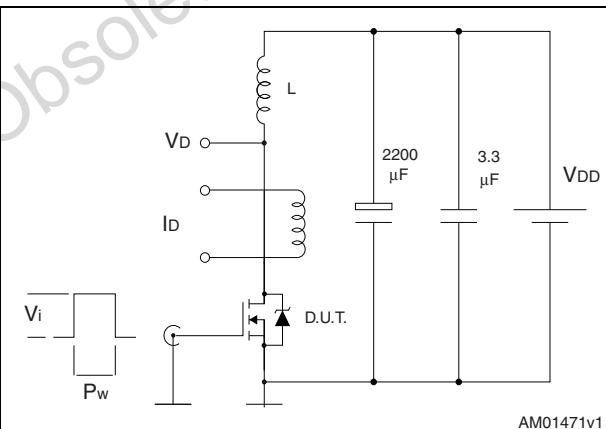
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Figure 16. Test circuit for inductive load switching and diode recovery times



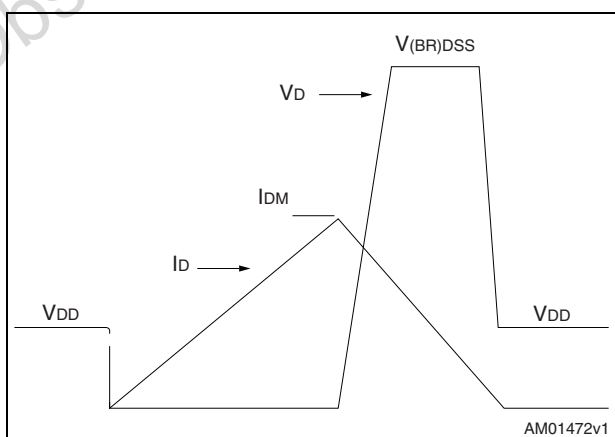
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Figure 17. Unclamped inductive load test circuit



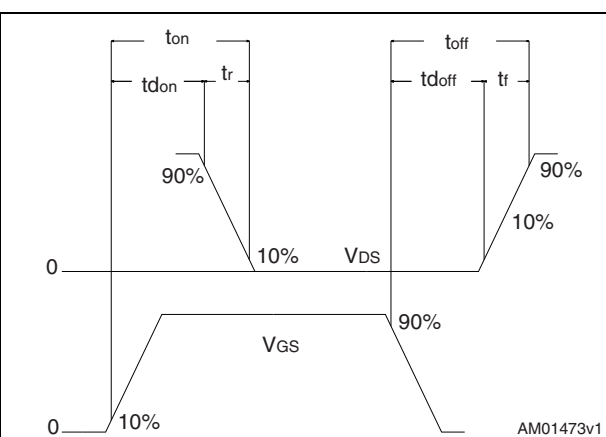
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Figure 18. Unclamped inductive waveform



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Figure 19. Switching time waveform



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4 Package mechanical data

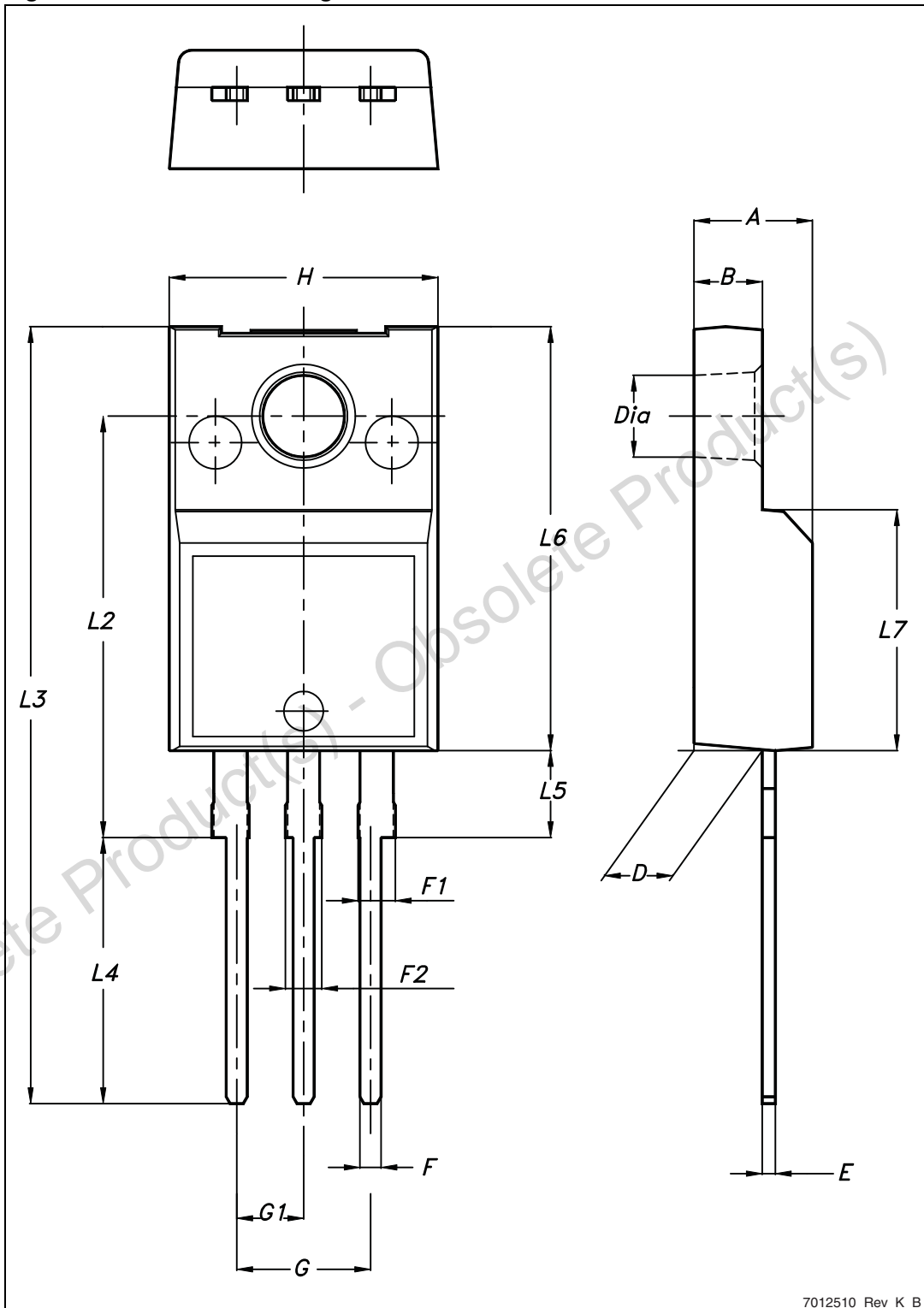
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Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 20. TO-220FP drawing



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
28-Mar-2012	1	First release.

Obsolete Product(s) - Obsolete Product(s)

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