ON Semiconductor™

DAP008 Maximus

PWM Current-Mode Controller for High-Power Universal Off-Line Supplies

Housed in an SO−8 package, the DAP008 represents a major leap toward ultra−compact Switch−Mode Power Supplies. Due to its novel concept, the circuit allows the implementation of complete off−line AC/DC adapters, battery charger or a high−power SMPS with few external components. Due to its high drive capability, ***Maximus*** is not afraid by 30 nC gate charge MOSFETs which, together with internal ramp compensation and built−in frequency jittering, ease the design of high power AC/DC adapters.

With an internal structure operating at a fixed 65 kHz, the controller supplies itself from the high−voltage rail, avoiding the need of an auxiliary winding. This feature naturally eases the designer task in battery charger applications. Finally, current−mode control provides an excellent audio−susceptibility and inherent pulse−by−pulse control.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so−called skip cycle mode and provides excellent efficiency at light loads. Because this occurs at a user adjustable low peak current, no acoustic noise takes place.

The DAP008 features two efficient protective circuitries:

1. In presence of an overcurrent condition, the output pulses are disabled and the device enters a safe burst mode, trying to restart. Once the default has gone, the device auto−recovers.
2. If an external signal (e.g. a temperature sensor) pulls the Adj pin above 3.2 V, the output pulses are immediately stopped and the DAP008 stays latched in this position. Reset occurs when the V_{CC} collapses to ground, e.g. the user unplugs the power supply.

Features

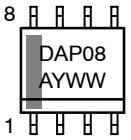
- No Auxiliary Winding Operation
- Internal Ramp Compensation
- Built−in Frequency Jittering for Lower EMI
- Internal 1.0 ms Typical Soft−Start
- Auto−Recovery Internal Output Short−Circuit Protection
- Full Latchoff if Adj Pin is Brought High
- Extremely Low No−Load Standby Power
- Current−Mode with Skip−Cycle Capability
- Internal Temperature Shutdown
- Internal Leading Edge Blanking
- 500 mA Peak Current Capability
- Internally Fixed Frequency at 65 kHz
- Direct Optocoupler Connection
- SPICE Models Available for TRANsient and AC Analysis
- Pb−Free Package is Available

Typical Applications

- High Power AC/DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Auxiliary Power Supplies (USB, Appliances, TVs, etc.)

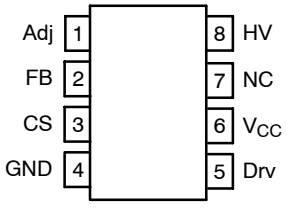
SO−8
D SUFFIX
CASE 751

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

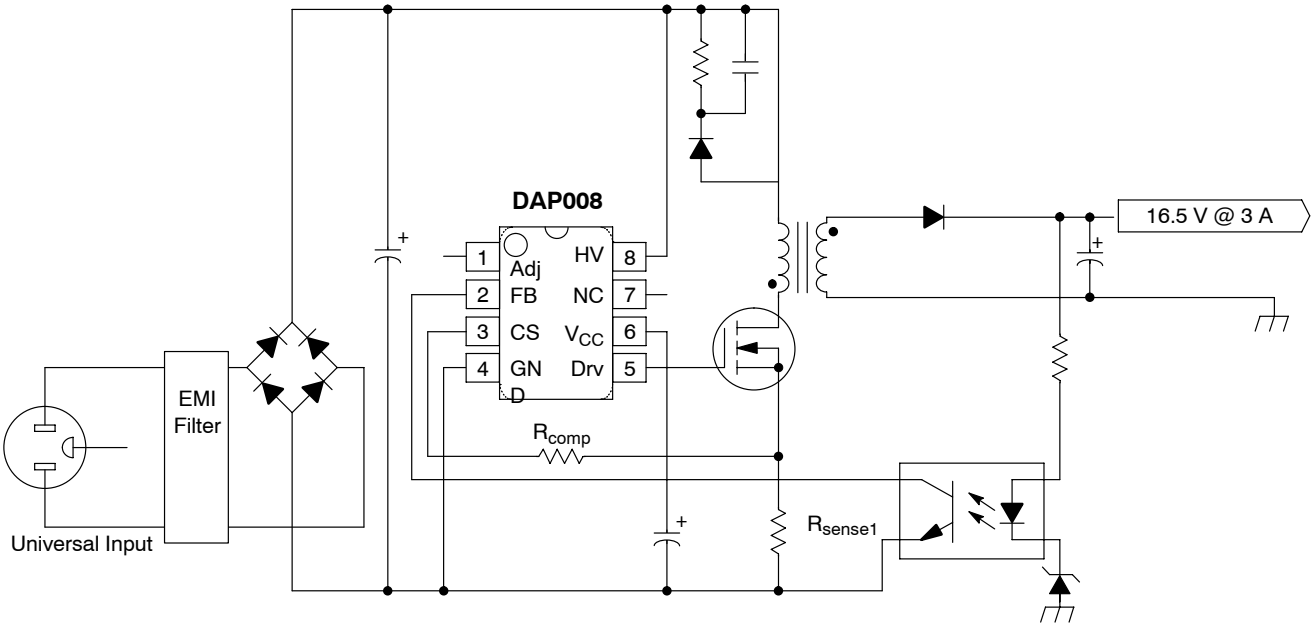


Figure 1. Typical Application

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	Adj	Adjust the skipping peak current	This pin lets you adjust the level at which the cycle skipping process takes place. Shorting this pin to ground, permanently disables the skip cycle feature. By bringing this pin above 3.2 V, you permanently shut off the device.
2	FB	Sets the peak current setpoint	By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand.
3	CS	Current sense input	This pin senses the primary current and routes it to the internal comparator via an L.E.B. By inserting a resistor in series with the pin, you control the amount of ramp compensation you need.
4	GND	The IC ground	–
5	Drv	Driving pulses	The driver's output to an external MOSFET.
6	V_{CC}	Supplies the IC	This pin is connected to an external bulk capacitor of typically 22 μF.
7	NC	–	This unconnected pin ensures adequate creepage distance.
8	HV	Generates the V_{CC} from the line	Connected to the high voltage rail, this pin injects a constant current into the V_{CC} bulk capacitor.

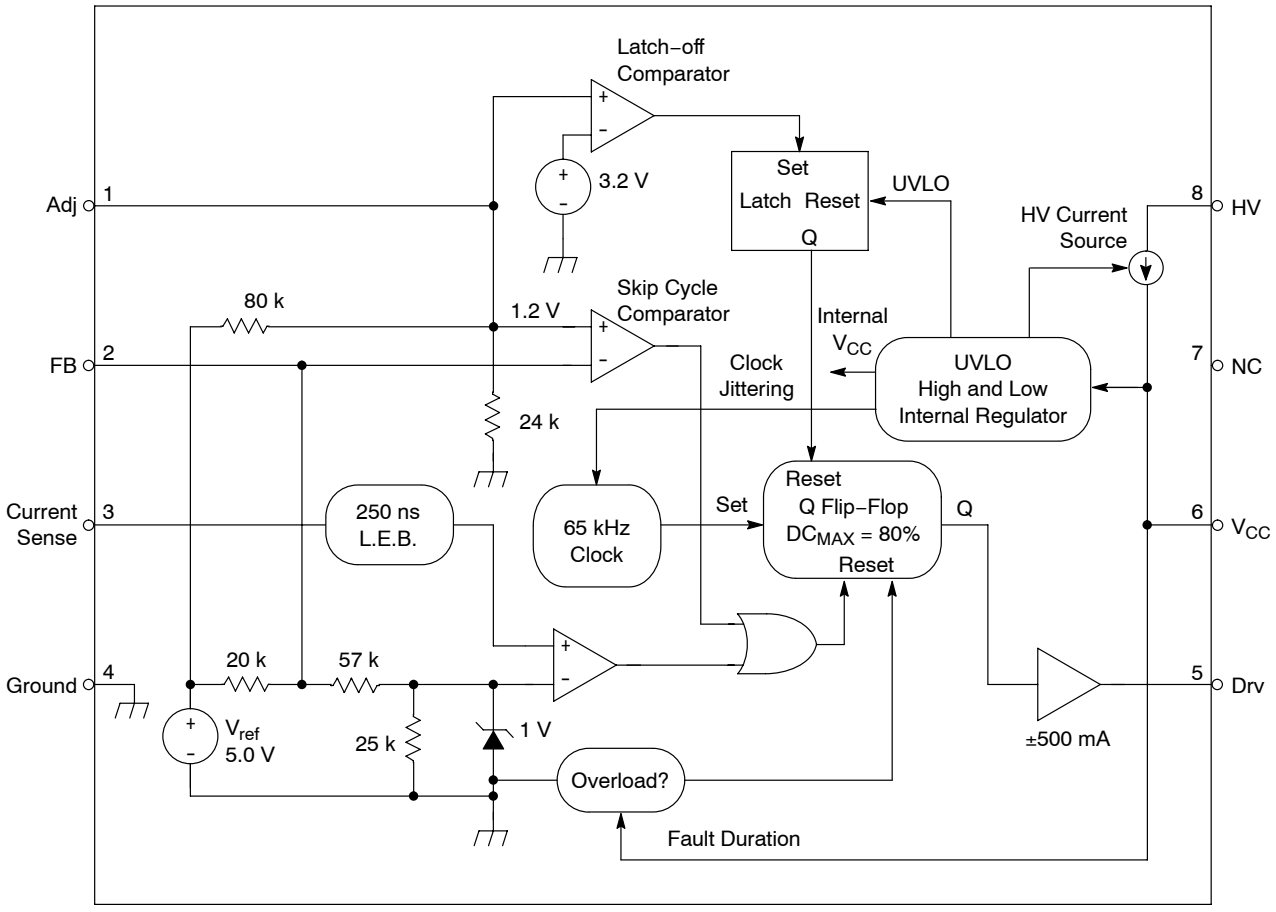


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Continuous Power Supply or Drive Voltage	V_{CC}, Drv	18	V
Transient Power Supply Voltage Duration < 10 ms, I_{VCC} < 10 mA	V_{CC}	20	V
Power Supply Voltage on all other pins except pin 8 (HV), pin 6 (V_{CC}) and pin 5 (Drv)	–	−0.8 to 10	V
Maximum Current into all pins except V_{CC} (6) and HV (8) when 10 V ESD diodes are activated	–	5.0	mA
Maximum Current into pin 6 when exceeding the 16 V maximum rating	I_V_{CC}	20	mA
Thermal Resistance Junction−to−Case	$R_{\theta JC}$	57	°C/W
Thermal Resistance Junction−to−Air, SOIC version	$R_{\theta JA}$	178	°C/W
Maximum Junction Temperature	TJ_{MAX}	150	°C
Temperature Shutdown	–	150	°C
Storage Temperature Range	–	−60 to +150	°C
ESD Capability, HBM Model (All pins except V_{CC} and HV)	–	2.0	kV
ESD Capability, Machine Model	–	200	V
Maximum Voltage on pin 8 (HV), pin 6 (V_{CC}) grounded	V_{HV}	450	V
Maximum Voltage on pin 8 (HV), pin 6 (V_{CC}) decoupled to ground with 10 μF	V_{HV}	500	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −5°C to +125°C, Max T_J = 150°C, V_{CC} = 11 V unless otherwise noted.)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
DYNAMIC SELF−SUPPLY (All frequency versions, unless otherwise noted)						
V_{CC} Increasing Level at which the Current Source Turns Off	V_{CCOFF}	6	11.6	12.5	13.5 (Note 3)	V
V_{CC} Decreasing Level at which the Current Source Turns On	V_{CCON}	6	9.6	10.3	11.4 (Note 3)	V
V_{CC} Decreasing Level at which the Latch−off Phase Ends	$V_{CCLatch}$	6	–	5.6	–	V
Internal IC Consumption, No Output Load on Pin 6	ICC1	6	–	750	980 (Note 1)	μA
Internal IC Consumption, 1.0 nF Output Load on Pin 6, F_{SW} = 65 kHz	ICC2	6	–	1.6	1.9 (Note 2)	mA
Internal IC Consumption, Latch−off Phase	ICC3	6	–	600	–	μA
INTERNAL STARTUP CURRENT SOURCE (T_J > −5°C)						
High Voltage Current Source, V_{CC} = 10 V	IC1	8	5.2 (Note 4)	8.0	9.5	mA
High Voltage Current Source, V_{CC} = 0	IC2	8	–	15	–	mA
DRIVE OUTPUT						
Output Voltage Rise−time @ CL = 1.0 nF, 10−90% of Output Signal	T_r	5	–	40	–	ns
Output Voltage Fall−time @ CL = 1.0 nF, 10−90% of Output Signal	T_f	5	–	20	–	ns
Source Resistance	R_{OH}	5	15	20	35	Ω
Sink Resistance	R_{OL}	5	5.0	10	18	Ω
CURRENT COMPARATOR (Pin 5 unloaded)						
Input Bias Current @ 1.0 V Input Level on Pin 3	I_{IB}	3	–	0.02	–	μA
Maximum Internal Current Setpoint	I_{Limit}	3	0.95	1.0	1.1	V
Default Internal Current Setpoint for Skip Cycle Operation	I_{Lskip}	3	–	370	–	mV
Propagation Delay from Current Detection to Gate OFF State	T_{DEL}	3	–	90	150	ns
Leading Edge Blanking Duration	T_{LEB}	3	–	350	–	ns
INTERNAL OSCILLATOR (V_{CC} = 11 V, pin 5 loaded by 1.0 kΩ)						
Oscillation Frequency, 65 kHz Version	f_{OSC}	–	58.5	65	71.5	kHz
Built−in Frequency Jittering, F_{SW} = 65 kHz	f_{jitter}	–	–	±3.0	–	kHz
Maximum Duty Cycle	D_{MAX}	–	74	80	87	%
FEEDBACK SECTION (V_{CC} = 11 V, pin 5 loaded by 1.0 kΩ)						
Internal Pull−up Resistor	R_{up}	2.0	–	20	–	kΩ
Pin 3 to Current Setpoint Division Ratio	I_{ratio}	–	–	3.3	–	–
Internal Soft−Start (Guaranteed by Design)	T_{SS}	–	0.6	1.0	–	ms
SKIP CYCLE GENERATION						
Default Skip Mode Level	V_{skip}	1	1.03	1.2	1.35	V
Pin 1 Internal Output Impedance	Z_{out}	1	–	25	–	kΩ
INTERNAL RAMP COMPENSATION						
Internal Ramp Level @ 25°C (Note 5)	V_{ramp}	3	2.0	2.2	2.5	V
Internal Ramp Resistance to CS Pin	R_{ramp}	3	–	19	–	kΩ
AdjUSTMENT LATCHOFF LEVEL						
Latching Level	V_{latch}	1	2.9	3.22	3.55	V

1. Maximum value at T_J = −5°C.
2. Maximum value @ T_J = 25°C, please see characterization curves.
3. V_{CC}OFF and V_{CC}ON min−max always ensure a hysteresis of 2.0 V.
4. Minimum value for T_J = 125°C.
5. A 20 kΩ resistor is connected to the ground for the measurement.

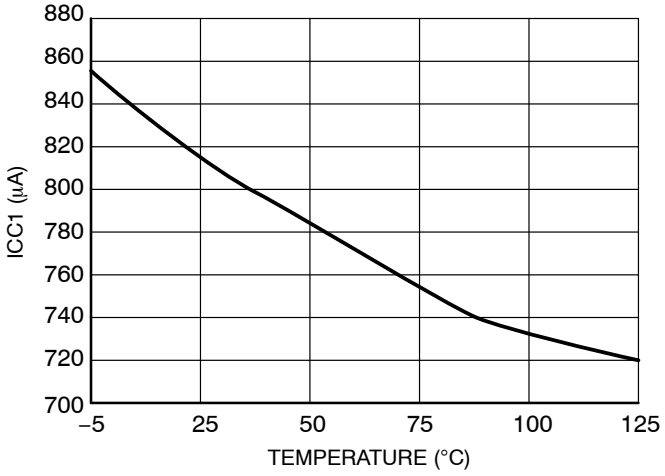


Figure 3. No Load Current Consumption vs. Temperature

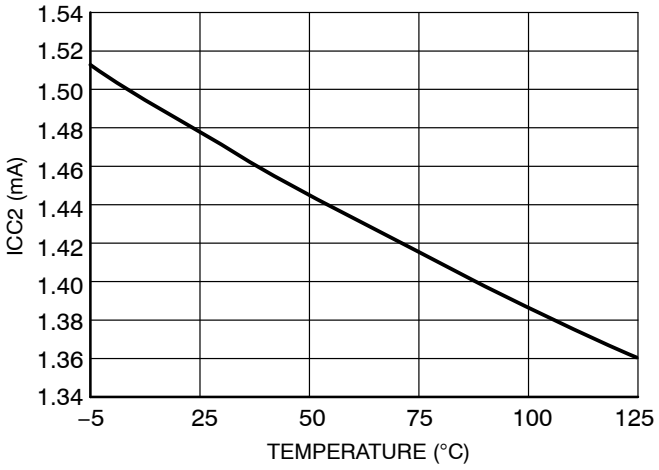


Figure 4. 1.0 nF Load Current Consumption vs. Temperature

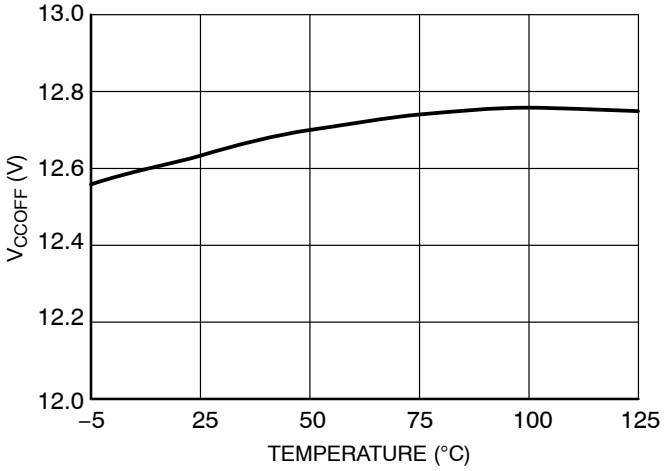


Figure 5. V_{CCOFF} Level Variation vs. Temperature

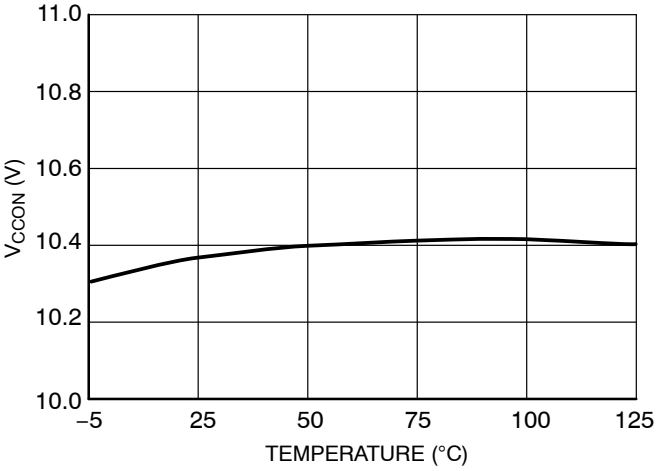


Figure 6. V_{CCON} Level Variation vs. Temperature

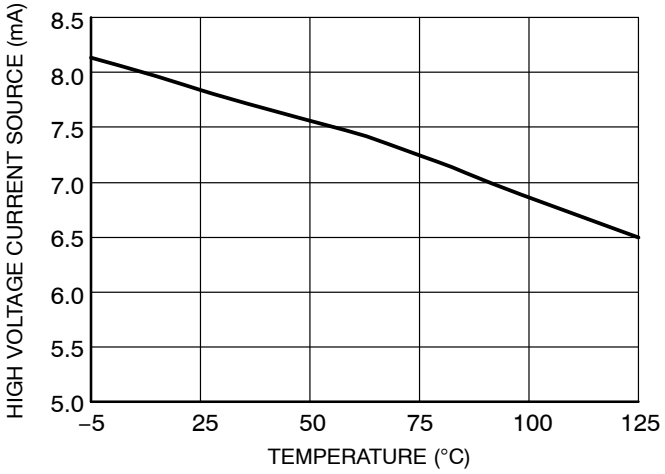


Figure 7. Startup Current Evolution with Junction Temperature

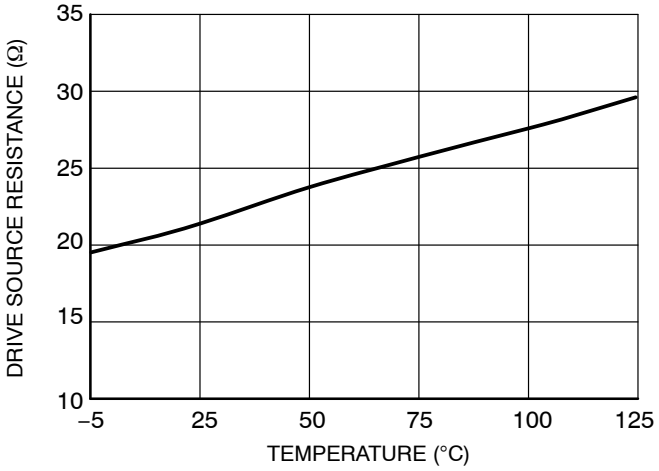


Figure 8. Drive Output Impedance Behavior with Junction Temperature

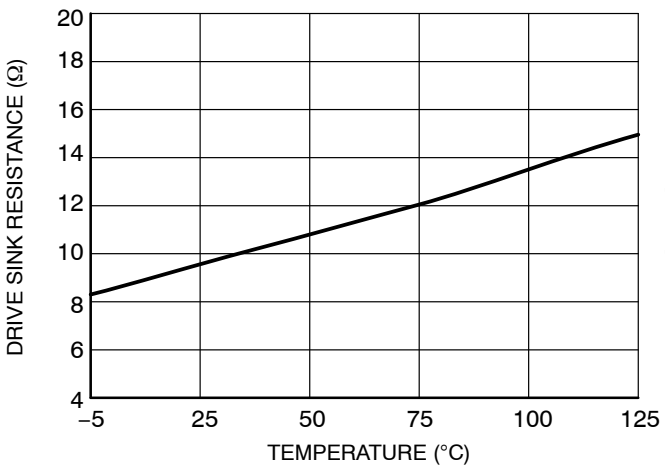


Figure 9. Drive Output Impedance Behaviour with Junction Temperature

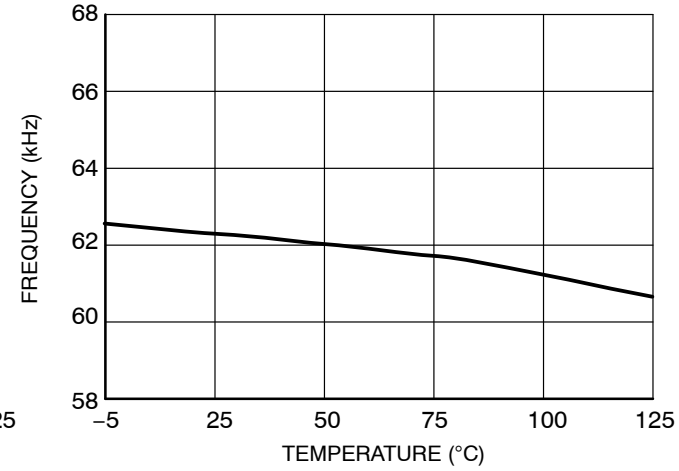


Figure 10. Switching Frequency Behaviour with Junction Temperature

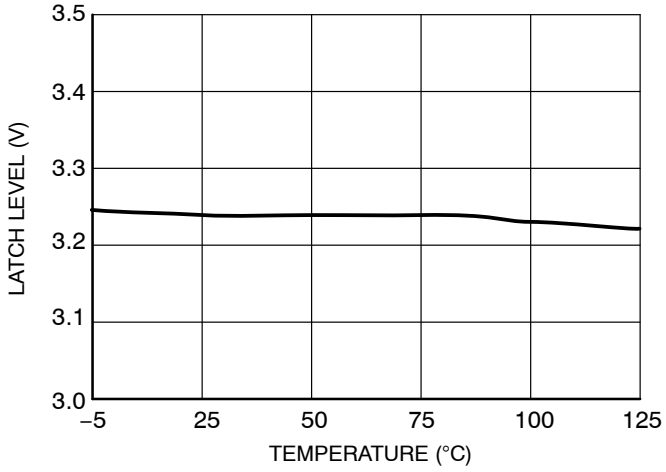


Figure 11. Latch−off Level Evolution with Junction Temperature

APPLICATION INFORMATION

Introduction

The DAP008 implements a standard current mode architecture where the switch−off time is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count is the key parameter, particularly in low−cost AC/DC adapters, auxiliary supplies etc. Due to its high−performance High−Voltage technology, the DAP008 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low−pass filter and self−supply. This later point emphasizes the fact that ON Semiconductor's DAP008 does NOT need an auxiliary winding to operate: the product is naturally supplied from the high−voltage rail and delivers a V_{CC} to the IC. This system is called the Dynamic Self−Supply (DSS).

Dynamic Self−Supply

The DSS principle is based on the charge/discharge of the V_{CC} bulk capacitor from a low level up to a higher level. We can easily describe the current source operation with a bunch of simple logical equations:

POWER−ON: IF V_{CC} < VCC_H THEN Current Source is ON, no output pulses

IF V_{CC} decreasing > VCC_L THEN Current Source is OFF, output is pulsing

IF V_{CC} increasing < VCC_H THEN Current Source is ON, output is pulsing

Typical values are: VCC_H = 12 V, VCC_L = 10 V

To better understand the operational principle, Figure 12's sketch offers the necessary light:

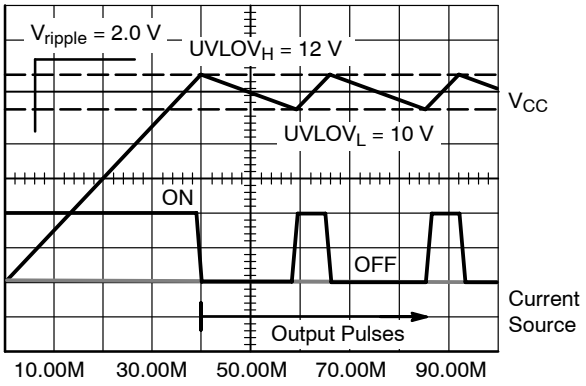


Figure 12. The Charge/Discharge Cycle Over a 10 μF V_{CC} Capacitor

The DSS behavior actually depends on the internal IC consumption and the MOSFET's gate charge Qg. If we select a MOSFET like the MTP6N60E, Qg equals 25 nC (typ). With a maximum switching frequency of 72 kHz, the average power necessary to drive the MOSFET (excluding the driver efficiency and neglecting various voltage drops) is: $F_{SW} \cdot Qg \cdot V_{CC}$ with:

F_{SW} = Maximum Switching Frequency
Qg = MOSFET's Gate Charge
$V_{CC} = V_{GS}$ Level Applied to the Gate

To obtain the final IC current, simply divide this result by V_{CC}: $I_{driver} = F_{SW} \cdot Qg \cdot = 1.8$ mA. The total standby power consumption at no−load will therefore heavily rely on the internal IC consumption plus the above driving current (altered by the driver's efficiency). Suppose that the IC is supplied from a 350 VDC line. The current flowing through pin 8 is a direct image of the DAP008 consumption (neglecting the switching losses of the HV current source). If ICC2 equals 2.5 mA @ T_J = 25°C, then the power dissipated (lost) by the IC is simply: 350 x 2.5 m = 875 mW. For design and reliability reasons, it would be interested to reduce this source of wasted power which increases the die temperature. This can be achieved by using different methods:

3. Use a MOSFET with lower gate charge Qg
4. Connect pin through a diode (1N4007 typically) to one of the mains input. The average value on pin 8 becomes $\frac{VmainSPEAK \cdot 2}{\pi}$.
   Our power contribution example drops to: 223 x 2.5 m = 557 mW. If a resistor is installed between the mains and the diode, you further force the dissipation to migrate from the package to the resistor. The resistor value should account for low−line startups.

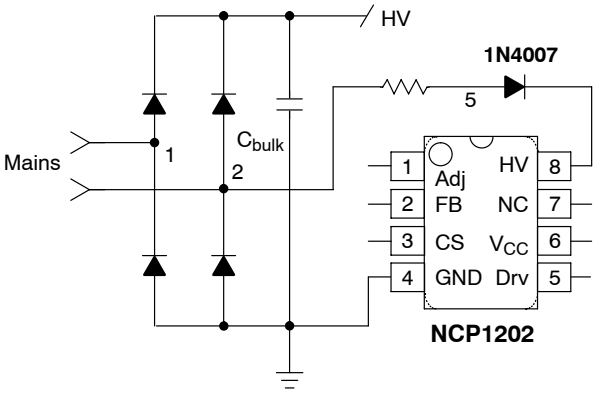


Figure 13. A Simple Diode Naturally Reduces the Average Voltage on Pin 8

5. Permanently force the V_{CC} level above VCC_H with an auxiliary winding. It will automatically disconnect the internal startup source and the IC will be fully self−supplied from this winding. Again, the total power drawn from the mains will significantly decrease. Make sure the auxiliary voltage never exceeds the 16 V limit.

Ramp Compensation

Ramp compensation is a known mean to cure subharmonic oscillations. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty−cycle greater than 50%. To lower the current loop gain, one usually injects between 50 and 100% of the inductor downslope. Figure 14 depicts how internally the ramp is generated:

In the DAP008, the ramp features a swing of 2.0 V. Over a 65 kHz frequency, it corresponds to a 130 mV/μs ramp. In our FLYBACK design, let's suppose that our primary inductance Lp is 350 μH, delivering 12 V with a Np:Ns ratio of 1:0.1. The OFF time primary current slope is thus given by: $\frac{(Vout + Vf)\cdot\frac{Ns}{Np}}{Lp} = 371\ mA/\mu s$ or 37 mV/μs when projected over an R_{sense} of 0.1 Ω, for instance. If we select 75% of the downslope as the required amount of ramp compensation, then we shall inject 27 mV/μs. Our internal compensation being of 130 mV, the divider ratio (*divratio*) between R_{comp} and the 19 kΩ is 0.207. A few lines of algebra to determine R_{comp}: $Rcomp = \frac{19\ k\cdot divratio}{(1 - divratio)} = 4.95\ k\Omega$.

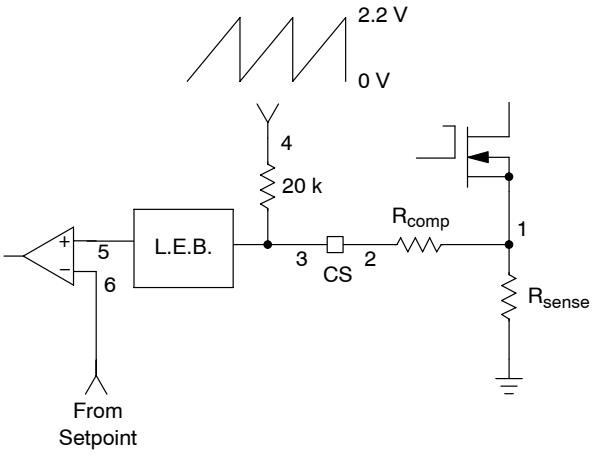


Figure 14. Inserting a Resistor in Series with the Current Sense Information brings Ramp Compensation

Frequency Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. *Maximus* offers a ±3.0 kHz frequency jittering whose sweep is synchronized with the V_{CC} ripple. With a 2.0 V peak−to−peak ripple, the frequency will equal 65 kHz in the middle of the ripple and will increase as V_{CC} rises or decrease as V_{CC} ramps down. Figure 15 portrays the behavior we have adopted:

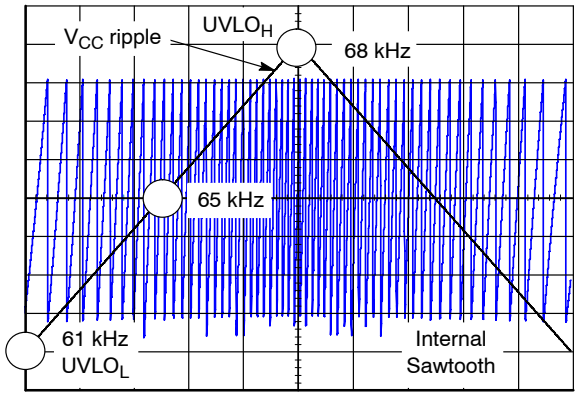


Figure 15. The V_{CC} Ripple is used to Introduce a Frequency Jittering on the Internal Oscillator Sawtooth

Skipping Cycle Mode

The DAP008 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so−called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 17). Suppose we have the following component values:

Lp, Primary Inductance = 350 μH

F_{SW}, Switching Frequency = 65 kHz

Ip Skip = 600 mA (or 333 mV/R_{sense})

The theoretical power transfer is therefore: $\frac{1}{2} \cdot Lp \cdot Ip^2 \cdot F_{SW} = 4.0$ W.

If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is: 2.2. 0.1 = 400 mW.

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight:

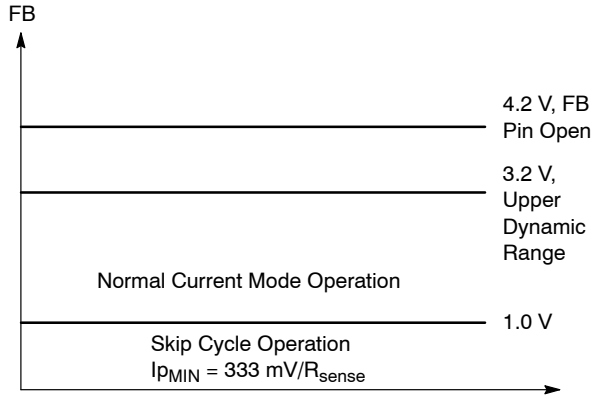


Figure 16. Operation Mode vs. FB Level

When FB is above the skip cycle threshold (1.0 V by default), the peak current cannot exceed 1.0 V/R_{sense}. When the IC enters the skip cycle mode, the peak current cannot go below Vpin1/3.3. The user still has the flexibility to alter this 1.0 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level. In this later case, care must be taken to keep sufficient margin between this pin 1 adjustment level and the latch−off level. Grounding pin 1 permanently invalidates the skip cycle operation.

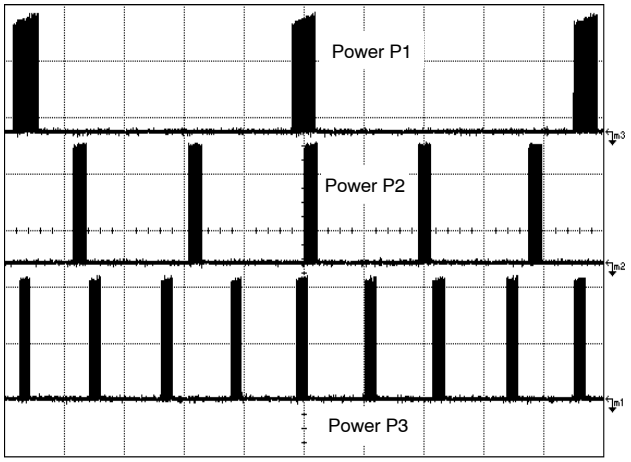


Figure 17. Output Pulses at Various Power Levels (X = 5.0 μs/div) P1 < P2 < P3

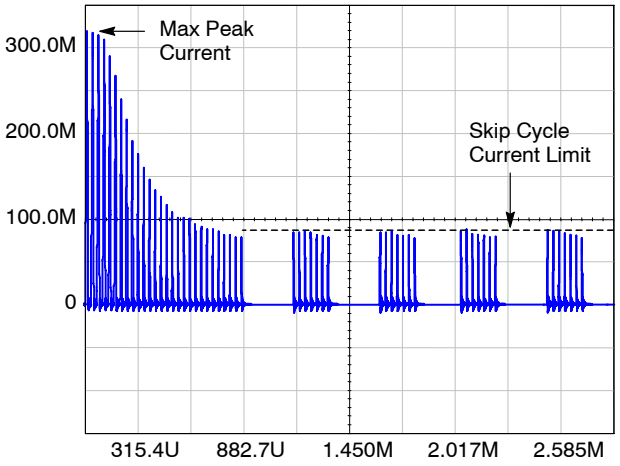


Figure 18. The Skip Cycle Takes Place at Low Peak Currents Which Guarantees Noise−Free Operation

We recommend a Pin 1 operation between 400 mV and 1.3 V that will fix the skip peak current level between 120 mV/R_{sense} and 390 mV/R_{sense}.

Latching Off the DAP008

Total latched shutdown can easily be implemented through a simple PNP bipolar transistor as depicted by Figure 19. When OFF, Q1 is transparent to the operation. When forward biased, the transistor pulls the Adj pin toward V_{CC} and permanently latches−off the IC as soon V_{adj} goes above the latching level (typical 3.2 V). Figure 19 shows how to wire the bipolar transistor to activate the latch−off. A typical candidate for Q1 could be an MMBT3906 from ON Semiconductor.

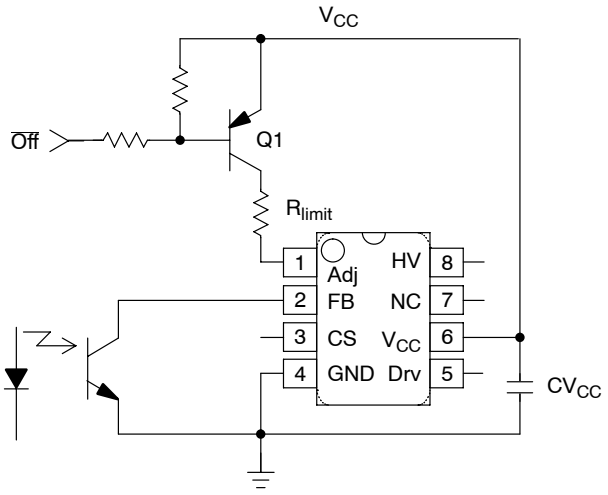


Figure 19. A Simple Bipolar Transistor Totally Disables the IC

In normal operation, the Adj pin level is kept at a fixed level, the default one or lower. As soon as some external signal pulls this Adj pin level above 3.2 V typical, the output pulses are permanently disabled. Care must be taken to limit the injected current into pin 1 to less than 2.0 mA, e.g. through a series resistor of 5.6 k with a 10 V V_{CC}. The DSS is still working and maintains the output low. The reset occurs when the mains disappears, e.g. when the user unplugs the power supply from the wall outlet. Figure 21 illustrates the operation with DSS.

Non−Latching Shutdown

In some cases, it might be desirable to shut off the part temporarily and authorize its restart once the default has disappeared. This option can easily be accomplished through a single NPN bipolar transistor wired between FB and ground. By pulling FB below the Adj pin 1 level, the output pulses are disabled as long as FB is pulled below pin 1. As soon as FB is relaxed, the IC resumes its operation. Figure 20 depicts the application example:

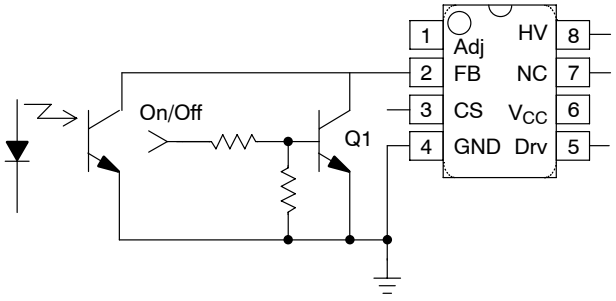


Figure 20. Another Way of Shutting Down the IC Without a Definitive Latch−Off State

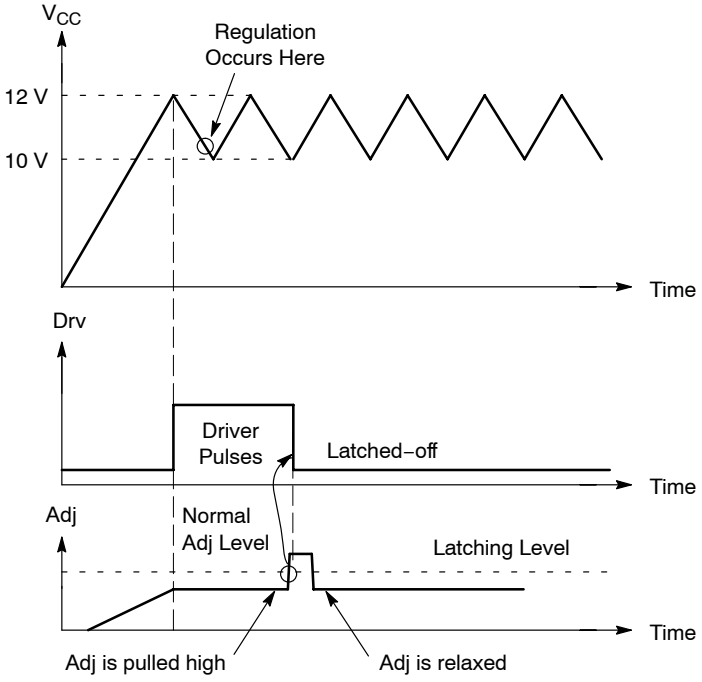


Figure 21. When V_{adj} is Pulled Above 3.2 V, DAP008 Permanently Latches−Off the Output Pulses

Soft−Start

The DAP008 features an internal 1ms soft−start activated during the power on sequence (PON). As soon as V_{CC} reaches VCC_{OFF} , the peak current is gradually increased from nearly zero up to the maximum clamping level (e.g. 1.0 V). This situation lasts during 1ms and further to that time period, the peak current limit is blocked to 1.0 V until the supply enters regulation. The soft−start is also activated during the over current burst (OCP) sequence. Every restart attempt is followed by a soft−start activation. Generally speaking, the soft−start will be activated when V_{CC} ramps up either from zero (fresh power−on sequence) or 6.0 V, the latch−off voltage occurring during OCP. Figure 22 portrays the soft−start behavior. The time scales are purposely shifted to offer a better zoom portion.

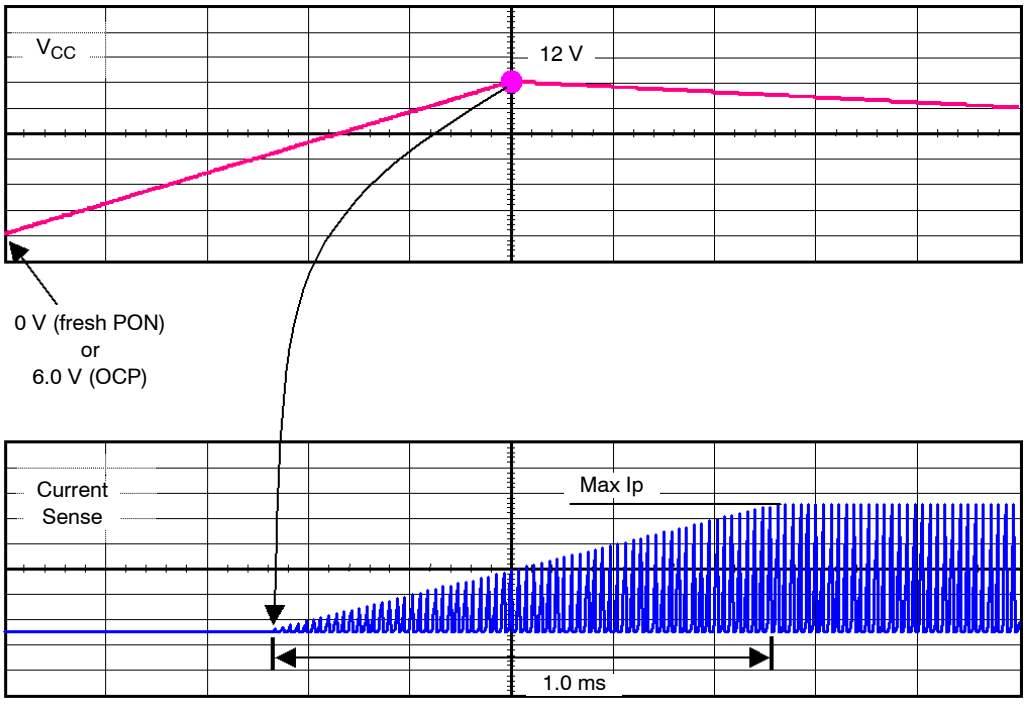


Figure 22. Soft−Start is Activated During a Startup Sequence or an OCP Condition

Power Dissipation

The DAP008 is directly supplied from the DC rail through the internal DSS circuitry. The current flowing through the DSS is therefore the direct image of the DAP008 current consumption. The total power dissipation can be evaluated using: $(V_{HVDC} - 11\ V) \cdot ICC2$. If we operate the device on a 250 VAC rail, the maximum rectified voltage can go up to 350 VDC. However, as the characterization curves show, the current consumption drops at high junction temperature, which quickly occurs due to the DSS operation. At T_J = 50°C, ICC2 = 1.7 mA. As a result, the DAP008 will dissipate 350 . 1.7 mA @ T_J = 50°C = 595 mW. The SO−8 package offers a junction−to−ambient thermal resistance $R_{\theta JA}$ of 178°C/W. Adding some copper area around the PCB footprint will help decreasing this number: 12 mm x 12 mm to drop $R_{\theta JA}$ down to 100°C/W with 35 μ copper thickness (1 oz.) or 6.5 mm x 6.5 mm with 70 μ copper thickness (2 oz.). With this later number, we can compute the maximum power dissipation the package accepts at an ambient of 50°C:

$$P_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{R_{\theta JA}} = 750\ mW$$

Which is okay with our previous budget. However, ICC2 is based on a 1.0 nF output capacitor. As seen before, ICC2 will depend on your MOSFET's Qg: $ICC2 \approx ICC1 + F_{SW} \times Qg$. Final calculation shall thus accounts for the total gate−charge Qg your MOSFET will exhibit.

If the power estimation is finally beyond the limit, other solutions are possible: a) add a series diode with pin 8 (as suggested in the above lines) to drop the average input voltage and lower the dissipation to:

$$\frac{350 \cdot 2}{\pi} \cdot 1.7\ m = 380\ mW$$

b) put an auxiliary winding to disable the DSS and decrease the power consumption to V_{CC} x ICC2. The auxiliary level should be thus that the rectified auxiliary voltage permanently stays above 10 V (to not reactivate the DSS) and is safely kept below the 16 V maximum rating.

Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short−circuit protection. A short−circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the FB pin level is pulled up to 4.2 V, as internally imposed by the IC. The peak current setpoint goes to the maximum and the supply delivers a rather high power with all the associated effects. Please note that this can also happen in case of feedback loss, e.g. a broken optocoupler. To account for this situation, DAP008 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty−cycle. The system auto−recovers when the fault condition disappears.

During the startup phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. This period of time depends on normal output load conditions and the maximum peak current allowed by the system. The time−out used by this IC works with the V_{CC} decoupling capacitor: as soon as the V_{CC} decreases from the $UVLO_H$ level (typically 12 V) the device internally watches for an overload current situation. If this condition is still present when the $UVLO_L$ level is reached, the controller stops the driving pulses, prevents the self−supply current source to restart and puts all the circuitry in standby, consuming as little as 350 μA typical (ICC3 parameter). As a result, the V_{CC} level slowly discharges toward 0. When this level crosses 6.0 V typical, the controller enters a new startup phase by turning the current source on: V_{CC} rises toward 12 V and again delivers output pulses at the $UVLO_H$ crossing point. If the fault condition has been removed before $UVLO_L$ approaches, then the IC continues its normal operation. Otherwise, a new fault cycle takes place. Figure 23 shows the evolution of the signals in presence of a fault.

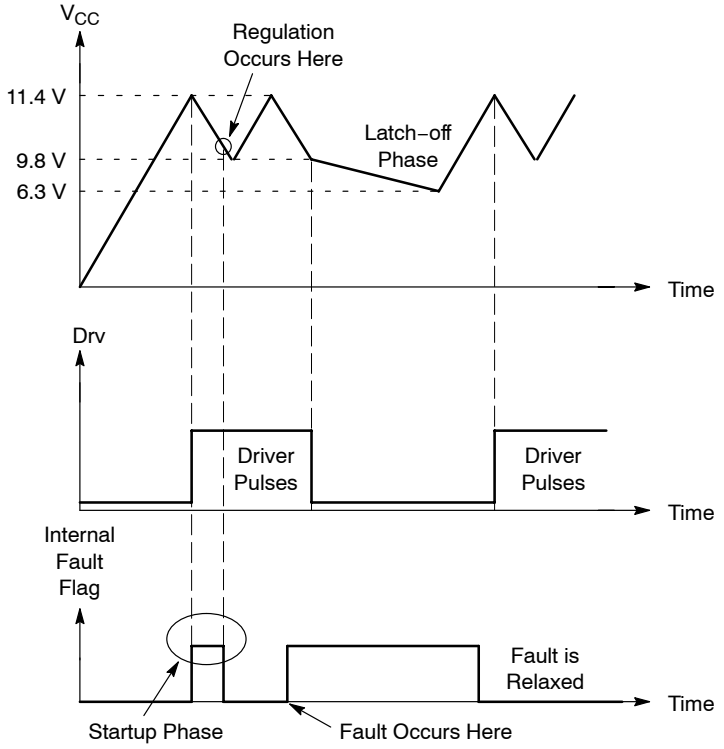


Figure 23. If the fault is relaxed during the V_{CC} natural fall down sequence, the IC automatically resumes. If the fault persists when V_{CC} reached $UVLO_L$, then the controller cuts everything off until recovery.

Calculating the V_{CC} Capacitor

As the above section describes, the fall down sequence depends upon the V_{CC} level: how long does it take for the V_{CC} line to go from 12 V to 10 V? The required time depends on the startup sequence of your system, i.e. when you first apply the power to the IC. The corresponding transient fault duration due to the output capacitor charging must be less than the time needed to discharge from 12 V to 10 V, otherwise the supply will not properly start. The test consists in either simulating or measuring in the lab how much time the system takes to reach the regulation at full load. Let's suppose that this time corresponds to 6.0 ms. Therefore a V_{CC} fall time of 10 ms could be well appropriated in order to not trigger the overload detection circuitry. If the corresponding IC consumption, including the MOSFET drive, establishes at 1.8 mA (**TBD**), we can calculate the required capacitor using the following formula:

$$\Delta t = \frac{\Delta V \cdot C}{i}, \text{with } \Delta V = 2.0 \text{ V}$$

Then for a wanted Δt of 10 ms, C equals 9.0 μF or 10 μF for a standard value. When an overload condition occurs, the IC blocks its internal circuitry and its consumption drops to 350 μA typical. This happens at V_{CC} = 10 V and it remains stuck until V_{CC} reaches 6.0 V: we are in latch−off phase. Again, using the calculated 10 μF and 350 μA current consumption, this latch−off phase lasts: 109 ms.

ORDERING INFORMATION

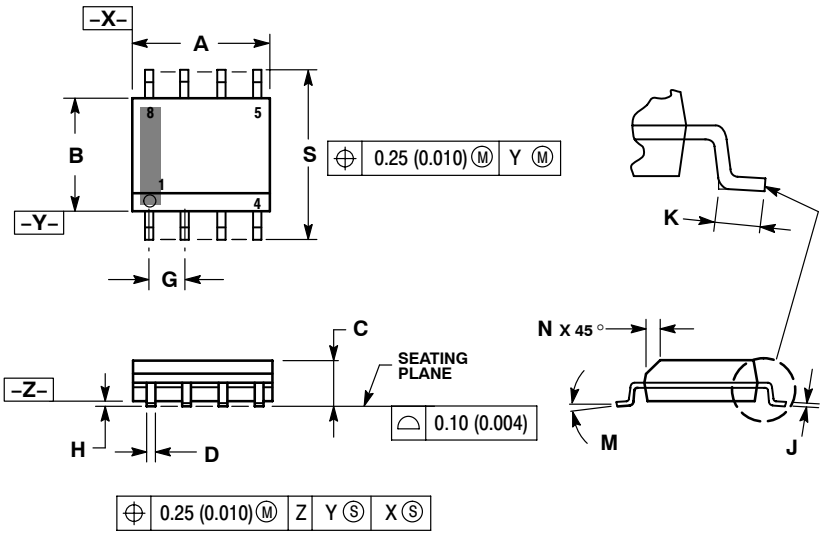
Device	Operating Temperature Range	Package	Shipping†
SCY99008R2	T_J = −5°C to 125°C	SO−8	2500 / Tape and Reel
SCY99008R2G	T_J = −5°C to 125°C	SO−8 (Pb−Free)	2500 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DAP008 Maximus

PACKAGE DIMENSIONS

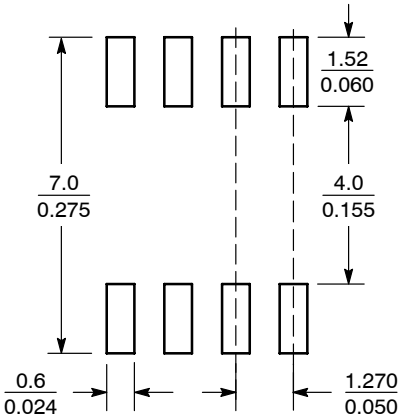
SOIC−8 NB
CASE 751−07
ISSUE AG



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The product described herein (DAP008), may be covered by the following U.S. patent: 6,385,060. There may be other patents pending.

PUBLICATION ORDERING INFORMATION

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