3A Bus Termination Regulator

Features

- Provide Bi-direction Current
  - Sourcing or Sinking Current up to 3A
- 1.25V/0.9V Output for DDR I/II Applications
- Fast Transient Response
- High Output Accuracy
  - ±20mV over Load, VOUT Offset and Temperature
- Adjustable Output Voltage by External Resistors
- Current-Limit Protection
- On-Chip Thermal Shutdown
- Shutdown for Standby or Suspend Mode
- Simple SOP-8, SOP-8-P with thermal pad, TO-252- 5 and TO-263-5 Packages

Applications

- DDR I/II SDRAM Termination
- SSTL-2/3 Termination Voltage
- Applications Requiring the Regulator with Bi-direction 3A Current Capability

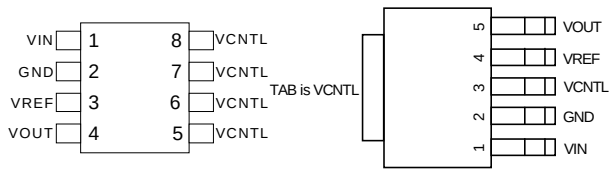
General Description

The APL5331 linear regulator is designed to provide a regulated voltage with bi-directional output current for DDR-SDRAM termination. The APL5331 integrates two power transistors to source or sink current up to 3A. It also incorporate current-limit, thermal shutdown and shutdown control functions into a single chip. Current-limit circuit limits the short-circuit current.

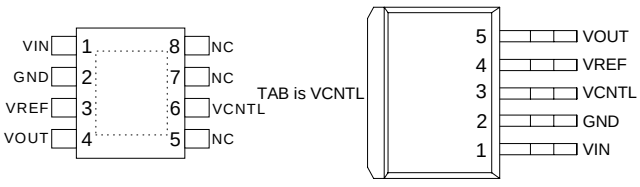
General Description (Cont.)

On-chip thermal shutdown provides protection against any combination of overload that would create excessive junction temperature. The output voltage of APL5331 track the voltage at VREF pin. A resistor divider connected to VIN, GND and VREF pins is used to provide a half voltage of VIN to VREF pin. In addition, an external ceramic capacitor and an open-drain transistor connected to VREF pin provides soft-start and shutdown control respectively. Pulling and holding the VREF to GND shuts off the output. The output of APL5331 will be high impedance after being shut down by VREF or thermal shutdown function.

Pin Configuration



SOP-8 (Top View) TO-252-5 (Top View)



SOP-8-P (Top View) TO-263-5 (Top View)

NC = No internal connection

= Thermal Pad (connected to GND plane for better heat dissipation)

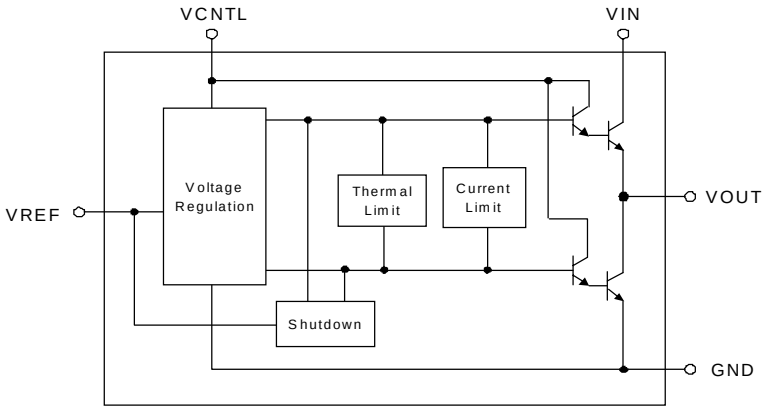
Ordering and Marking Information

APL5331 □□□-□□□ Lead Free Code Handling Code Temp. Range Package Code	Package Code K : SOP-8 KA : SOP-8-P U5 : TO-252-5 G5 : TO-263-5 Temp. Range C : 0 to 70 °C Handling Code TR : Tape & Reel Lead Free Code L : Lead Free Device Blank : Orginal Device
APL5331KC-TR : APL5331KAC-TR :	APL5331 XXXXX XXXXX - Date Code
APL5331U5C-TR : APL5331G5C-TR :	APL5331 XXXXX XXXXX - Date Code

Pin Description

PIN NAME	I/O	DESCRIPTION
VIN	I	Main power input pin. Connect this pin to a voltage source and an input capacitor. The APL5331 sources current to VOUT pin by controlling the upper NPN pass transistor, providing a current path from VIN pin.
GND	O	Power and signal ground. Connect this pin to system ground plane with shortest traces. The APL5331 sinks current from VOUT pin by controlling the lower NPN pass transistor, providing a current path to GND pin. This pin is also the ground path for internal control circuitry.
VCNTL	I	Power input pin for internal control circuitry. Connect this pin to a voltage source, providing a bias for the internal control circuitry. A bypass capacitor is usually connected near this pin.
VREF	I	Reference voltage input and active-low shutdown control pin. Apply a voltage to this pin as a reference voltage for the APL5331. Connect this pin to a resistor divider, between VIN and GND, and a capacitor for soft-start and filtering noise purposes. Applying and holding this pin low by an open-drain transistor to shut down the output.
VOUT	O	Output pin of the regulator. Connect this pin to load. Output capacitors connected this pin improves stability and transient response. The output voltage tracks the reference voltage and is capable of sourcing or sinking current up to 3A.

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CNTL}	VCNTL Supply Voltage, VCNTL to GND	-0.2 ~ 7	V
V_{IN}	VIN Supply Voltage, VIN to GND	-0.2 ~ 3.9	V
P_D	Power Dissipation	Internally Limited	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Soldering Temperature, 10 Seconds	300	°C
V_{ESD}	Minimum ESD Rating (Human Body Mode)	±3	kV

Thermal Characteristics

Symbol	Parameter	Rating	Unit
θ_{JA}	Thermal Resistance in Free Air		
	SOP-8	160	°C/W
	SOP-8-P	80	
	TO-252-5	80	
	TO-263-5	50	

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{CNTL}	VCNTL Supply Voltage	3.1 ~ 6V	V
V_{IN}	VIN Supply Voltage	1.6 ~ 3.5	V
V_{REF}	VREF Input Voltage	0.8 ~ 1.75	V
I_{OUT}	VOUT Output Current (Note1, 2)	-3 ~ +3	A
T_J	Junction Temperature	0 ~ 125	°C

Note1 : The symbol “+” means the VOUT sources current to load; the symbol “-“ means the VOUT sinks current to GND.

Note2 : The max. I_{OUT} varies with the T_J. Please refer to the typical characteristics.

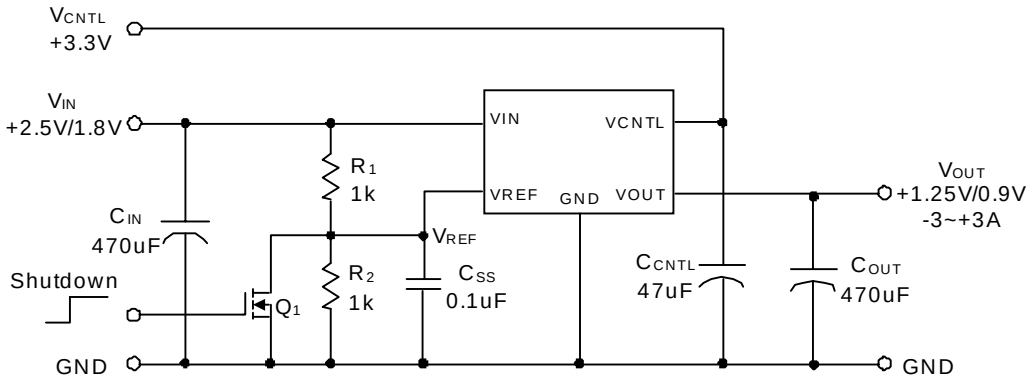
Electrical Characteristics

Refer to the typical application circuit. These specifications apply over, V_{CNTL}=3.3V, V_{IN}=2.5V/1.8V, V_{REF}=0.5V_{IN} and T_J= 0 to 125°C, unless otherwise specified. Typical values refer to T_J =25°C.

Symbol	Parameter	Test Conditions	APL5331			Unit
			Min	Typ	Max	
Output Voltage						
V_{OUT}	VOUT Output Voltage	I_{OUT}=0A		V_{REF}		V
	System Accuracy	Over temperature, VOUT offset, and load regulation	-20		20	mV
V_{OS}	VOUT Offset Voltage (V_{OUT}–V_{REF})	I_{OUT}=+10mA	-14	-9		mV
		I_{OUT}=-10mA		2	8	
	Load Regulation	I_{OUT}=+10mA to +3A	-6	-3		mV
		I_{OUT} = -10mA to -3A		7	12	
Protection						
I_{LIM}	Current Limit	Sourcing Current (V_{IN}=2.5V) T_J=25°C	+3.3	+3.6		A
		Sourcing Current (V_{IN}=2.5V) T_J=125°C		+3.1		
		Sinking Current (V_{IN}=2.5V) T_J=25°C	-3.3	-3.6		
		Sinking Current (V_{IN}=2.5V) T_J=125°C		-3.1		
		Sourcing Current (V_{IN}=1.8V) T_J=25°C	+2.9	+3.2		
		Sourcing Current (V_{IN}=1.8V) T_J=125°C		+2.6		
		Sinking Current (V_{IN}=1.8V) T_J=25°C	-2.9	-3.2		
		Sinking Current (V_{IN}=1.8V) T_J=125°C		-2.6		
T_{SD}	Thermal Shutdown Temperature	Rising T_J		150		°C
	Thermal Shutdown Hysteresis			40		°C
Input Current						
I_{CNTL}	VCNTL Supply Current	I_{OUT}=0A	2	4.5	6	mA
		I_{OUT}=±3A (Normal Operation), V_{CNTL}=5V		50	110	
		V_{REF}=GND (Shutdown)		2.6		
I_{VREF}	VREF Bias Current (The current flows out of VREF)	V_{REF}=1.25V/0.9V (Normal Operation)		150	500	nA
		V_{REF}=GND (Shutdown)		20	40	µA
Shutdown Control						
	Shutdown Threshold Voltage		0.2	0.35	0.65	V

Typical Application Circuit

1. V_{OUT}=1.25V/0.9V Application



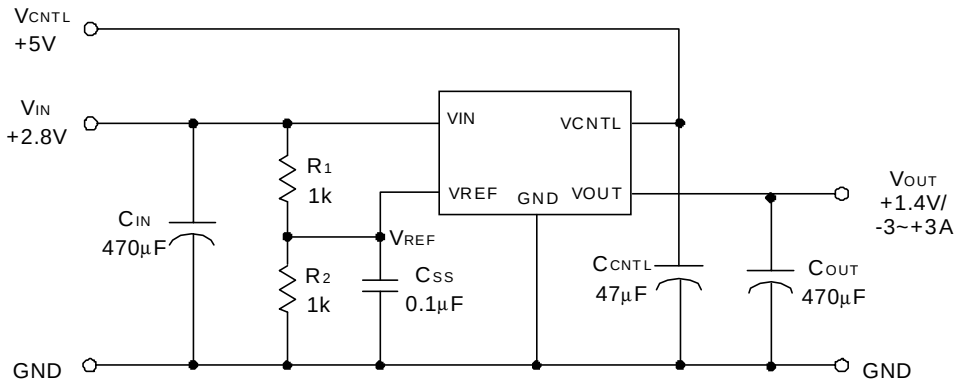
C_{OUT} : 470µF, ESR=25mΩ

R_1, R2 : 1kΩ, 1%

Q1 : APM2300 AC

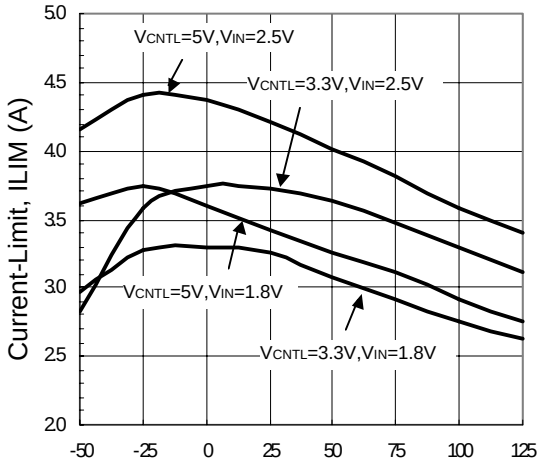
Note : Since R_1 and R_2 are very small, the voltage offset caused by the bias current of VREF can be ignore.

2. V_{OUT}=1.4V Application

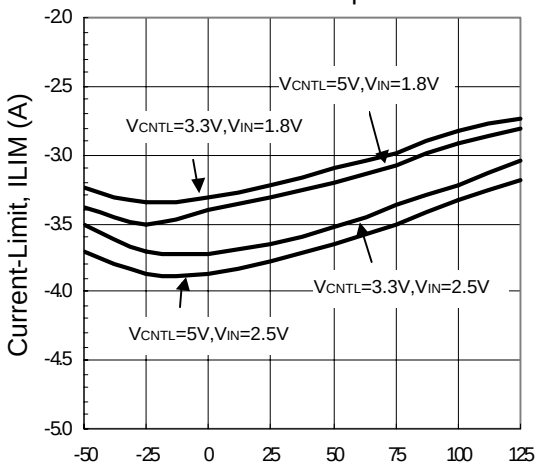


Typical Characteristics

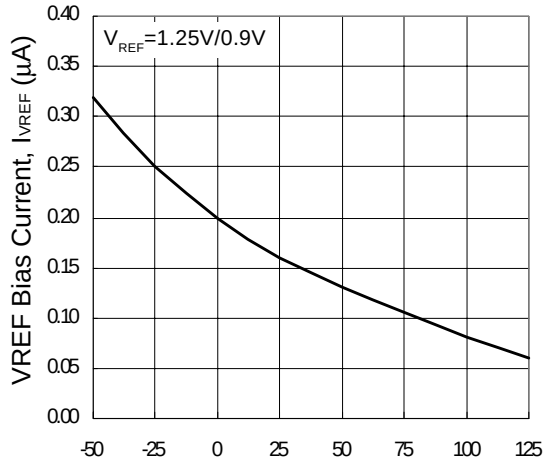
Sourcing Current-Limit
vs Junction Temperature



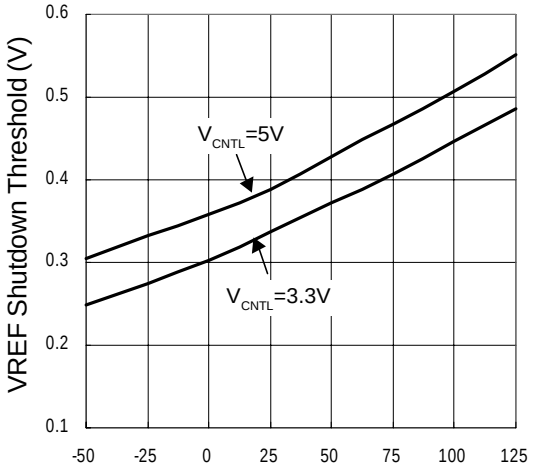
Sinking Current-Limit
vs Junction Temperature



VREF Bias Current
vs Junction Temperature

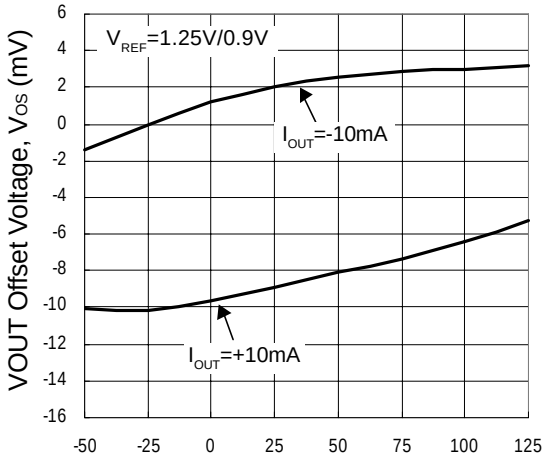


VREF Shutdown Threshold
vs Junction Temperature

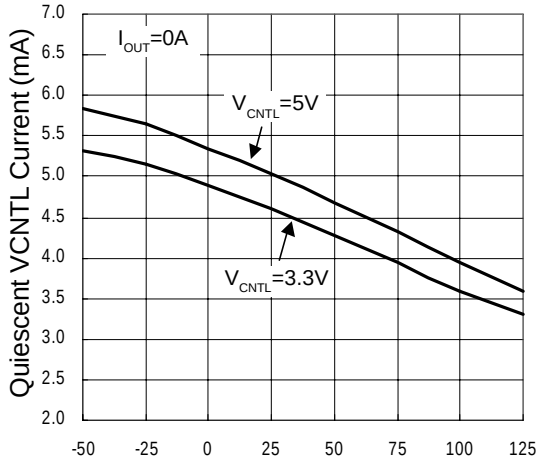


Typical Characteristics (Cont.)

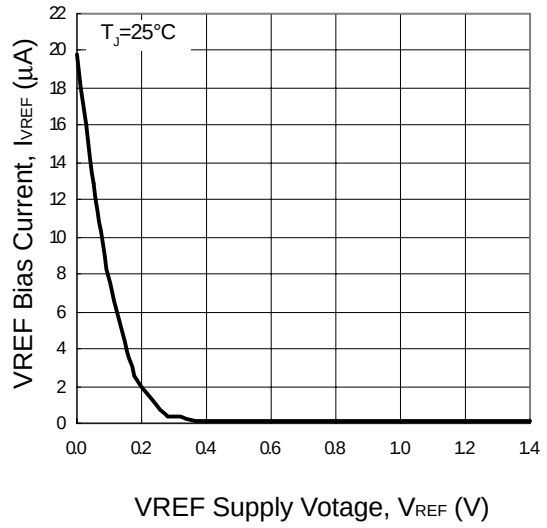
VOUT Offset Voltage
vs Junction Temperature



Quiescent VCNTL Current
vs Junction Temperature



VREF Bias Current
vs VREF Supply Voltage

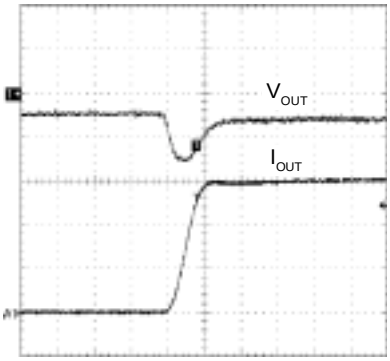


Operating Waveforms

1. Load Transient Response : I_{OUT} = +10mA -> +3A -> +10mA

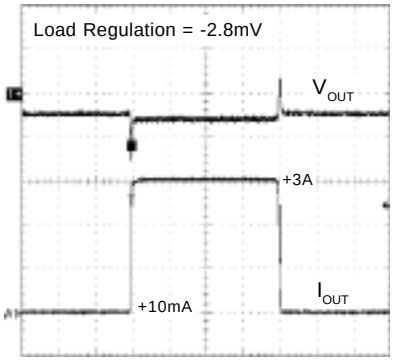
- V_{IN} = 2.5V, V_{CNTL} = 3.3V
- V_{REF} is 1.250V supplied by a regulator
- C_{OUT} = 470µF/10V, ESR = 30mΩ
- I_{OUT} slew rate = ±3A/µS

I_{OUT} = +10mA -> +3A



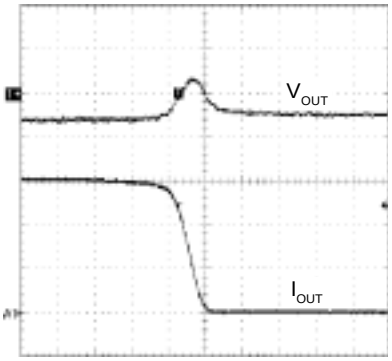
Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 1µS/Div

I_{OUT} = +10mA -> +3A -> +10mA



Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 20µS/Div

I_{OUT} = +3A -> +10mA

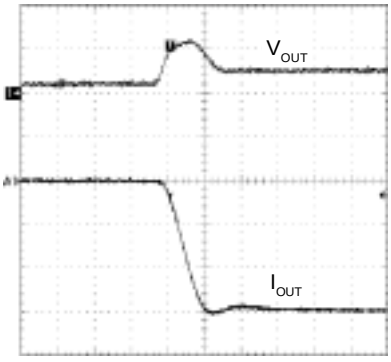


Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 1µS/Div

2. Load Transient Response : I_{OUT} = -10mA -> -3A -> -10mA

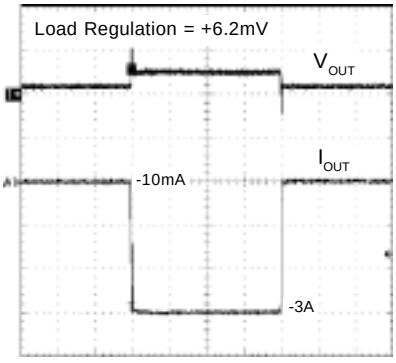
- V_{IN} = 2.5V, V_{CNTL} = 3.3V
- V_{REF} is 1.250V supplied by a regulator
- C_{OUT} = 470µF/10V, ESR = 30mΩ
- I_{OUT} slew rate = ±3A/µS

I_{OUT} = -10mA -> -3A



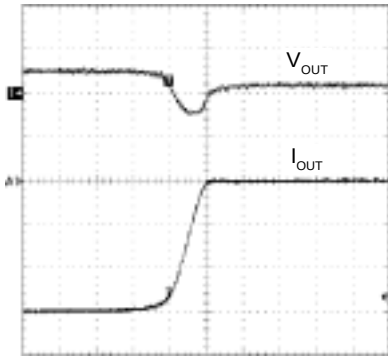
Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 1µS/Div

I_{OUT} = -10mA -> -3A -> -10mA



Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 20µS/Div

I_{OUT} = -3A -> -10mA



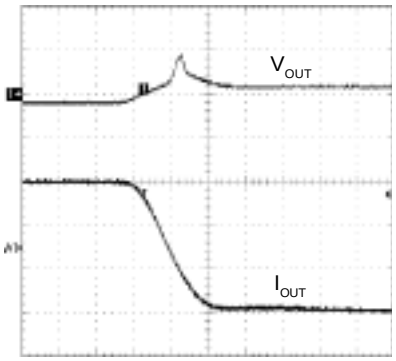
Ch1 : V_{OUT}, 20mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 1A/Div
Time : 1µS/Div

Operating Waveforms (Cont.)

3. Load Transient Response : I_{OUT} = +3A -> -3A -> +3A

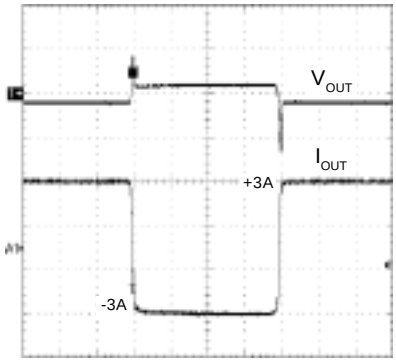
- V_{IN} = 2.5V, V_{CNTL} = 3.3V
- V_{REF} is 1.250V supplied by a regulator
- C_{OUT} = 470µF/10V, ESR = 30mΩ
- I_{OUT} slew rate = ±3A/µS

I_{OUT} = +3A -> -3A



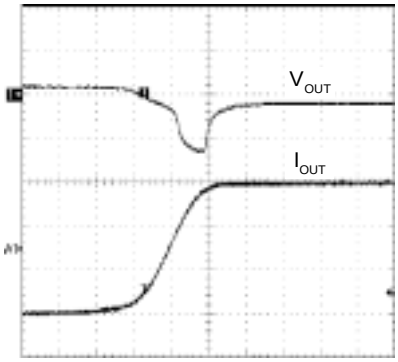
Ch1 : V_{OUT}, 50mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 2A/Div
Time : 1µS/Div

I_{OUT} = +3A -> -3A -> +3A



Ch1 : V_{OUT}, 50mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 2A/Div
Time : 20µS/Div

I_{OUT} = -3A -> +3A

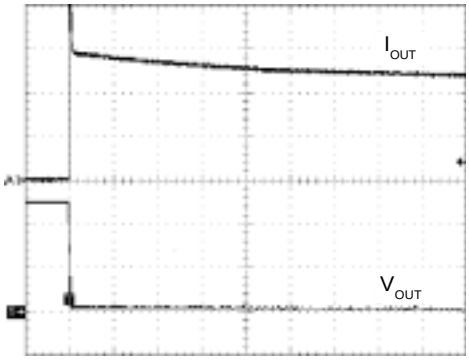


Ch1 : V_{OUT}, 50mV/Div, DC,
Offset = 1.250V
Ax1 : I_{OUT}, 2A/Div
Time : 1µS/Div

4. Short-Circuit Test

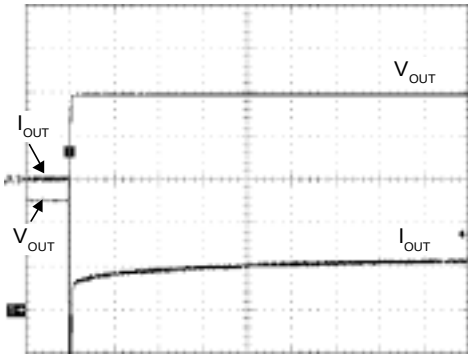
- V_{IN} = 2.5V, V_{CNTL} = 3.3V

V_{OUT} is Shorted to GND



Ch1 : V_{OUT}, 500mV/Div, DC,
Ax1 : I_{OUT}, 2A/Div
Time : 5mS/Div

V_{OUT} is Shorted to V_{IN} (2.5V)



Ch1 : V_{OUT}, 500mV/Div, DC,
Ax1 : I_{OUT}, 2A/Div
Time : 5mS/Div

Application Information

General

The APL5331 is a linear regulator and is capable of sourcing or sinking current up to 3A. The APL5331 has fast transient response, accurate output voltage (small voltage offset, load regulation), active-low shutdown control and fault protections (current-limit, thermal shutdown). The APL5331 is available in several packages to meet different of power dissipation in requirement various applications.

Output Voltage Regulation

The output voltage at VOUT pin tracks the reference voltage applied at VREF pin. Two internal NPN pass transistors controlled by separate high bandwidth error amplifiers regulate the output voltage by sourcing current from VIN pin or sinking current to GND pin. The base currents of the pass transistors are provided by VCNTL pin. An internal kelvin sensing scheme use at the VOUT pin for perfect load regulation at various load current. To prevent the two pass transistors from shoot-through, a small voltage offset is created between the positive inputs of the two error amplifiers. This results in higher output voltage while the regulator sinks light or heavy load current. Since the APL5331 exhibits very fast load transient response, lesser amount of capacitors can be use. In addition, capacitors with high ESR can also be use.

Current Limit

The APL5331 monitors sourcing and sinking current, and limits the maximum output current to prevent damages during overload or short-circuit, To increase the input voltage of VIN or VCNTL will get higher current-limit points.

Shutdown and Soft-Start

The VREF pin is a dual-function input pin, acting as reference input and shutdown control input. Applying and holding a voltage below 0.35V(typ.) to VREF pin shuts down the output of the regulator. An NPN transistor or N-channel MOSFET is used to pull down the VREF while applying a “high” signal to turn on the transistor. When shutdown function is active, the two pass transistors are turned off and the impedance of the VOUT is about 10MΩ (typ.), sourcing or sinking no current. When release the VREF pin, the current through the resistor divider charges the soft-start capacitor to initiate a soft-start cycle. The output voltage tracks the rising VREF. The soft start process limits the input surge current.

Thermal Shutdown

An thermal shutdown circuit limits the junction temperature of the APL5331. When the junction temperature exceeds T_J= +150°C, a thermal sensor turns off both pass transistors, allowing the device to cool down. The regulator starts to regulate again after the junction temperature reduces by 40°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal limit designed with a 40°C hysteresis lowers the average T_J during continuous thermal overload conditions, extend life time of APL5331.

Application Information

Power Inputs

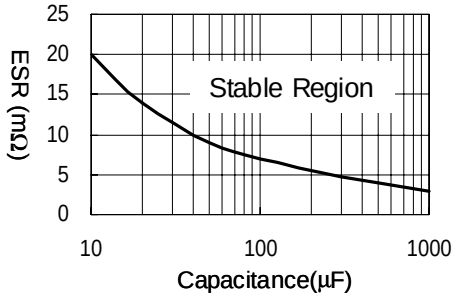
Input power sequence are not required for VIN and VCNTL. However, do not apply a voltage to VOUT when there is not voltage VCNTL. This is due to the internal parasitic diodes between VOUT to VIN and VOUT to VCNTL which will be forward bias. The APL5331 can source few current or sinks current up to 3A for load when the input Voltage at VIN is not present.

Reference Voltage

A reference voltage is applied at the VREF pin by a resistor divider between VIN and GND pins. Normally the bias current of the VREF pin flows out of the IC and is about 150nA(typ.), creating voltage offset at the resistor divider and affecting the output voltage accuracy. The recommended resistor is <5kΩ to maintain the accuracy of the output voltage. An external bypass capacitor is also connected to VREF. The capacitor and the resistor divider form a low-pass filter to reduce the inherent reference noise from VIN. A ceramic capacitor can be use and is selected to be greater than 0.1µF. Connected the capacitor as close to VREF as possible for optimal effect. More capacitance and large resistor divider will increase the soft-start interval. Do not place any additional loading on this reference input pin.

Output Capacitor

The APL5331 requires a proper output capacitor to maintain stability over full temperature and current ranges, and improve transient response. The output capacitor selection is dependent upon the ESR (equivalent series resistance) and capacitance of the output capacitor over full temperature range. The following chart shows the stable region of the output capacitor for APL5331. The stable region is above the curve, indicating minimum required ESR and capacitance to maintain stability. However, the output capacitor should have an ESR less than 1Ω.



Ultra-low-ESR capacitors, such as ceramic chip capacitors, may promote under-damped transient response, but proper ceramic chip capacitors placed near loads can be used as decoupling capacitors. A low-ESR solid tantalum and aluminum electrolytic capacitor (ESR<1Ω) works extremely well and provides good transient response and stability over temperature.

The output capacitors are also used to reduce the slew rate of load current and help the APL5331 to minimize variations of the output voltage, improving transient response. For this purpose, the low-ESR capacitors are recommended and depend on the stepping and slew rate of load current.

Input Capacitor

The input capacitors of VCNTL and VIN pins are not required for stability but for supplying surge currents during large load transients, This will prevent the input rail from drooping and improve the performance of the APL5331. Because of parasitic inductors from voltage sources or other bulk capacitors to the VCNTL and VIN pins will limit the slew rate of the surge currents during large load transients, resulting in voltage drop at VIN and VCNTL pins.

A capacitor of 1μF (ceramic chip capacitor) or greater (aluminum electrolytic capacitor) is recommended to connect near VCNTL pin. For VIN pin, an aluminum electrolytic capacitor (>50μF) is recommended. It is not necessary to use low-ESR capacitors.

Layout and Thermal Consideration

The input capacitors for VIN and VCNTL pins are normally placed near each pin for good performances. Ceramic decoupling capacitors at output must be placed as close to the load to reduce the parasitic inductors of traces. It is also recommended that the APL5331 and output capacitors are placed near the load for good load regulation and load transient response. The negative pins of the input and output capacitors and the GND pin of the APL5331 should connect to analog ground plane of the load.

See figure 1. The SOP-8-P utilizes a bottom thermal pad to minimize the thermal resistance of the package, making the package suitable for high current applications. The thermal pad is soldered to the top ground pad and is connected to the internal or bottom ground plane by several vias. The printed circuit board (PCB) forms a heat sink and dissipates most of the heat into ambient air. The vias are recommended to have proper size to retain solder, helping heat conduction.

Thermal resistance consists of two main elements, θ_{JC} (junction-to-case thermal resistance) and θ_{CA} (case-to-ambient thermal resistance). θ_{JC} is specified from the IC junction to the bottom of the thermal pad directly below the die. θ_{CA} is the resistance from the bottom of thermal pad to the ambient air and it includes θ_{CS} (case-to-sink thermal resistance) and θ_{SA} (sink-to-ambient thermal resistance). The specified path for heat flow is the lowest resistance path and it dissipates majority of the heat to the ambient air. Typically, θ_{CA} is the dominant thermal resistance. Therefore, enlarging the internal or bottom ground plane reduces the resistance θ_{CA}. The relationship between power dissipation and temperatures is the following equation :

$$P_D = (T_J - T_A) / \theta_{JA}$$

where,

P_D : Power dissipation

T_J : Junction Temperature

T_A : Ambient Temperature

θ_{JA}: Junction-to-Ambient Thermal Resistance

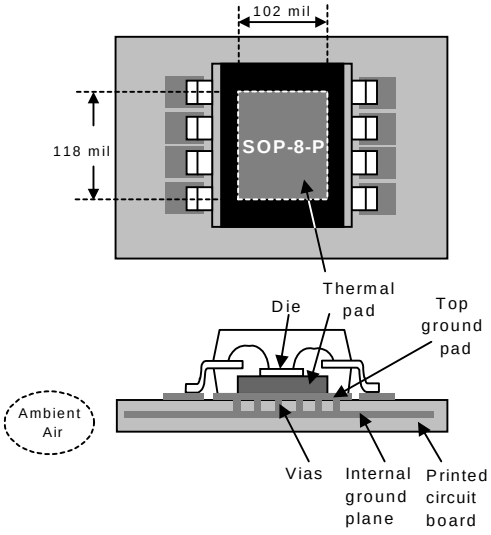


Figure 1 Package Top and side view

Figure 2 shows a board layout using the SOP-8-P package. The demo board is made of FR-4 material and is a two-layer PCB. The size and thickness are 65mm* 65mm and 1.6mm. An area of 140mil*105mil on the top layer is use as a thermal pad for the APL5331 and this is connected to the bottom layer by vias. The bottom layer using 2 oz. copper acts as the ground plane for the system. The PCB and all components on the board form a heat sink. The θ_{JA} of the APL5331(SOP-8-P) mounted on this demo board is about 37°C/W in free air. Assuming the T_A=25°C and the maximum T_J=150°C (typical thermal limit temperature), the maximum power dissipation is calculated as :

P_D (max) = (150 - 25) / 37
= 3.38W

If the T_J is designed to be below 125°C, the calculated power dissipation should be less than :

P_D = (125 - 25) / 37
= 2.70W

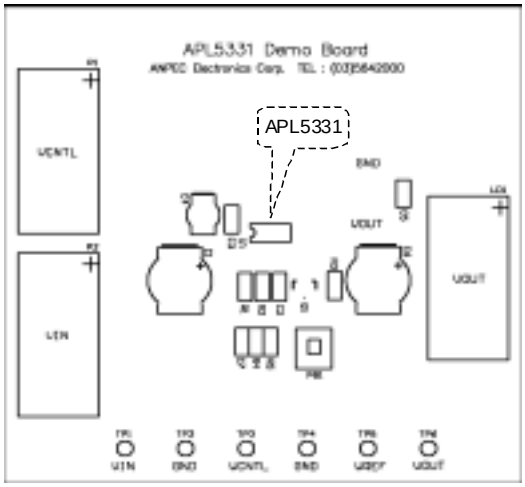


Figure 2(a) TopOver layer

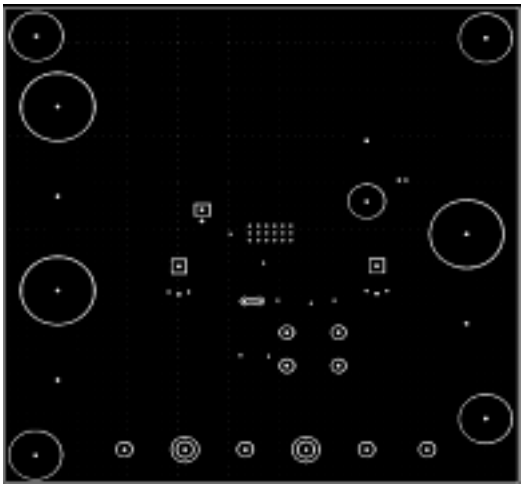


Figure 2(c) Bottom layer

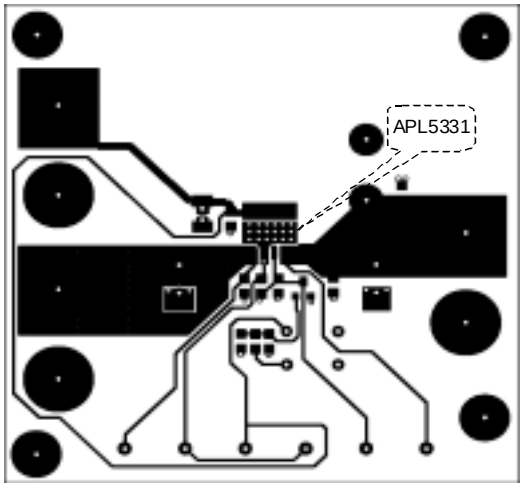
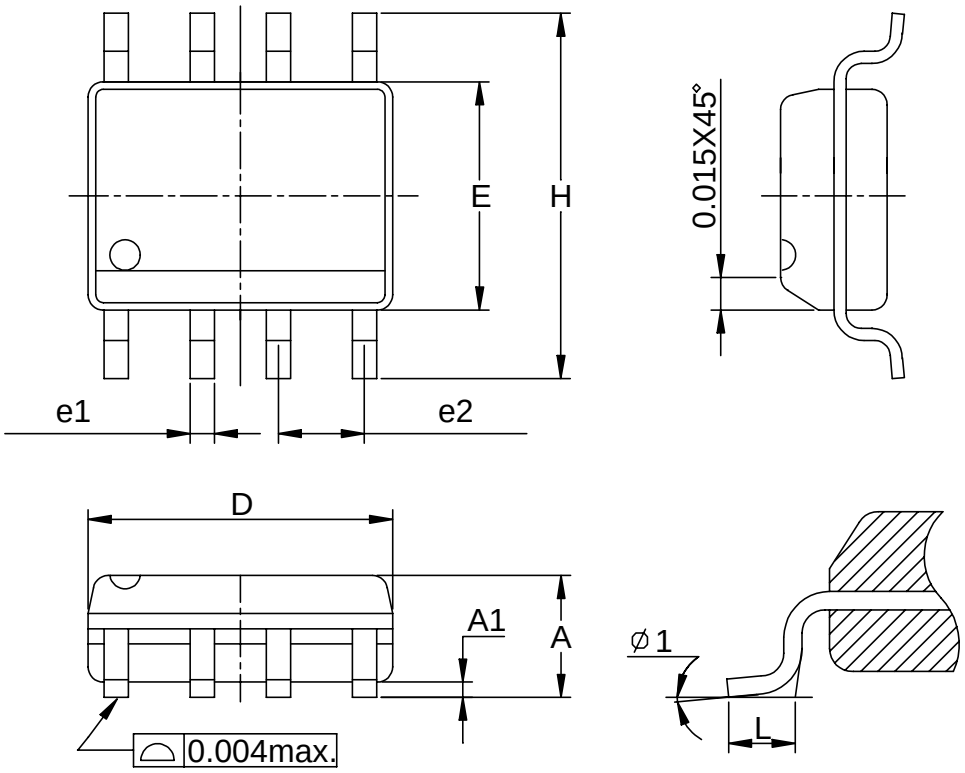


Figure 2(b) Top layer

Packaging Information

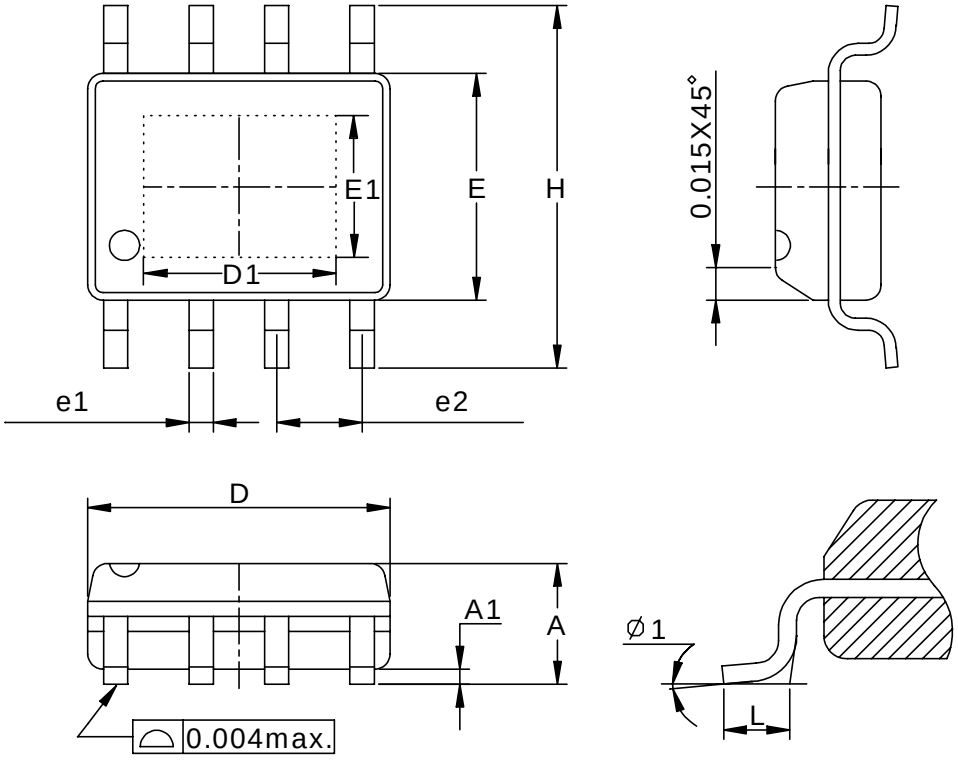
SOP-8 pin (Reference JEDEC Registration MS-012)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	8°		8°	

Packaging Information

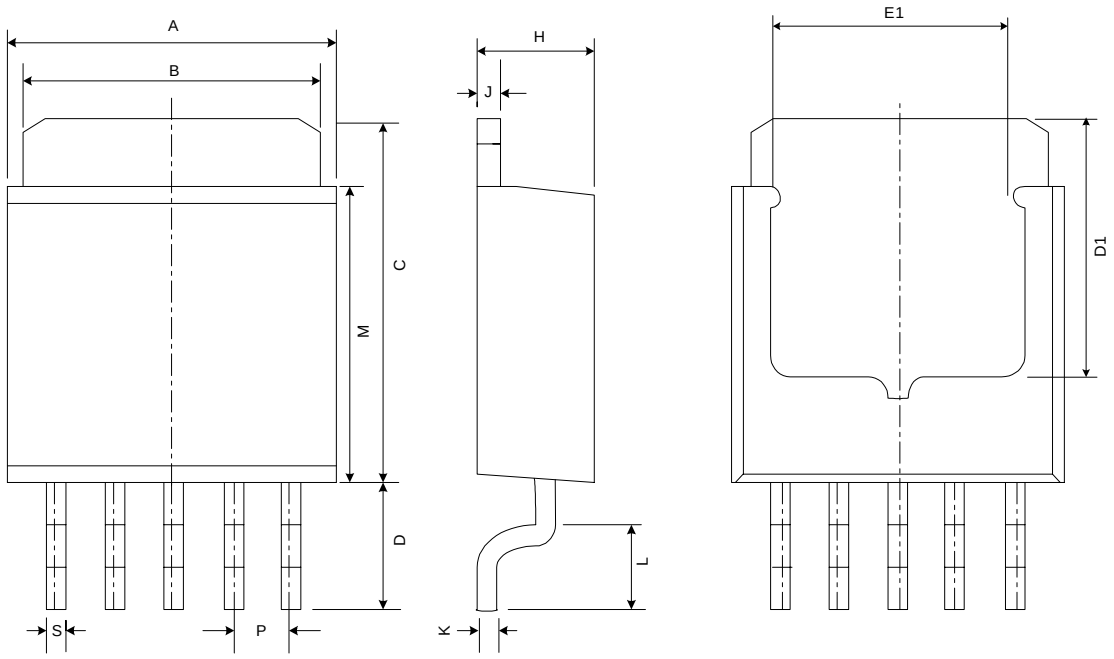
SOP-8-P pin (Reference JEDEC Registration MS-012)



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
D1	3.00REF		0.118REF	
E	3.80	4.00	0.150	0.157
E1	2.60REF		0.102REF	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
e1	0.33	0.51	0.013	0.020
e2	1.27BSC		0.50BSC	
ϕ 1	8°		8°	

Packaging Information

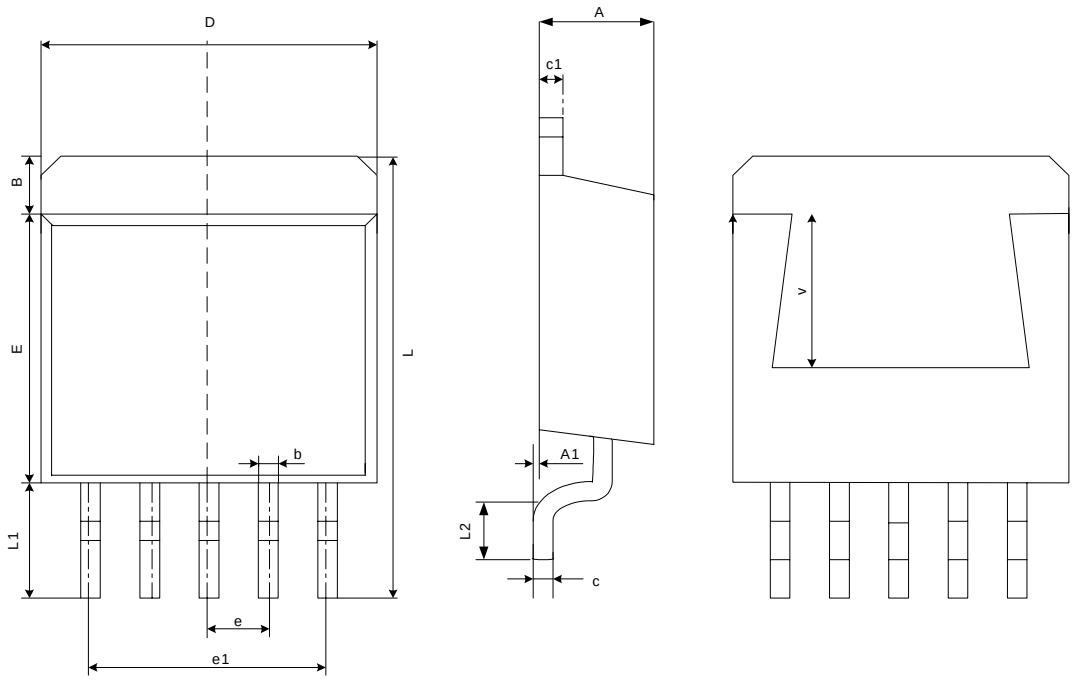
TO-252-5



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	6.40	6.80	0.25	0.26
B	5.20	5.50	0.20	0.21
C	6.80	7.20	0.26	0.27
D	2.20	2.80	0.08	0.11
D1	5.2REF		0.205REF	
E1	5.3REF		0.209REF	
P	1.27REF		0.05REF	
S	0.50	0.80	0.02	0.03
H	2.20	2.40	0.08	0.09
J	0.45	0.55	0.01	0.02
K	0.45	0.60	0.018	0.024
L	0.90	1.50	0.03	0.06
M	5.40	5.80	0.21	0.22

Packaging Information

TO-263-5



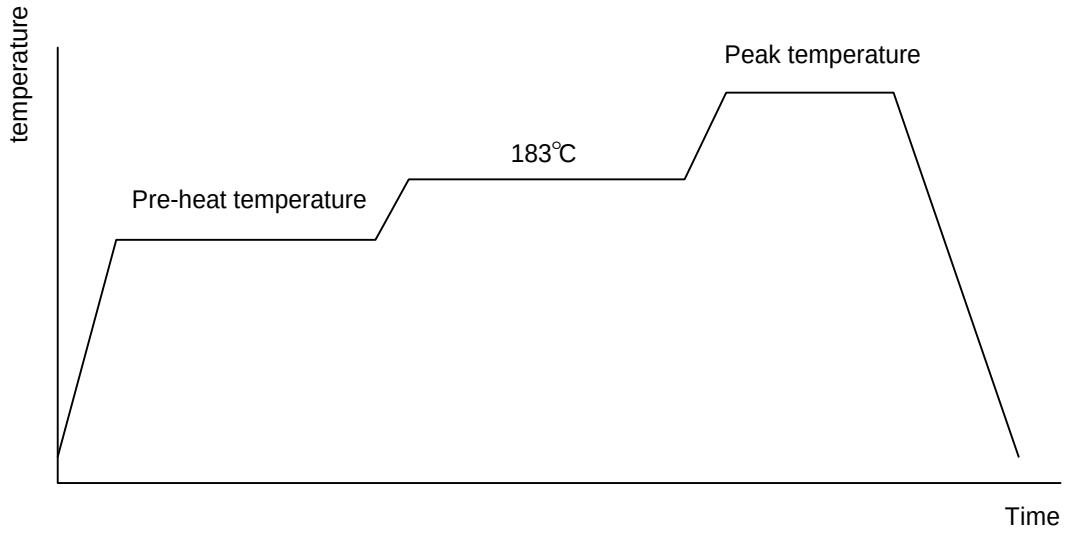
Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.06	4.83	0.160	0.190
b	0.50	0.99	0.020	0.039
b1	1.52	1.83	0.060	0.072
c	0.457	0.736	0.018	0.029
c1	1.14	1.40	0.045	0.055
D	8.25	9.66	0.325	0.380
E	9.65	10.29	0.380	0.405
L	14.60	15.88	0.575	0.625
L1	2.28	2.80	0.090	0.110
L2		1.40		0.055

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A APRIL 1999



Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183°C to Peak)	3°C/second max.	10 °C /second max.
Preheat temperature 125 ± 25°C)	120 seconds max	
Temperature maintained above 183°C	60 – 150 seconds	
Time within 5°C of actual peak temperature	10 –20 seconds	60 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C	215-219°C or 235 +5/-0°C
Ramp-down rate	6 °C /second max.	10 °C /second max.
Time 25°C to peak temperature	6 minutes max.	

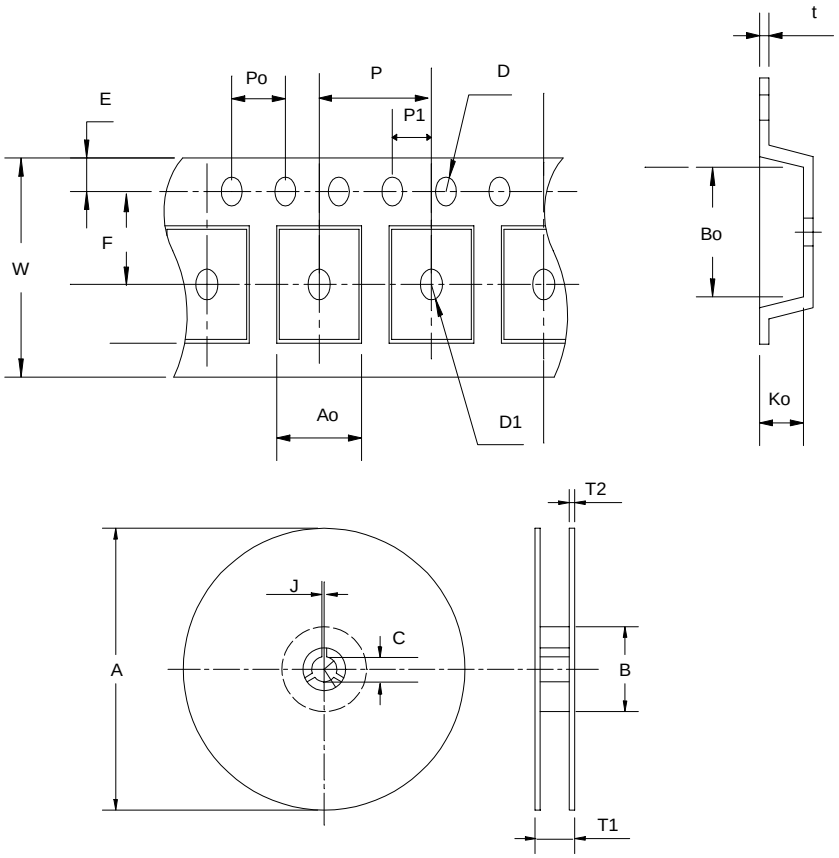
Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bgas	pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm³	pkg. thickness < 2.5mm and pkg. volume < 350mm³
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Carrier Tape



Application	A	B	C	J	T1	T2	W	P	E
SOP- 8 SOP-8-P	330 ± 1	62 +1.5	12.75+ 0.15	2 ± 0.5	12.4 ± 0.2	2 ± 0.2	12± 0. 3	8± 0.1	1.75±0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5± 1	1.55 +0.1	1.55+ 0.25	4.0 ± 0.1	2.0 ± 0.1	6.4 ± 0.1	5.2± 0. 1	2.1± 0.1	0.3±0.013
Application	A	B	C	J	T1	T2	W	P	E
TO-252	330 ±3	100 ± 2	13 ± 0. 5	2 ± 0.5	16.4 + 0.3 -0.2	2.5± 0.5	16+ 0.3 - 0.1	8 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	7.5 ± 0.1	1.5 +0.1	1.5± 0.25	4.0 ± 0.1	2.0 ± 0.1	6.8 ± 0.1	10.4± 0.1	2.5± 0.1	0.3±0.05
Application	A	B	C	J	T1	T2	W	P	E
TO-263	380±3	80 ± 2	13 ± 0. 5	2 ± 0.5	24 ± 4	2± 0.3	24 + 0.3 - 0.1	16 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	11.5 ± 0.1	1.5 +0.1	1.5± 0.25	4.0 ± 0.1	2.0 ± 0.1	10.8 ± 0.1	16.1± 0.1	5.2± 0.1	0.35±0.013

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 8 / SOP-8-P	12	9.3	2500
TO- 252	16	13.3	2500
TO- 263	24	21.3	1000

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