

# 74LCX125

## Low Voltage Quad Buffer with 5V Tolerant Inputs and Outputs

### Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V  $V_{CC}$  specifications provided
- 6.0ns  $t_{PD}$  max. ( $V_{CC} = 3.3V$ ), 10 $\mu$ A  $I_{CC}$  max.
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal<sup>(1)</sup>
- $\pm 24mA$  output drive ( $V_{CC} = 3.0V$ )
- Implements proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds JEDEC 78 conditions
- ESD performance:
  - Human body model > 2000V
  - Machine model > 100V
- Leadless DQFN package

### Note:

1. To ensure the high-impedance state during power up or down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor: the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### General Description

The LCX125 contains four independent non-inverting buffers with 3-STATE outputs. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX125 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

### Ordering Information

Order Number	Package Number	Package Description
74LCX125M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX125SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX125BQX <sup>(2)</sup>	MLP14A	14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
74LCX125MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

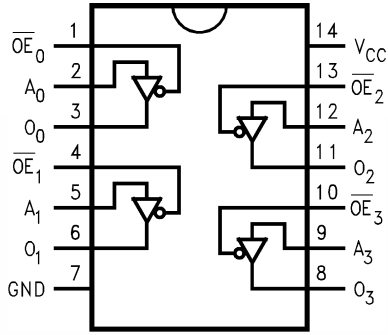
### Note:

2. DQFN package available in Tape and Reel only.  
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

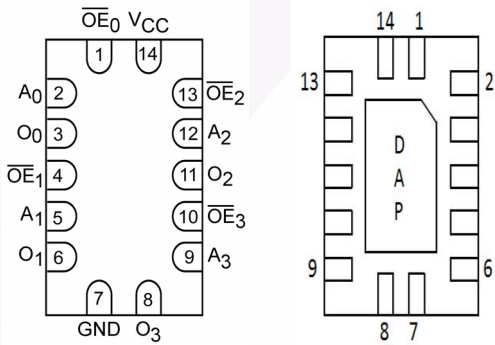
## Connection Diagrams

Pin Assignments for SOIC, SOP, and TSSOP



(Top View)

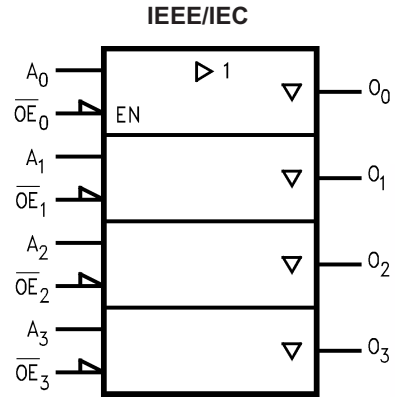
Pad Assignments for DQFN



(Top Through View)

(Bottom View)

## Logic Symbol



## Truth Table

Inputs		Output
$\overline{OE}_n$	$A_n$	$O_n$
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

Z = High Impedance

X = Immaterial

## Pin Description

Pin Names	Description
$A_n$	Inputs
$\overline{OE}_n$	Output Enable Inputs
$O_n$	Outputs
DAP	No Connect

Note: DAP (Die Attach Pad)

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$V_I$	DC Input Voltage	-0.5V to +7.0V
$V_O$	DC Output Voltage, Output in 3-STATE	-0.5V to +7.0V
	Output in HIGH or LOW State <sup>(3)</sup>	-0.5V to $V_{CC} + 0.5V$
$I_{IK}$	DC Input Diode Current, $V_I < GND$	-50mA
$I_{OK}$	DC Output Diode Current $V_O < GND$	-50mA
	$V_O > V_{CC}$	+50mA
$I_O$	DC Output Source/Sink Current	$\pm 50mA$
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 100mA$
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C

**Note:**

3.  $I_O$  Absolute Maximum Rating must be observed.

## Recommended Operating Conditions<sup>(4)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
$V_{CC}$	Supply Voltage Operating	2.0	3.6	V
	Data Retention	1.5	3.6	
$V_I$	Input Voltage	0	5.5	V
$V_O$	Output Voltage HIGH or LOW State	0	$V_{CC}$	V
	3-STATE	0	5.5	
$I_{OH} / I_{OL}$	Output Current $V_{CC} = 3.0V-3.6V$		$\pm 24$	mA
	$V_{CC} = 2.7V-3.0V$		$\pm 12$	
	$V_{CC} = 2.3V-2.7V$		$\pm 8$	
$T_A$	Free-Air Operating Temperature	-40	85	°C
$\Delta t / \Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V

**Note:**

4. Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Max.	
V <sub>IH</sub>	HIGH Level Input Voltage	2.3–2.7		1.7		V
		2.7–3.6		2.0		
V <sub>IL</sub>	LOW Level Input Voltage	2.3–2.7			0.7	V
		2.7–3.6			0.8	
V <sub>OH</sub>	HIGH Level Output Voltage	2.3–3.6	I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2		V
		2.3	I <sub>OH</sub> = -8mA	1.8		
		2.7	I <sub>OH</sub> = -12mA	2.2		
		3.0	I <sub>OH</sub> = -18mA	2.4		
			I <sub>OH</sub> = -24mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.3–3.6	I <sub>OL</sub> = 100μA		0.2	V
		2.3	I <sub>OL</sub> = 8mA		0.6	
		2.7	I <sub>OL</sub> = 12mA		0.4	
		3.0	I <sub>OL</sub> = 16mA		0.4	
			I <sub>OL</sub> = 24mA		0.55	
I <sub>I</sub>	Input Leakage Current	2.3–3.6	0 ≤ V <sub>I</sub> ≤ 5.5V		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	2.3–3.6	0 ≤ V <sub>O</sub> ≤ 5.5V, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	0	V <sub>I</sub> or V <sub>O</sub> = 5.5V		10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.3–3.6	V <sub>I</sub> = V <sub>CC</sub> or GND		10	μA
			3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V <sup>(5)</sup>		±10	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.3–3.6	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		500	μA

**Note:**

5. Outputs disabled or 3-STATE only.

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V, C <sub>L</sub> = 50 pF		V <sub>CC</sub> = 2.7V, C <sub>L</sub> = 50 pF		V <sub>CC</sub> = 2.5V ± 0.2V, C <sub>L</sub> = 30 pF		
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay	1.5	6.0	1.5	6.5	1.5	7.2	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	1.5	7.0	1.5	8.0	1.5	9.1	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time	1.5	6.0	1.5	7.0	1.5	7.2	ns
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew <sup>(6)</sup>		1.0					ns

**Note:**

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

**Dynamic Switching Characteristics**

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = 25°C	
				Typical	Unit
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	3.3	C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	0.8	V
		2.5	C <sub>L</sub> = 30pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	0.6	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	3.3	C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	-0.8	V
		2.5	C <sub>L</sub> = 30pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	-0.6	

**Capacitance**

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	7.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8.0	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10MHz	25.0	pF

**AC Loading and Waveforms** (Generic for LCX Family)

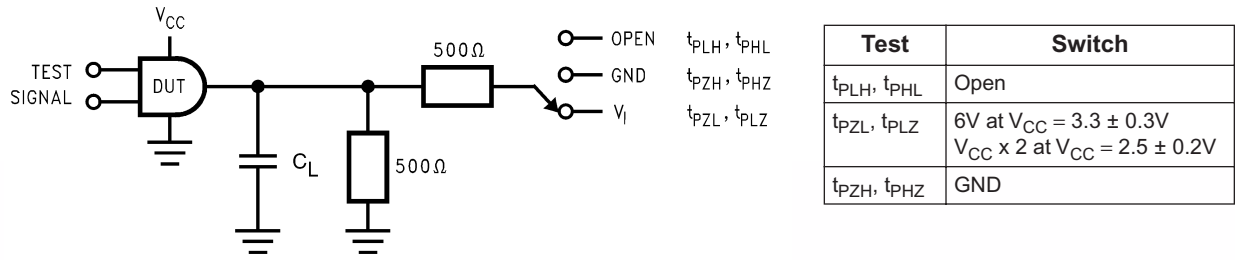
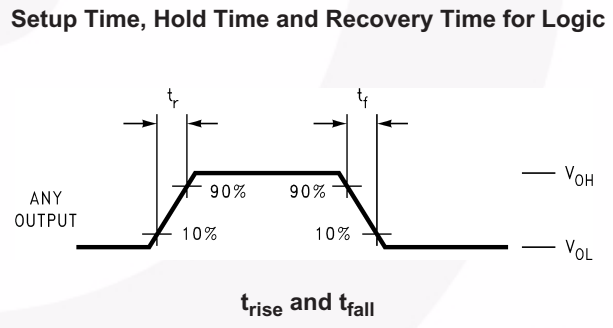
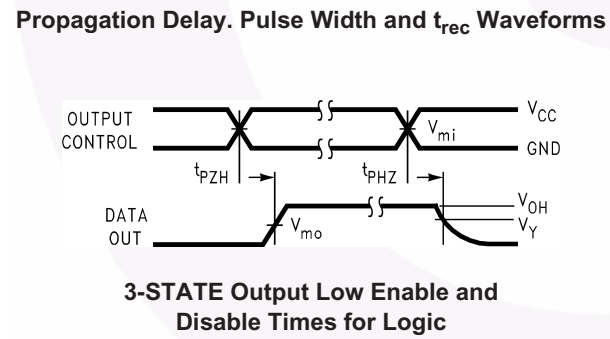
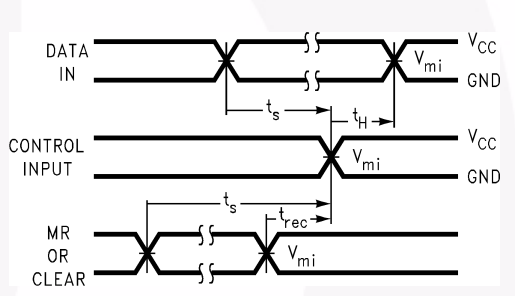
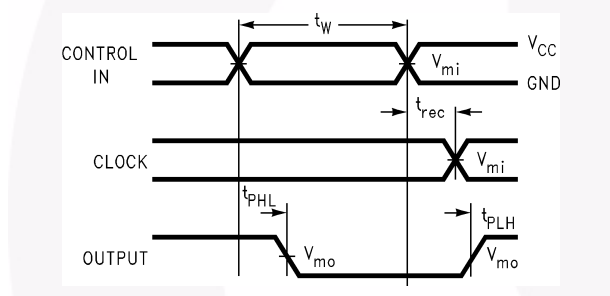
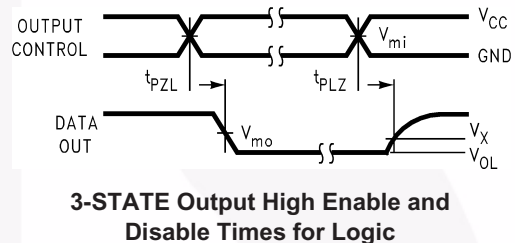
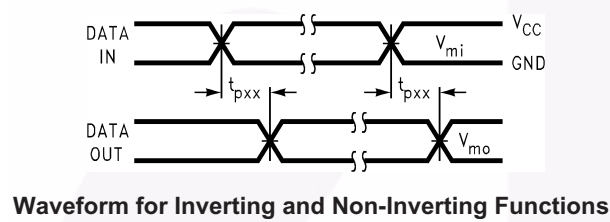


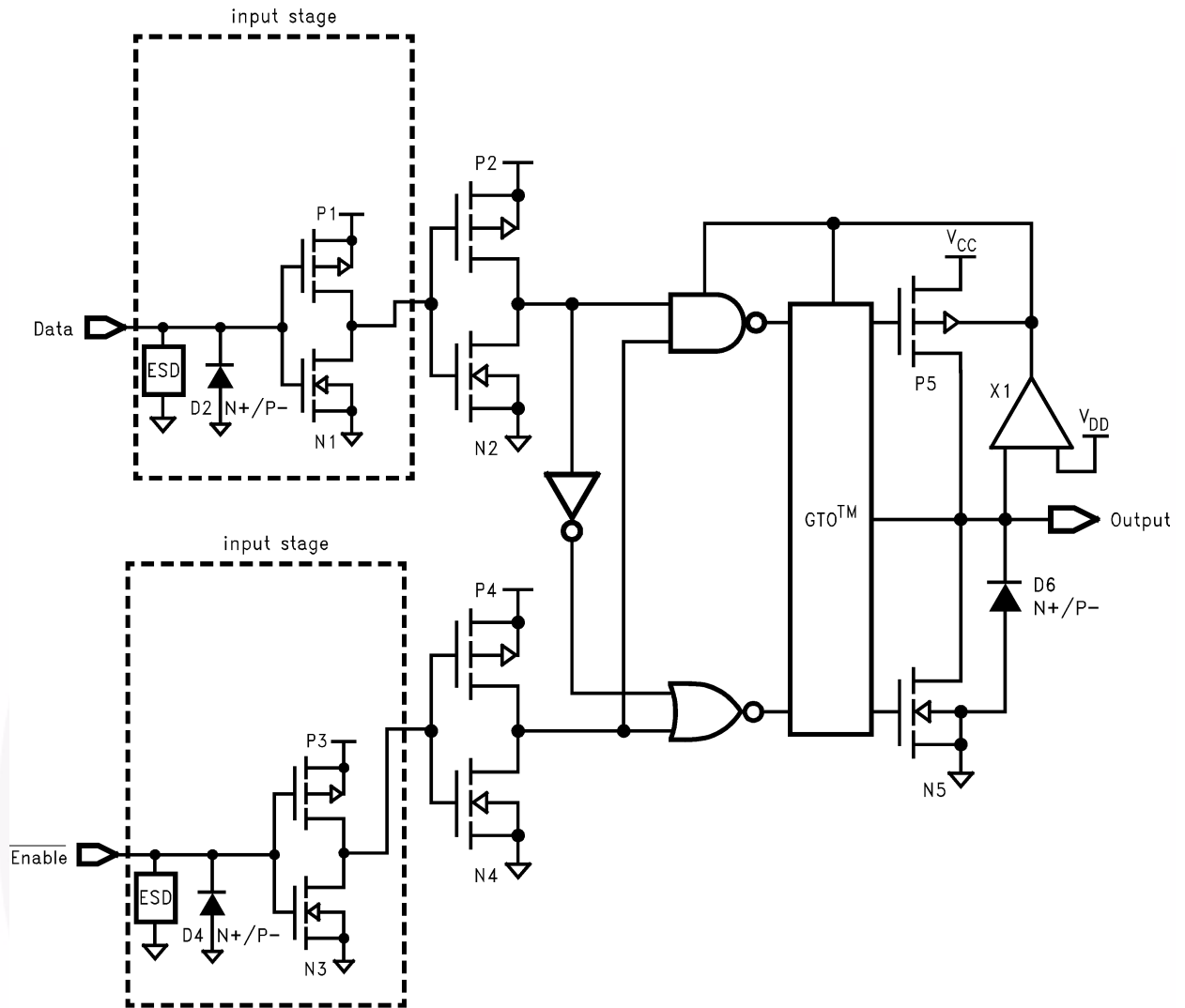
Figure 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)



Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Figure 2. Waveforms (Input Characteristics;  $f = 1MHz, t_r = t_f = 3ns$ )

Schematic Diagram (Generic for LCX Family)

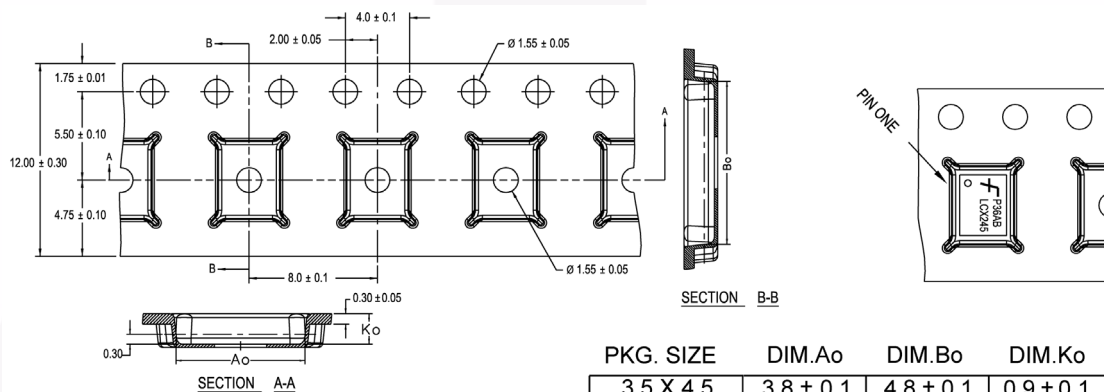


## Tape and Reel Specification

### Tape Format for DQFN

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (Typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typ.)	Empty	Sealed

### Tape Dimensions inches (millimeters)



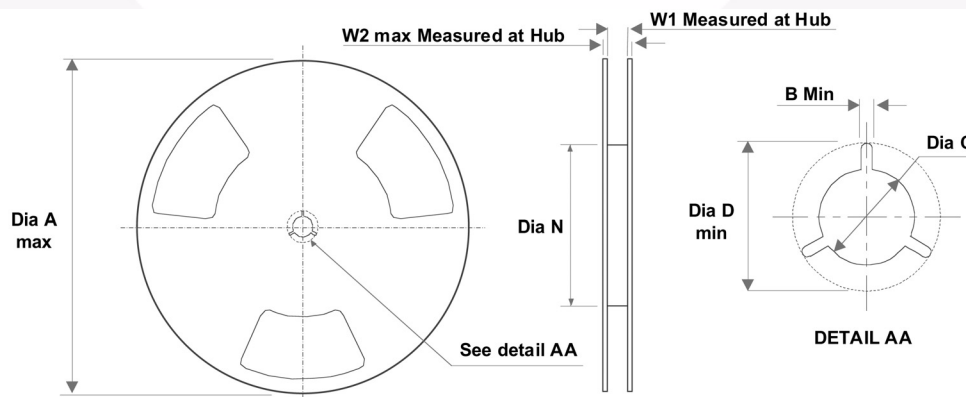
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

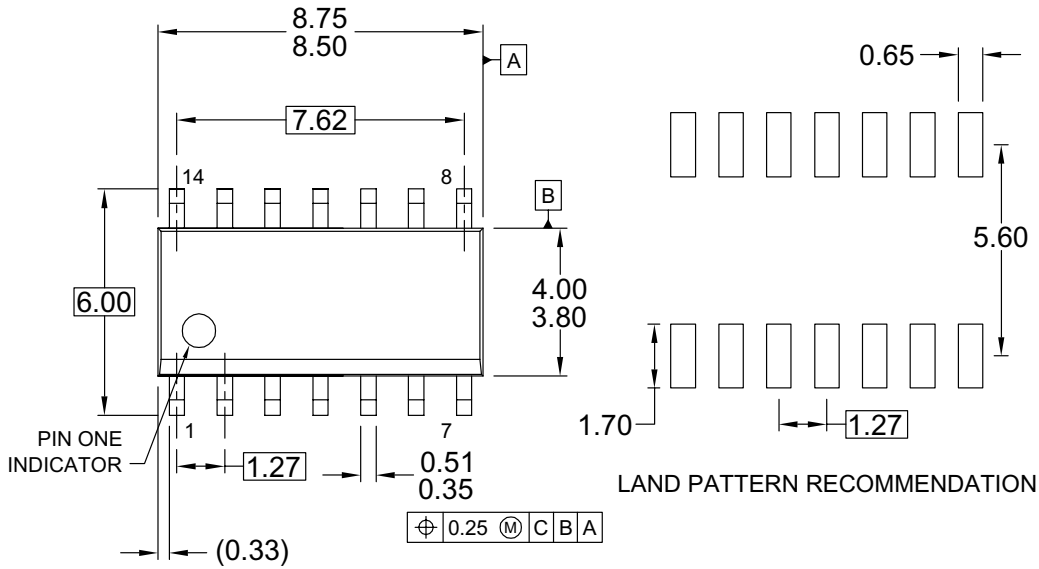
### Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12mm	13.0 (330.0)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.488 (12.4)	0.724 (18.4)



### Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13



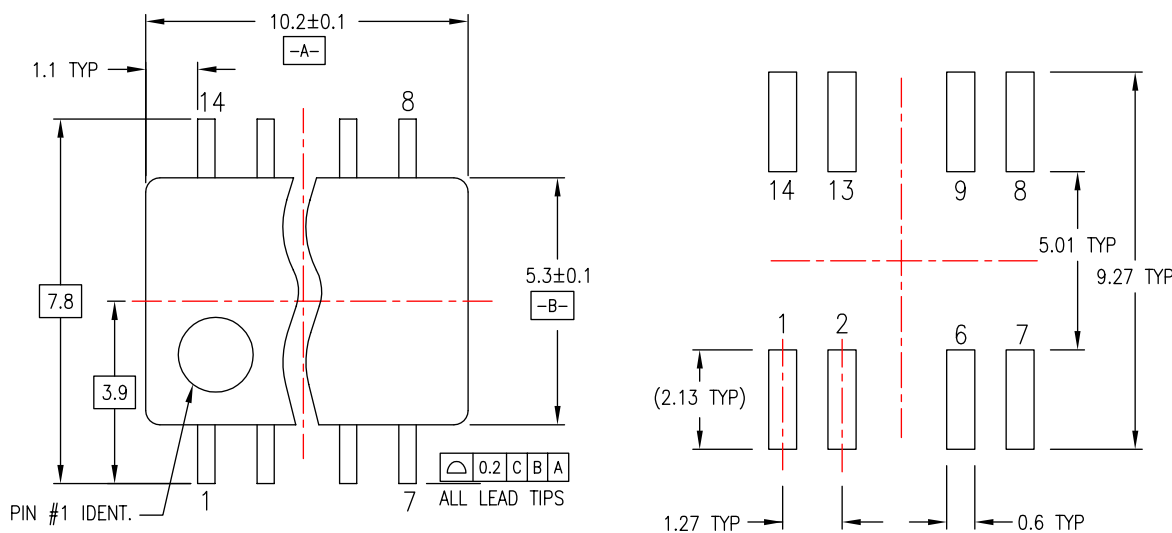
**Figure 3. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**

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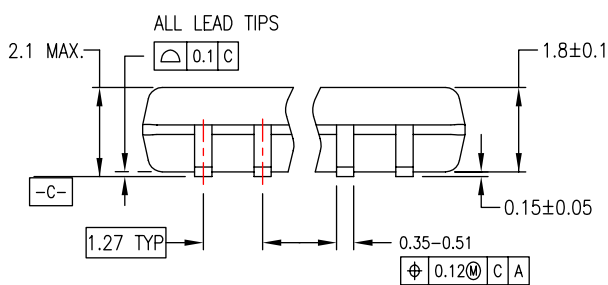
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Physical Dimensions (Continued)



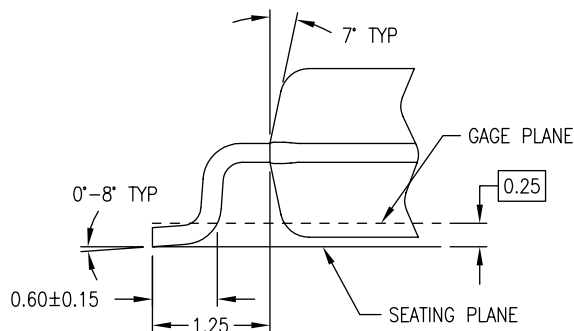
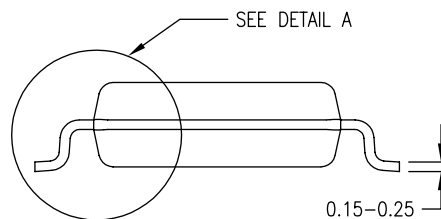
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



DETAIL A

M14DREVC

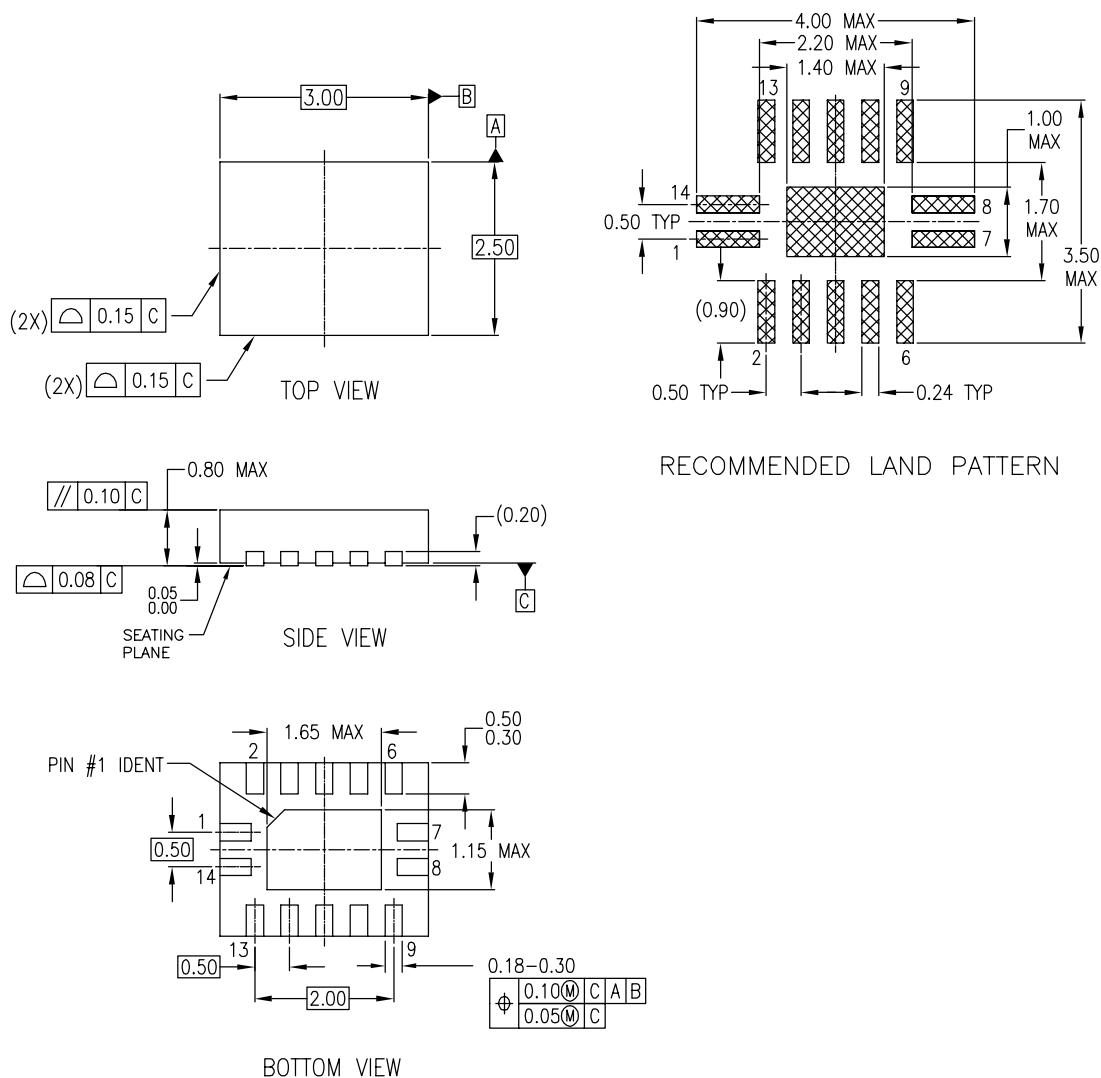
Figure 4. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP14ArevA

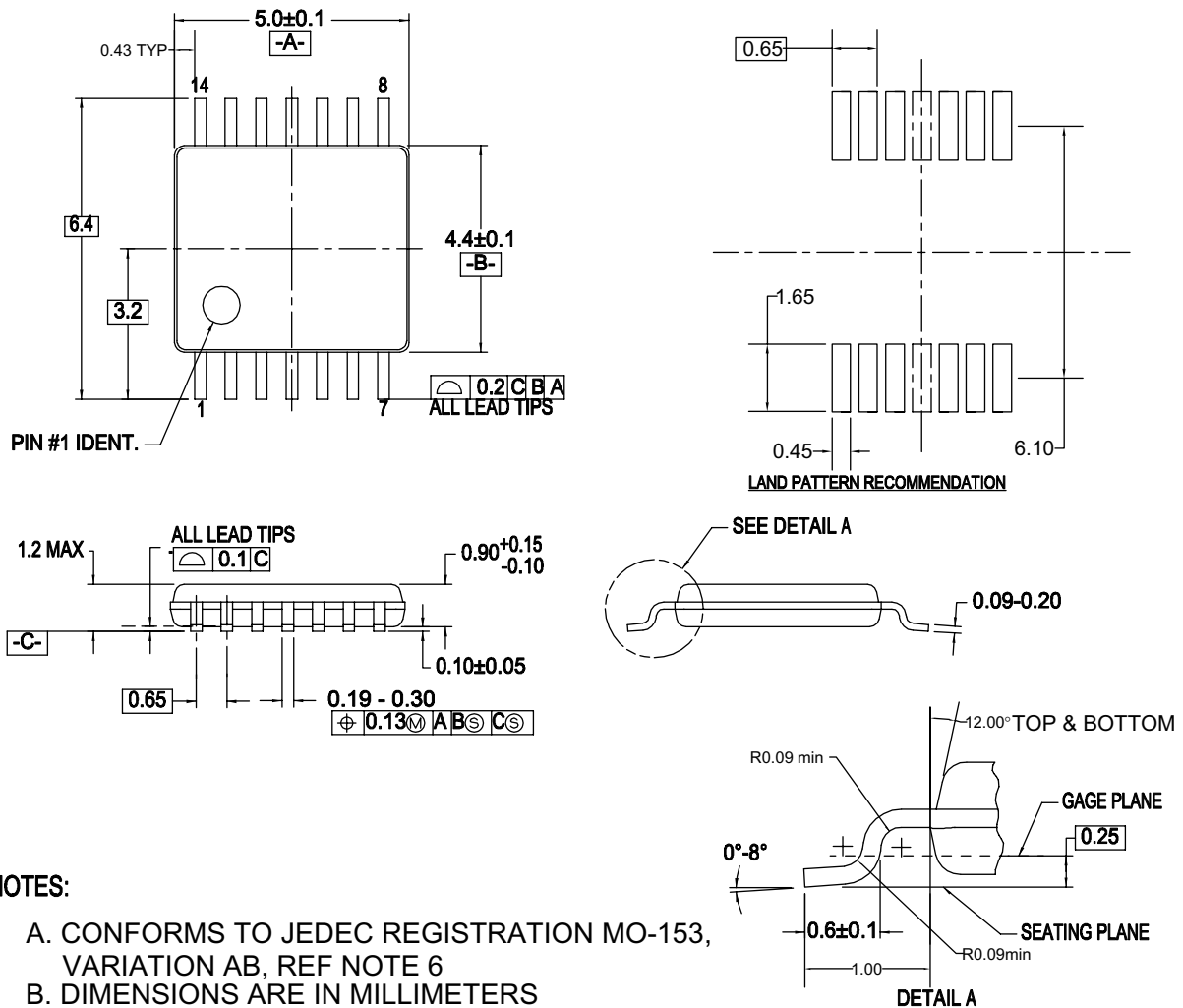
Figure 5. 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm

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Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 6. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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| AX-CAP®*  | FRFET®   | PowerXS™  |  |
| BitSiC™   | Global Power Resource™                         | PowerTrench®  | TinyBoost®  |
| Build it Now™   | GreenBridge™                                   | PowerXS™  | TinyBuck®   |
| CorePLUS™   | Green FPS™                                     | Programmable Active Droop™  | TinyCalc™   |
| CorePOWER™  | Green FPS™ e-Series™                           | QFET®   | TinyLogic®  |
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| FAST®   | OptoHiT™                                       | SuperSOT™-6   | VisualMax™  |
| FastvCore™  | OPTOLOGIC®                                     | SuperSOT™-8   | VoltagePlus™  |
| FETBench™   | OPTOPLANAR®                                    | SupreMOS®   | XS™   |
| FPS™  |  | SyncFET™  |   |

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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