

PCM1725

# SoundPlus™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER 16 Bits, 96kHz Sampling

## FEATURES

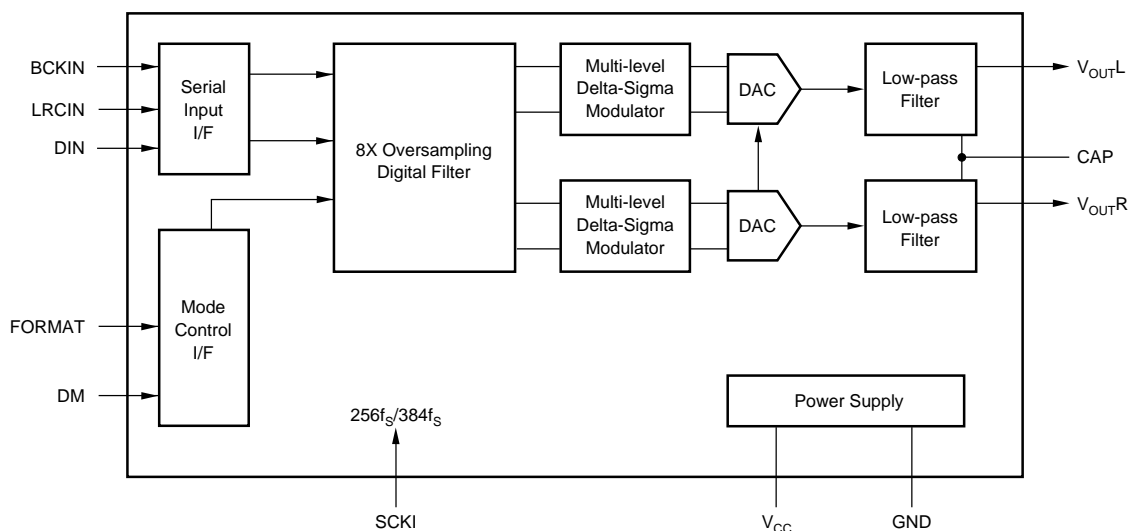
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 95dB
- MULTIPLE SAMPLING FREQUENCIES: 16kHz to 96kHz
- 8X OVERSAMPLING DIGITAL FILTER
- SYSTEM CLOCK:  $256f_s/384f_s$
- NORMAL OR I<sup>2</sup>S DATA INPUT FORMATS
- SMALL 14-PIN SOIC PACKAGE

## DESCRIPTION

The PCM1725 is a complete low cost stereo audio digital-to-analog converter (DAC), operating off of a  $256f_s$  or  $384f_s$  system clock. The DAC contains a 3rd-order  $\Delta\Sigma$  modulator, a digital interpolation filter, and an analog output amplifier. The PCM1725 accepts 16-bit input data in either normal or I<sup>2</sup>S formats.

The digital filter performs an 8X interpolation function and includes de-emphasis at 44.1kHz. The PCM1725 can accept digital audio sampling frequencies from 16kHz to 96kHz, always at 8X oversampling.

The PCM1725 is ideal for low-cost, CD-quality consumer audio applications.



# SPECIFICATIONS

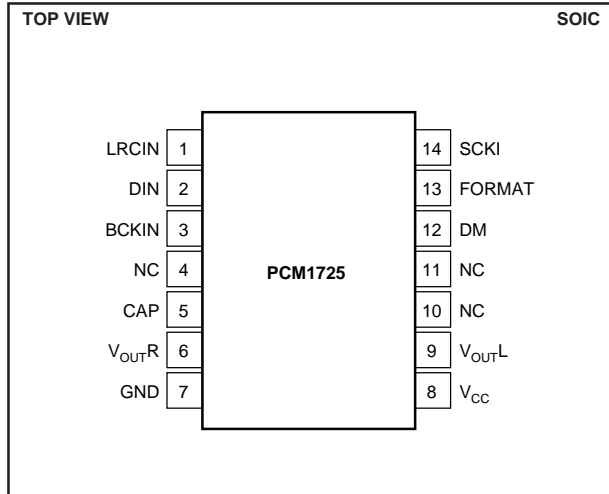
All specifications at +25°C, +V<sub>CC</sub> = +5V, f<sub>s</sub> = 44.1kHz, and 16-bit input data, SYSCLK = 384f<sub>s</sub>, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1725			UNITS
		MIN	TYP	MAX	
<b>RESOLUTION</b>		16			Bits
<b>DATA FORMAT</b> Audio Data Interface Format Audio Data Format Sampling Frequency (f <sub>s</sub> ) Internal System Clock Frequency		16	Standard/I <sup>2</sup> S Binary Two's Complement	96	kHz
<b>DIGITAL INPUT/OUTPUT</b> Logic Level Input Logic Level V <sub>IH</sub> <sup>(1)</sup> V <sub>IL</sub> <sup>(1)</sup> Input Logic Current: I <sub>IN</sub> <sup>(1)</sup>		2.0	TTL	0.8 ±0.8	VDC VDC µA
<b>DYNAMIC PERFORMANCE</b> <sup>(2)</sup> THD+N at FS (0dB) THD+N at -60dB Dynamic Range Signal-to-Noise Ratio Channel Separation	f = 991kHz  A-weighted A-weighted	90 90 88	-83 -32 95 97 95	-78	dB dB dB dB dB
<b>DC ACCURACY</b> Gain Error Gain Mismatch, Channel-to-Channel Bipolar Zero Error	V <sub>OUT</sub> = V <sub>CC</sub> /2 at BPZ		±1.0 ±1.0 ±20	±5.0 ±5.0 ±50	% of FSR % of FSR mV
<b>ANALOG OUTPUT</b> Output Voltage Center Voltage Load Impedance	Full Scale (0dB)  AC Load	10	0.62 x V <sub>CC</sub> V <sub>CC</sub> /2		Vp-p VDC kΩ
<b>DIGITAL FILTER PERFORMANCE</b> Passband Stopband Passband Ripple Stopband Attenuation Delay Time		0.555  -35		0.445 ±0.17 11.125/f <sub>s</sub>	f <sub>s</sub> f <sub>s</sub> dB dB sec
<b>INTERNAL ANALOG FILTER</b> -3dB Bandwidth Passband Response	f = 20kHz		100 -0.16		kHz dB
<b>POWER SUPPLY REQUIREMENTS</b> Voltage Range Supply Current Power Dissipation		4.5	5 13 65	5.5 18 90	VDC mA mW
<b>TEMPERATURE RANGE</b> Operation Storage		-25 -55		+85 +125	°C °C

NOTES: (1) Pins 1, 2, 3, 12, 13: LRCIN, DIN, BCKIN, DM, FORMAT (Schmitt Trigger Input); Pin 14: SCKI. (2) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode.

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## PIN CONFIGURATION



## PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
PCM1725U	14 Pin SOIC	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+6.5V
+V <sub>CC</sub> to +V <sub>DD</sub> Difference	±0.1V
Input Logic Voltage	-0.3V to (V <sub>DD</sub> + 0.3V)
Power Dissipation	290mW
Operating Temperature Range	-25°C to +85°C
Storage Temperature	-55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Thermal Resistance, $\theta_{JA}$	+90°C/W

## PIN ASSIGNMENTS

PIN	NAME	I/O	FUNCTION
1 <sup>(1)</sup>	LRCIN	IN	Sample Rate Clock Input
2 <sup>(1)</sup>	DIN	IN	Audio Data Input
3 <sup>(1)</sup>	BCKIN	IN	Bit Clock Input for Audio Data.
4	NC	—	No Connection
5	CAP	—	Common Pin of Analog Output Amp
6	V <sub>OUTR</sub>	OUT	Right-Channel Analog Output
7	GND	—	Ground
8	V <sub>CC</sub>	—	Power Supply
9	V <sub>OUTL</sub>	OUT	Left-Channel Analog Output
10	NC	—	No Connection
11	NC	—	No Connection
12 <sup>(2)</sup>	DM	IN	De-emphasis Control HIGH: De-emphasis ON LOW: De-emphasis OFF
13 <sup>(2)</sup>	FORMAT	—	Audio Data Format Select HIGH: I <sup>2</sup> S Data Format LOW: Standard Data Format
14	SCKI	IN	System Clock Input (256f <sub>S</sub> or 384f <sub>S</sub> )

NOTES: (1) Schmitt Trigger input. (2) Schmitt Trigger input with internal pull-up.



## ELECTROSTATIC DISCHARGE SENSITIVITY

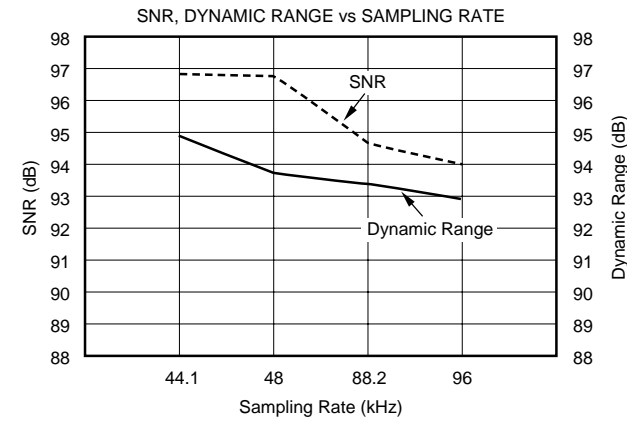
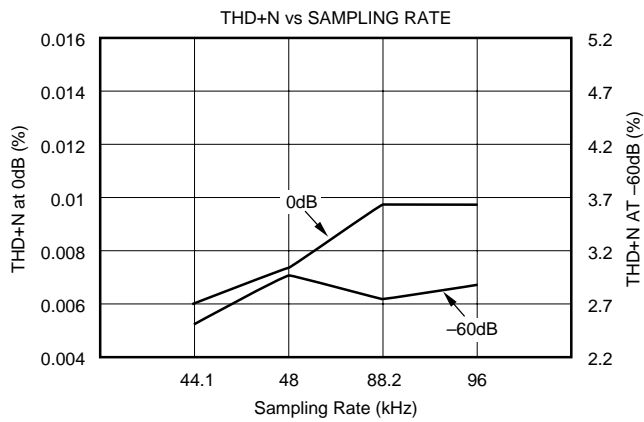
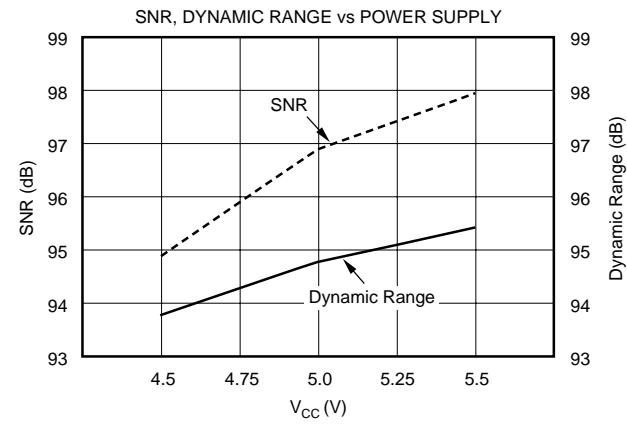
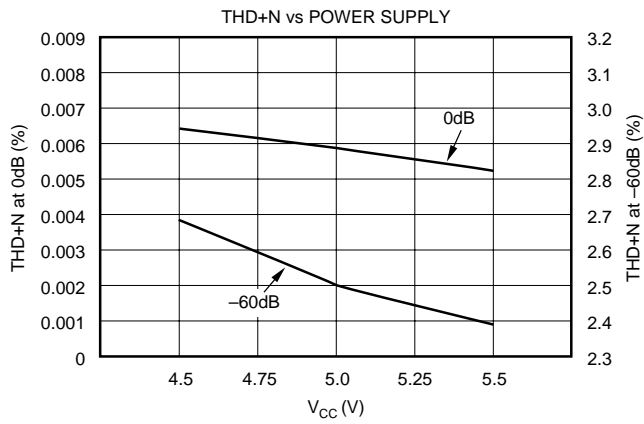
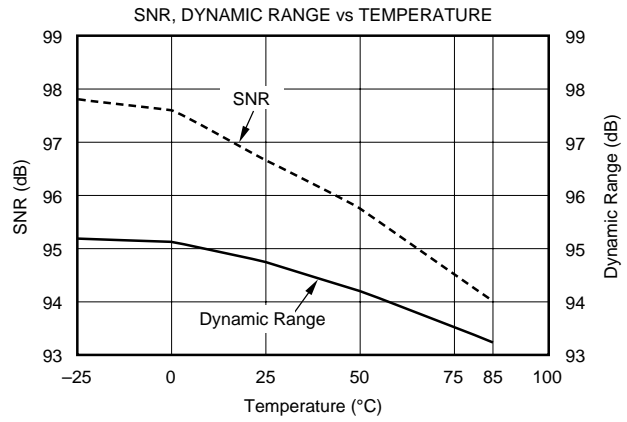
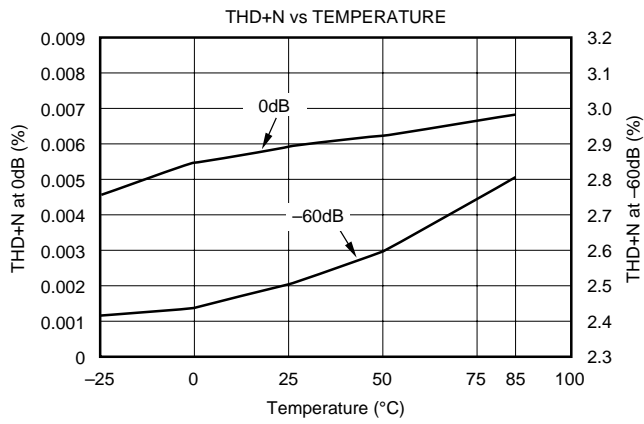
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $+V_{CC} = +5\text{V}$ ,  $f_s = 44.1\text{kHz}$ ,  $\text{SYSCLK} = 256f_s$ , unless otherwise noted.

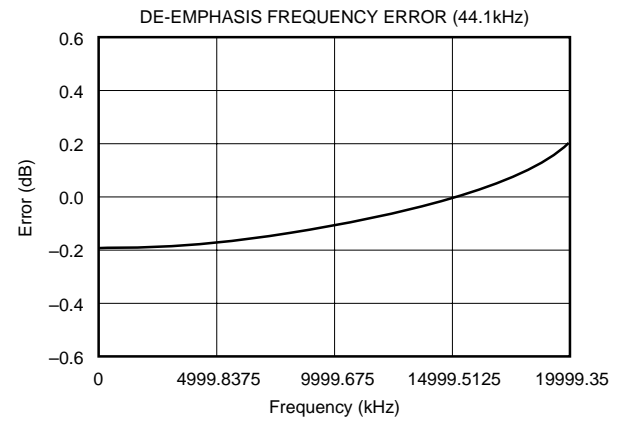
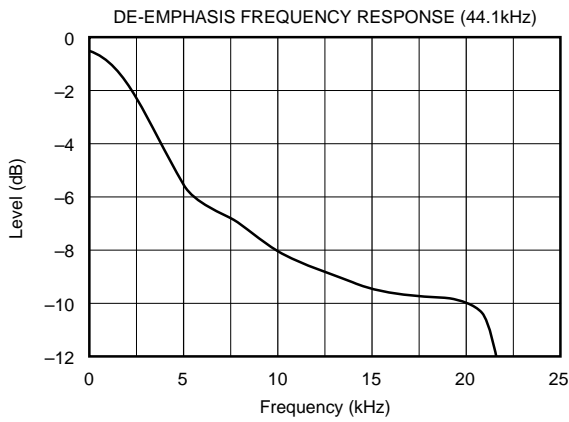
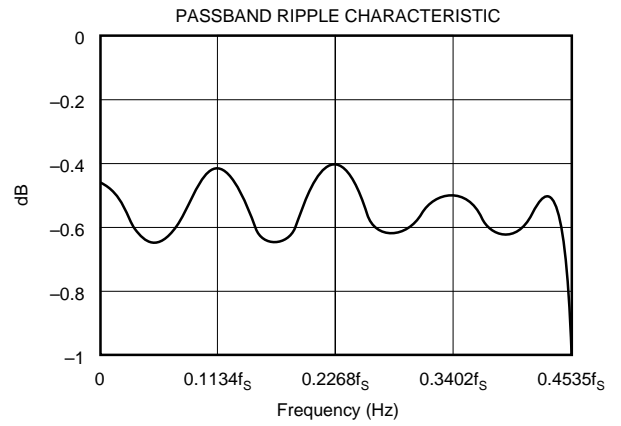
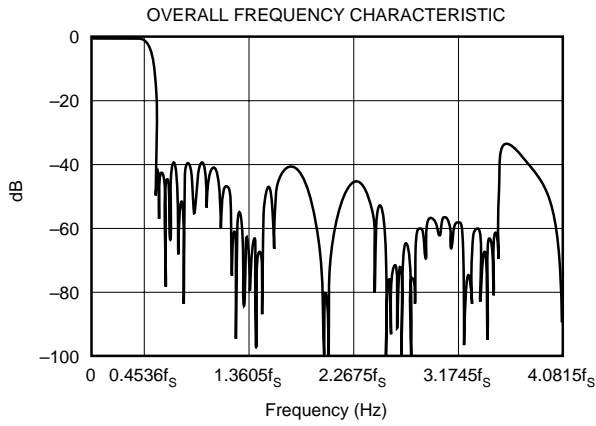
## DYNAMIC PERFORMANCE



# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $+V_{CC} = +V_{DD} = +5\text{V}$ ,  $f_S = 44.1\text{kHz}$ , and 16-bit input data,  $\text{SYSCLK} = 384f_S$ , unless otherwise noted.

## DIGITAL FILTER



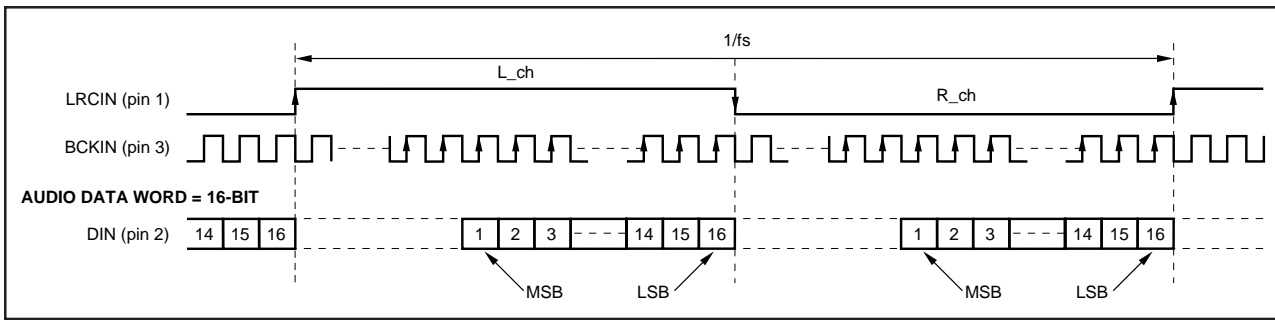


FIGURE 1. "Normal" Data Input Timing.

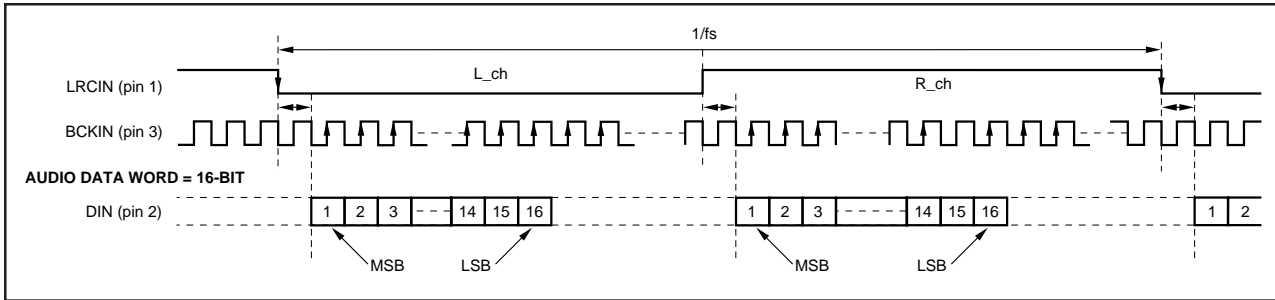


FIGURE 2. "I2S" Data Input Timing.

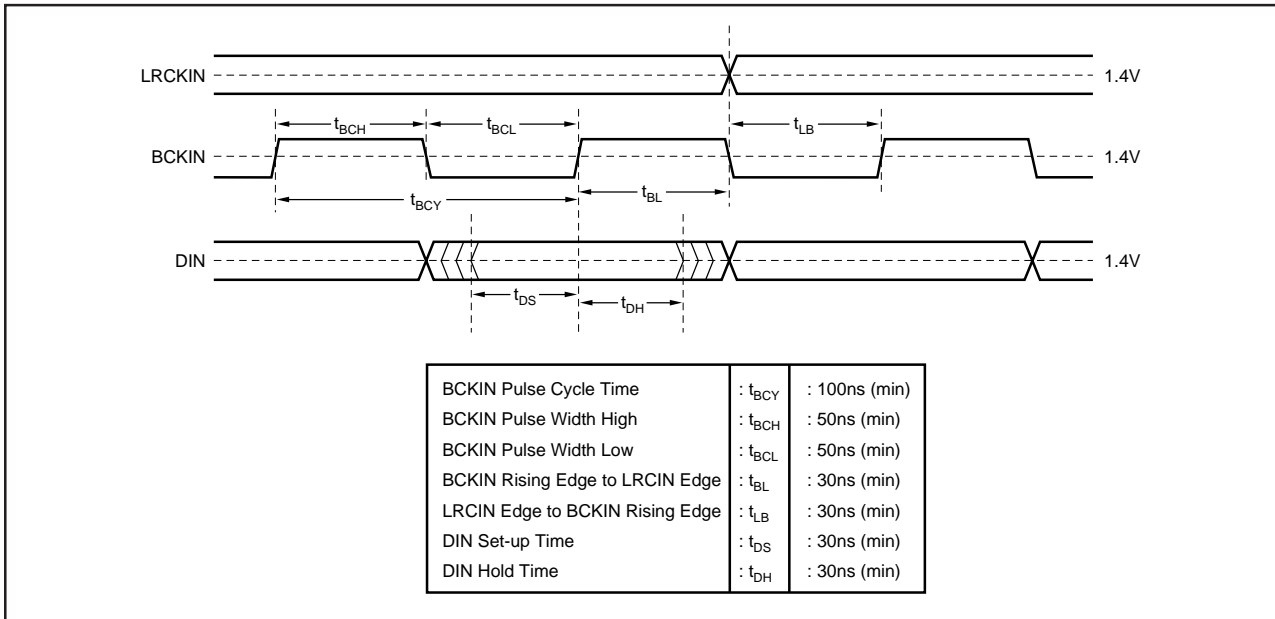


FIGURE 3. Audio Data Input Timing.

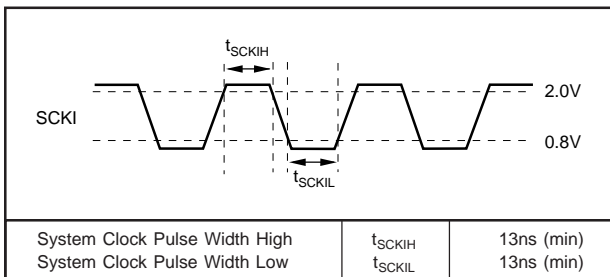


FIGURE 4. System Clock Timing Requirements.

## SYSTEM CLOCK

The system clock for PCM1725 must be either  $256f_s$  or  $384f_s$ , where  $f_s$  is the audio sampling frequency (LRCIN), typically 32kHz, 44.1kHz or 48kHz. The system clock is used to operate the digital filter and the noise shaper. The system clock input (SCKI) is at pin 14. Timing conditions for SCKI are shown in Figure 4.

PCM1725 has a system clock detection circuit which automatically detects the frequency, either  $256f_s$  or  $384f_s$ . The system clock should be synchronized with LRCIN (pin 1), but PCM1725 can compensate for phase differences. If the phase difference between LRCIN and system clock is greater than  $\pm 6$  bit clocks (BCKIN), the synchronization is performed automatically. The analog outputs are forced to a bipolar zero state ( $V_{CC}/2$ ) during the synchronization function. Table I shows the typical system clock frequency inputs for the PCM1725.

SAMPLING RATE (LRCIN)	SYSTEM CLOCK FREQUENCY (MHz)	
	$256f_s$	$384f_s$
32kHz	8.192	12.288
44.1kHz	11.2896	16.9340
48kHz	12.288	18.432

TABLE I. System Clock Frequencies vs Sampling Rate.

### TYPICAL CONNECTION DIAGRAM

Figure 5 illustrates the typical connection diagram for PCM1725 used in a stand-alone application.

### INPUT DATA FORMAT

PCM1725 can accept input data in either normal (MSB-first, right-justified) or I<sup>2</sup>S formats. When pin 13 (FORMAT) is LOW, normal data format is selected; a HIGH on pin 13 selects I<sup>2</sup>S format.

FORMAT	
0	Normal Format (MSB-first, right-justified)
1	I <sup>2</sup> S Format (Philips serial data protocol)

TABLE II. Input Format Selection.

### RESET

PCM1725 has an internal power-on reset circuit. The internal power-on reset initializes (resets) when the supply voltage  $V_{CC} > 2.2V$  (typ). The power-on reset has an initialization period equal to 1024 system clock periods after  $V_{CC} > 2.2V$ . During the initialization period, the outputs of the DAC are invalid, and the analog outputs are forced to  $V_{CC}/2$ . Figure 6 illustrates the power-on reset and reset-pin reset timing.

### DE-EMPHASIS CONTROL

Pin 12 (DM) enables PCM1725's de-emphasis function. De-emphasis operates only at 44.1kHz.

DM	
0	DEM OFF
1	DEM ON (44.1kHz)

TABLE III. De-Emphasis Control Selection.

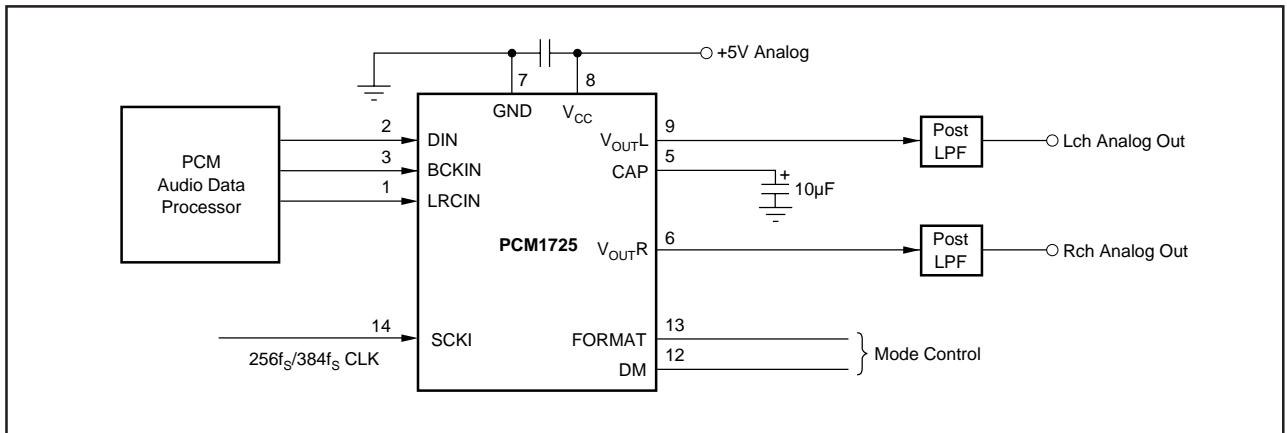


FIGURE 5. Typical Connection Diagram.

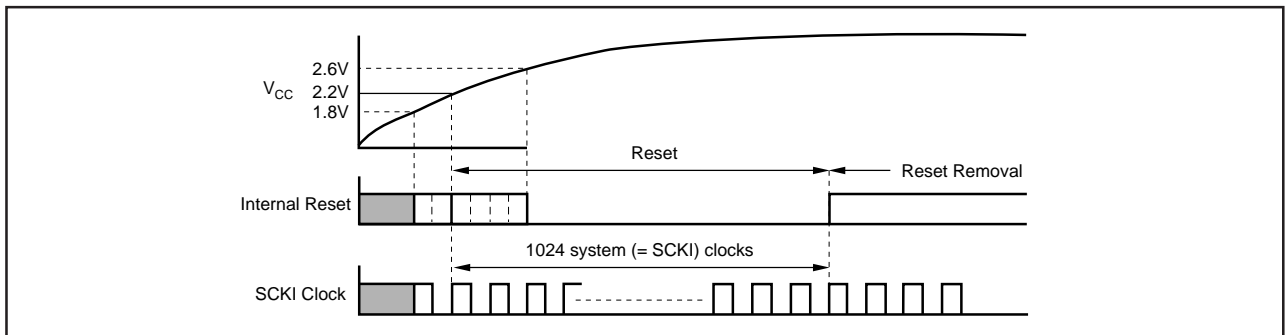


FIGURE 6. Internal Power-On Reset Timing.

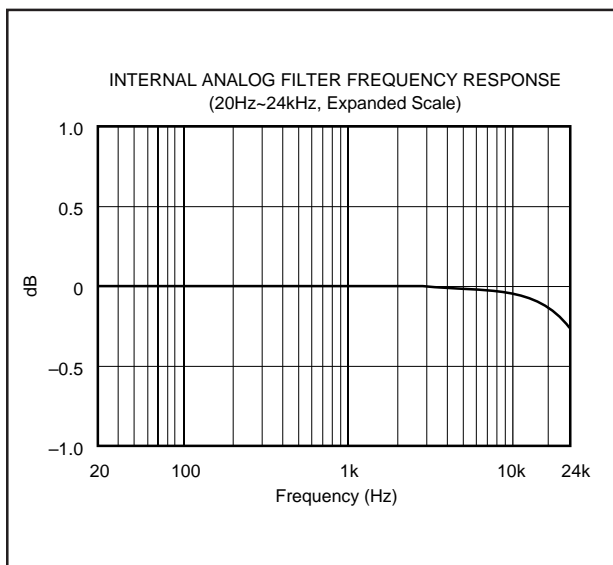


FIGURE 7. Low Pass Filter Frequency Response.

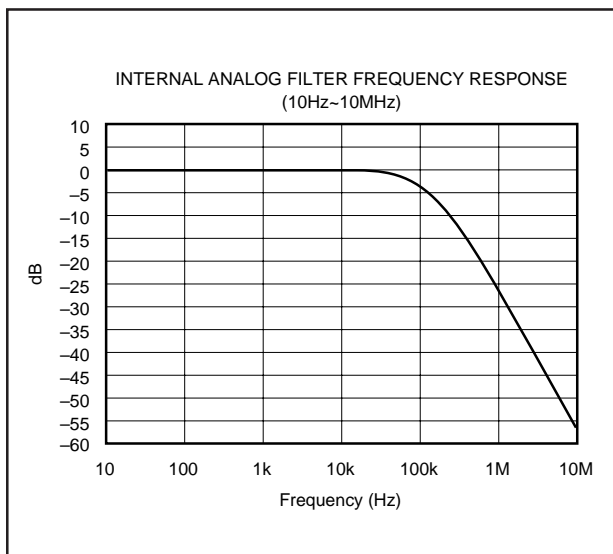


FIGURE 8. Low Pass Filter Wideband Frequency Response.

## APPLICATION CONSIDERATIONS

### DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1725:

$$T_D = 11.125 \times 1/f_S$$

$$\text{For } f_S = 44.1\text{kHz, } T_D = 11.125/44.1\text{kHz} = 251.4\mu\text{s}$$

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

### OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1725 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 7. The higher frequency rolloff of the filter is shown in Figure 8. If the user's application has the PCM1725 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 9. For some applications, a passive RC filter or 2nd-order filter may be adequate.

### BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. It is also recommended to include a 0.1μF ceramic capacitor in parallel with the 10μF tantalum bypass capacitor.

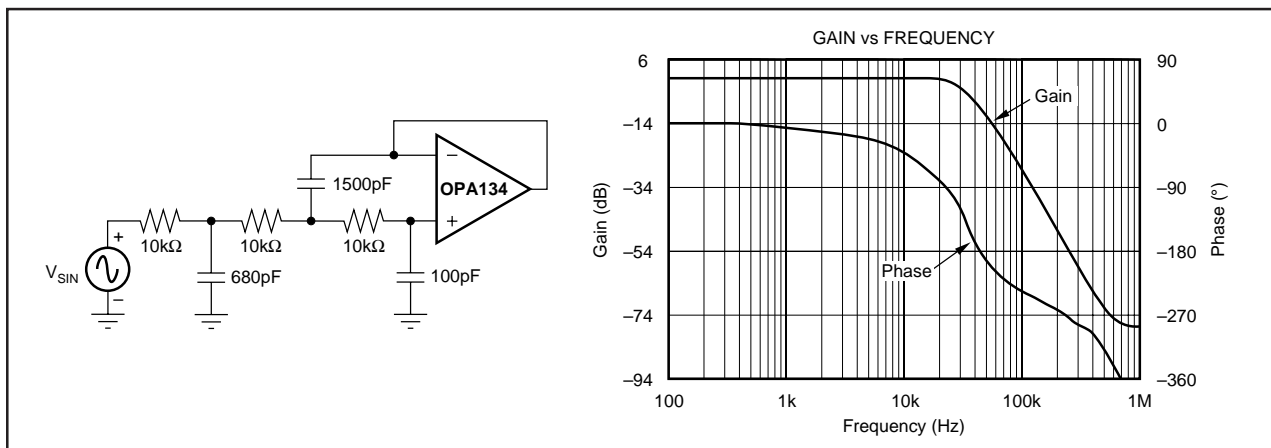


FIGURE 9. 3rd-Order LPF.



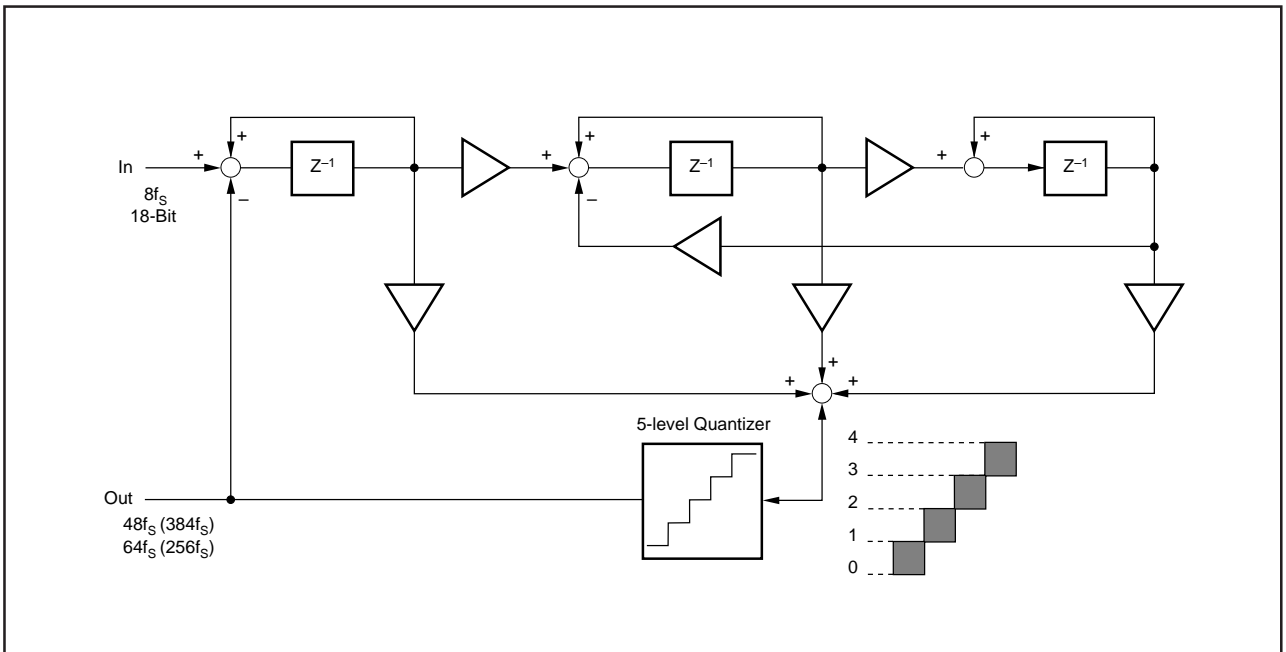


FIGURE 10. 5-Level  $\Delta\Sigma$  Modulator Block Diagram.

## THEORY OF OPERATION

The delta-sigma section of PCM1725 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 10. This 5-level delta-sigma modulator has the advantage of stability and clock jitter over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8X interpolation filter is  $96f_s$  for a  $384f_s$  system clock, and  $64f_s$  for a  $256f_s$  system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 11.

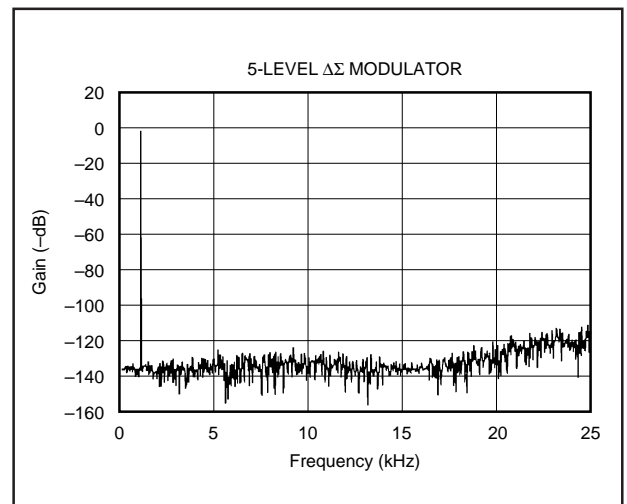


FIGURE 11. Quantization Noise Spectrum.