Dual Controllers - Step Down Synchronous PWM and Linear Controller

Features

- Provides Two Regulated Voltages
  - One Synchronous DC/DC Buck Controller
  - One Linear Controller
- 0.8V Internal Reference Voltage
  - Both Controllers: 0.8V ± 2% Line, Load and Temp.
- Output Voltage Range
  - PWM Controller : 0.8V to V_{IN}
  - Linear Controller : 0.8V to (12VCC-V_{GSpass})
- Full Duty Cycle Range for PWM Controller
  - 0% to 100%
- Internal Loop Compensation for PWM Controller
- Internal 2ms Soft Start and Short Circuit Protection for both Controllers
- Both Controllers Drive N-Channel MOSFETs
- Small Converter Size
  - 600kHz Constant Switching Frequency
  - Simple SO-14 Package
- Shutdown Control

Applications

- Motherboard
- Graphics Cards
- 12V, 5V and 3.3V Inputs DC-DC Converter
- DSP Supplies
- Embedded processor and I/O supplies

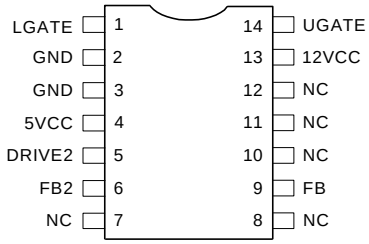
General Description

The APW7060 integrates a synchronous buck PWM controller and a linear controller to provide two regulated voltages in a single package. The PWM controller drives external N-channel MOSFETs and operates at a fixed 600kHz frequency. When the input supply drops close to the output, the upper MOSFET remains on, achieving 100% duty cycle. Internal loop compensation is optimized for fast transient response, eliminating external compensation network. The linear controller drives an external N-channel MOSFET to form a linear regulator. The internal 0.8V reference makes this part suitable for a wide variety of low voltage applications.

The APW7060 has an undervoltage lockout circuitry to ensures that both the 5VCC and 12VCC must be present before its internal circuitry is power up. Soft start is internally set to 2ms and will bring both outputs into regulation in a controlled manner. When either output goes into short, soft start will be initiated. If the short condition still remains after three cycles, both regulators will be shut down. To restart both regulators, recycle the voltage at 5VCC or 12VCC pin or momentarily pull the FB2 pin above 1.28V.

The APW7060 can be shutdown by pulling the FB2 pin above 1.28V. In shutdown, all gate drive signals will be low. This dual controller is available in SO-14 package.

Pinouts



Ordering and Marking Information

APW7060 □□-□□ Handling Code Temp. Range Package Code	Package Code K : SOP-14 Operating Junction Temp. Range C : 0 to 70°C Handling Code TU : Tube TR : Tape & Reel
APW7060 K : APW7060 XXXXX	XXXXX - Date Code

Block Diagram

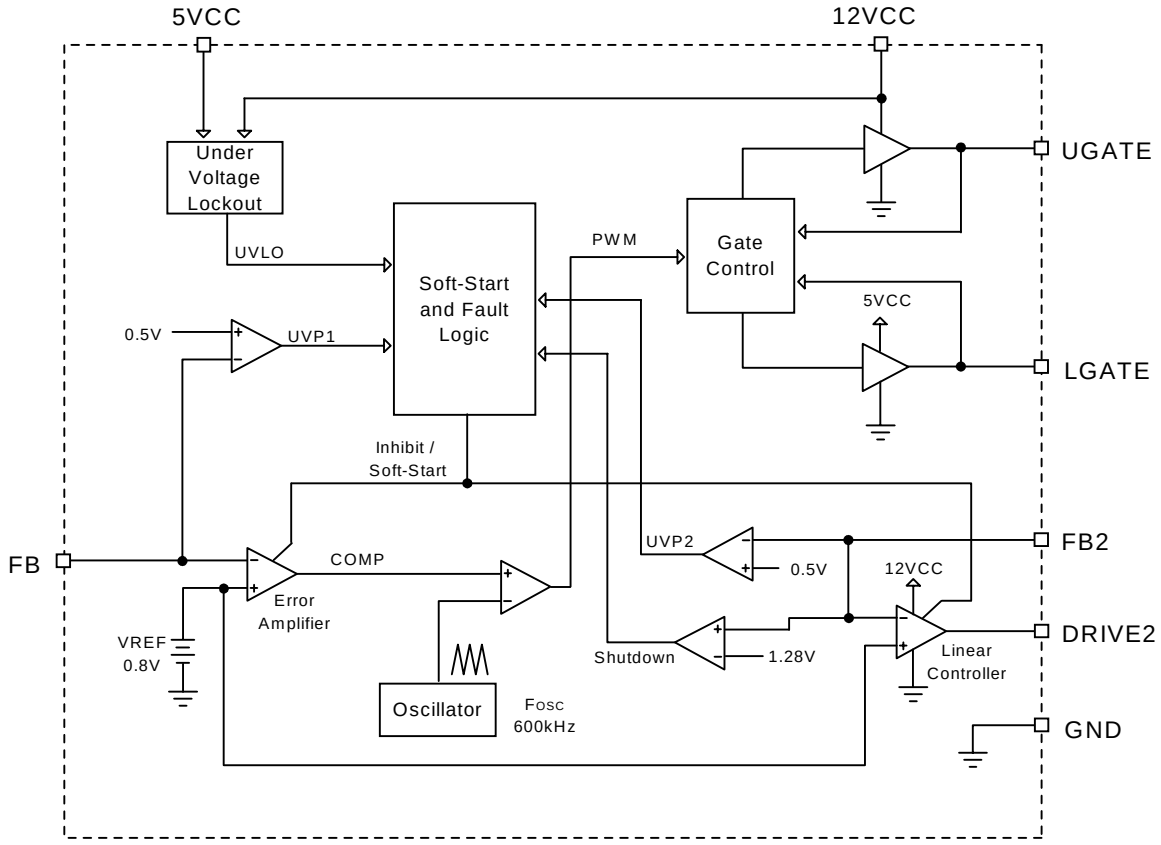
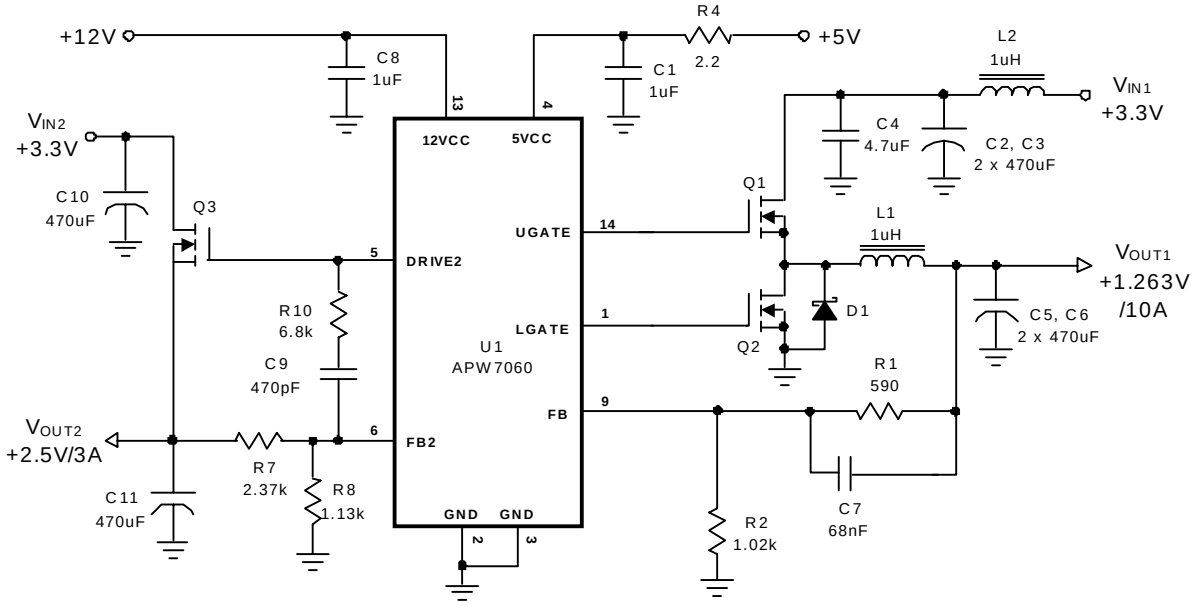


Figure 1.

Typical Application



Q1 : APM2014N UC

Q2 : APM2014N UC

Q3 : APM2055N UC

D1 : 3A Schottky Diode

C2, C3, C5, C6, C10, C11 : 470uF/6.3V, ESR=30mΩ

Figure 2.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
$5V_{CC}$	5VCC Supply Voltage (5VCC to GND)	-0.3 ~ 7	V
$12V_{CC}$	12VCC Supply Voltage (12VCC to GND)	-0.3 ~ 15	V
	UAGTE, DRIVE2 to GND	-0.3 ~ $12V_{CC}$	V
	LGATE, FB, FB2 to GND	-0.3 ~ $5V_{CC}$	V
	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Soldering Temperature, 10 Seconds	300	°C
V_{ESD}	Minimum ESD Rating (Human body model)	±2	KV

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (SOP-14)	160	°C/W

Recommended Operating Conditions (Note)

Symbol	Parameter	Range	Unit
$5V_{CC}$	5VCC Supply Voltage	5 ± 5%	V
$12V_{CC}$	12VCC Supply Voltage	12 ± 10%	V
V_{OUT1}	Output Voltage of the Buck converter	0.8 ~ 3.3	V
V_{IN1}	Input Voltage of the Buck converter	3.3/5 ± 5%	V
V_{OUT2}	Output Voltage of the Linear Regulator	0.8 ~ 3.3	V
V_{IN2}	Input Voltage of the Linear Regulator	3.3/5 ± 5%	V
T_A	Ambient Temperature	0 ~ 70	°C
T_J	Junction Temperature	0 ~ 125	°C

Note : Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over $5V_{CC}$=5V, $12V_{CC}$=12V and T_A= 0~70 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7060			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{CC}	5VCC Supply Current	LGATE Open, FB2=DRIVE2		2.5		mA
	12VCC Supply Current	UGATE Open		2.5		mA
UNDER VOLTAGE LOCKOUT						
	Rising 5VCC Threshold	$12V_{CC}$=12V	4.0	4.2	4.4	V
	Falling 5VCC Threshold	$12V_{CC}$=12V	3.5	3.7	3.9	V
	Rising 12VCC Threshold	$5V_{CC}$=5V	9.6	10.3	10.8	V
	Falling 12VCC Threshold	$5V_{CC}$=5V	9.3	9.7	10.2	V
OSCILLATOR						
F_{OSC}	Free Running Frequency		550	600	650	kHz
	Ramp Upper Threshold			2.85		V
	Ramp Lower Threshold			0.95		V
ΔV_{OSC}	Ramp Amplitude			1.9		V_{P-P}
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage			0.8		V
	System Accuracy	Over Line, Load and Temperature	-2		+2	%

Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $5V_{CC}$=5V, $12V_{CC}$=12V and T_A= 0~70 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7060			Unit
			Min	Typ	Max	
BUILT-IN PWM FEEDBACK COMPENSATION						
	DC Gain			75		dB
F_P	First Pole Frequency			10		Hz
F_Z	First Zero Frequency			1		kHz
	UGATE Duty Range		0		100	%
	FB Input Current				0.1	µA
PWM CONTROLLER GATE DRIVERS						
	UGATE Source	V_{UAGTE}=1V		0.6		A
	UGATE Sink	V_{UGATE}=1V		7.3		Ω
	LGATE Source	V_{LGATE}=1V		0.6		A
	LGATE Sink	V_{LGATE}=1V		1.8		Ω
T_D	Dead Time			50		nS
LINEAR CONTROLLER						
	DC Gain			78		dB
	Gain Bandwidth Product	C_L=0.5nF		1.6		MHz
		C_L=1nF		1		
	FB Input Current				0.1	µA
	DRIVE2 Source Current	$V_{FB2}=V_{REF}$-20mV, V_{DRIVE2}=7V		9.8		mA
	DRIVE2 Sink Current	$V_{FB2}=V_{REF}$+20mV, V_{DRIVE2}=3V		2.6		mA
	DRIVE2 Output High Voltage	DRIVE2 Open		11.7		V
	DRIVE2 Output Low Voltage	DRIVE2 Open		0.01		V
UNDER-VOLTAGE PROTECTION						
UV_{FB}	FB/FB2 Under-Voltage Level	FB or FB2 Falling		0.5		V
	FB/FB2 Under-Voltage Hysteresis			15		mV
SOFT-START AND SHUTDOWN						
T_{SS}	Soft-Start Interval			2		mS
	FB2 Shutdown Threshold	FB2 Rising		1.28		V
	FB2 Shutdown Hysteresis			30		mV

Functional Pin Description

LGATE (Pin 1)

This pin provides the gate drive signal for the low side MOSFET .

GND (Pin 2, 3)

Signal and power ground for the IC. All voltage levels are measured with respect to this pin. Tie this pin to the ground plane through the lowest impedance connection available.

5VCC (Pin 4)

This is the main bias supply for the DC/DC controller and its low side MOSFET driver. Must be closely decoupled to GND (Pin 2,3). The voltage at this pin is monitored for undervoltage lockout (UVLO) purposes. **DO NOT** apply a voltage greater than 5.5V to this pin.

DRIVE2 (Pin 5)

This pin provides the gate drive voltage for the linear regulator N-channel MOSFET pass transistor. It also provides a means of compensating the linear controller for applications where the user needs to optimize the regulator transient response.

FB2 (Pin 6)

Connect this pin to the output (V_{OUT2}) of the linear regulator via a proper sized resistor divider. The voltage at this pin is regulated to 0.8V and the V_{OUT2} is determined using the following formula :

$$V_{OUT2}=0.8V \times (1+\frac{R7}{R8})$$

where R7 is the resistor connected from V_{OUT2} to FB2, and R8 is the resistor connected from FB2 to GND. This pin is also monitored for under-voltage events. Pulling and holding FB2 above 1.28V shuts down both regulators. Releasing FB2 initiates soft-start on both regulators.

NC (Pin 7, 8, 10, 11, 12)

No internal connection.

FB (Pin 9)

This pin is the inverting input of the internal error amplifier of the buck controller. Connect this pin to the output (V_{OUT1}) of the DC/DC converter via a proper sized resistor divider to form a complete feedback loop. The V_{OUT1} is determined using the following formula :

$$V_{OUT1}=0.8V \times (1+\frac{R1}{R2})$$

where R1 is the resistor connected from V_{OUT1} to FB, and R2 is the resistor connected from FB to GND. This pin is also monitored for under-voltage events.

12VCC (Pin 13)

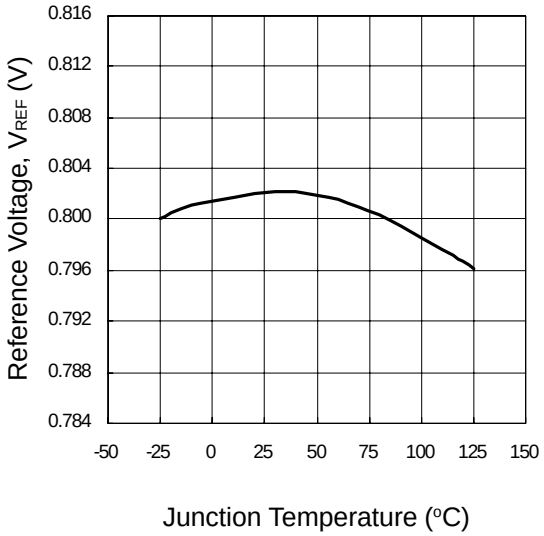
This pin provides the supply voltage to the high side MOSFET driver and the linear controller. A voltage no greater than 13V can be connected to this pin. The voltage at this pin is monitored for undervoltage lockout (UVLO) purposes.

UGATE (Pin 14)

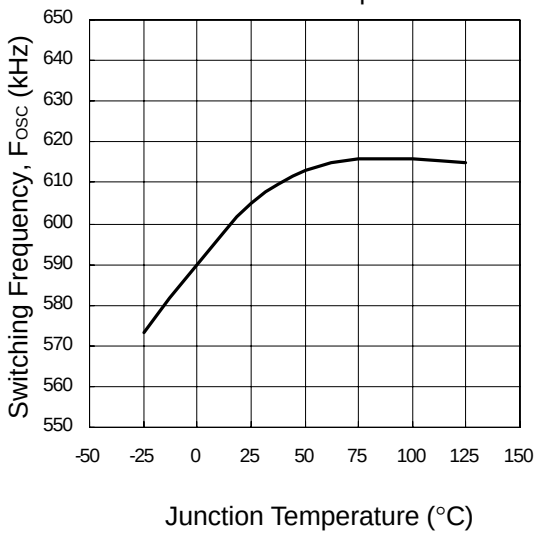
This pin provides gate drive for the high-side MOSFET.

Typical Characteristics

Reference Voltage
vs. Junction Temperature



Switching Frequency
vs. Junction Temperature

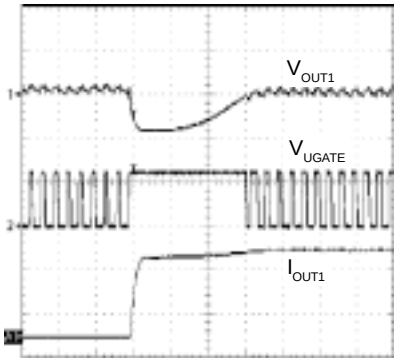


Operating Waveforms (Refer to the typical application circuit)

1.V_{OUT1} Load Transient Response : I_{OUT} = 0A -> 10A -> 0A

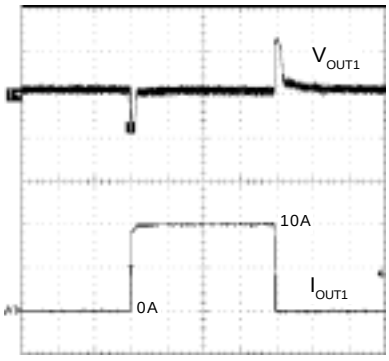
- I_{OUT1} slew rate = ±10A/µS

I_{OUT} = 0A -> 10A



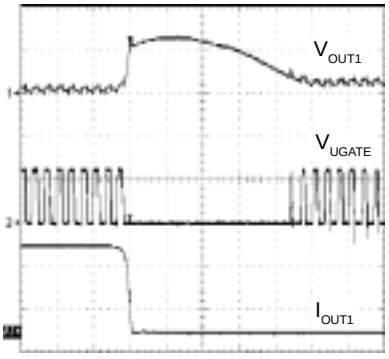
Ch1 : V_{OUT1}, 100mV/Div, DC,
Offset = 1.25V
Ch2 : V_{UGATE}, 10V/Div, DC
Ax1 : I_{OUT1}, 5A/Div
Time : 5µS/Div
BW = 20MHz

I_{OUT} = 0A -> 10A -> 0A



Ch1 : V_{OUT1}, 100mV/Div, DC,
Offset = 1.25V
Ax1 : I_{OUT1}, 5A/Div
Time : 100µS/Div
BW = 20MHz

I_{OUT} = 10A -> 0A

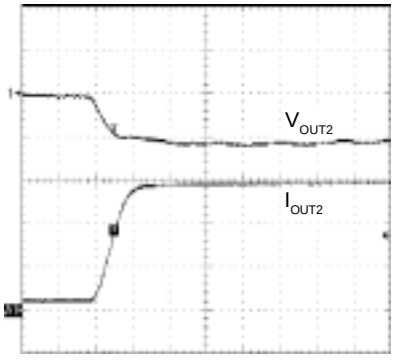


Ch1 : V_{OUT1}, 100mV/Div, DC,
Offset = 1.25V
Ch2 : V_{UGATE}, 10V/Div, DC
Ax1 : I_{OUT1}, 5A/Div
Time : 5µS/Div
BW = 20MHz

2.V_{OUT2} Load Transient Response : I_{OUT} = 0.2A -> 3A -> 0.2A

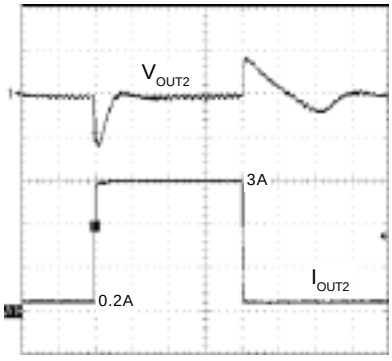
- I_{OUT2} slew rate = ±3A/µS

I_{OUT} = 0.2A -> 3A



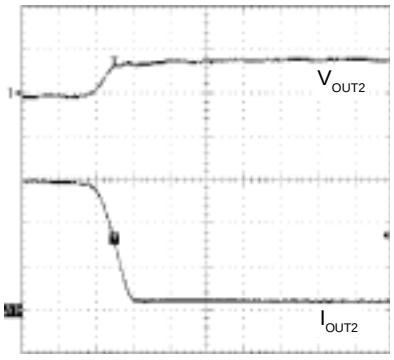
Ch1 : V_{OUT2}, 50mV/Div, DC,
Offset = 2.50V
Ax1 : I_{OUT2}, 1A/Div
Time : 1µS/Div
BW = 20MHz

I_{OUT} = 0.2A -> 3A -> 0.2A



Ch1 : V_{OUT2}, 50mV/Div, DC,
Offset = 2.50V
Ax1 : I_{OUT2}, 1A/Div
Time : 50µS/Div
BW = 20MHz

I_{OUT} = 3A -> 0.2A

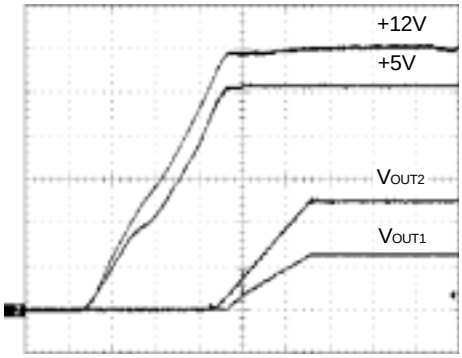


Ch1 : V_{OUT2}, 50mV/Div, DC,
Offset = 2.50V
Ax1 : I_{OUT2}, 1A/Div
Time : 1µS/Div
BW = 20MHz

Operating Waveforms (Cont.)

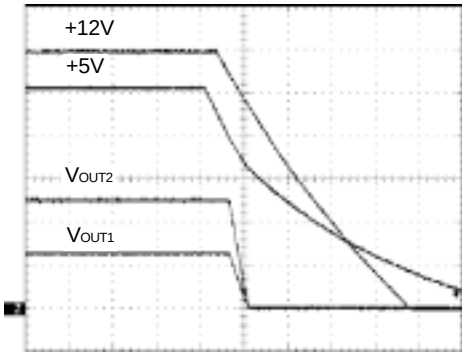
3. Powering ON / OFF

Soft-start at Powering ON



Ch1 : +5V, 1V/Div, DC
Ch2 : +12V, 2V/Div, DC
Ch3 : V_{OUT1}, 1V/Div, DC
Ch4 : V_{OUT2}, 1V/Div, DC
Time : 1mS/Div
BW = 20MHz

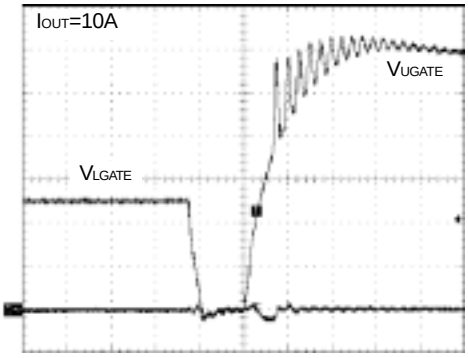
Powering OFF



Ch1 : +5V, 1V/Div, DC
Ch2 : +12V, 2V/Div, DC
Ch3 : V_{OUT1}, 1V/Div, DC
Ch4 : V_{OUT2}, 1V/Div, DC
Time : 5mS/Div
BW = 20MHz

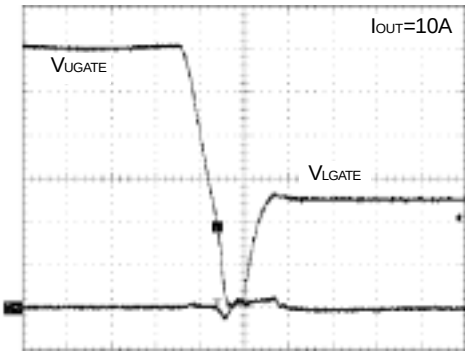
4. UGATE and LGATE

UGATE Rising



Ch1 : V_{UGATE}, 2V/Div, DC
Ch2 : V_{LGATE}, 2V/Div, DC
Time : 50nS/Div
BW = 500MHz

UGATE Falling



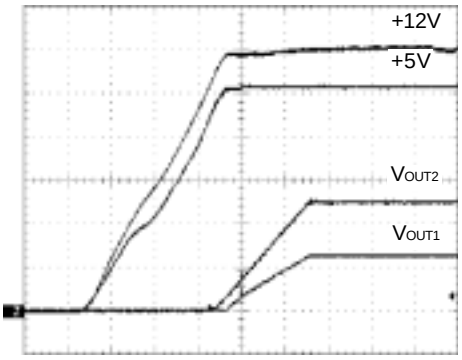
Ch1 : V_{UGATE}, 2V/Div, DC
Ch2 : V_{LGATE}, 2V/Div, DC
Time : 50nS/Div
BW = 500MHz

Application Information

Soft Start

Soft start can be initiated in several ways. One way is when the input bias supply to the 5VCC and 12VCC is above 4.2V and 10.2V respectively. The other way is when the part comes out of shutdown. In both ways, the soft start cycle will last for 2ms. During this period, the reference to the error amplifier of the PWM controller and linear controller will gradually slew up to its final value of 0.8V. This effectively will force both output voltages to track this reference ramp rate. Hence both outputs will reach regulation at the same time. Figure 3 illustrates this graphically.

Soft-start at Powering ON



Ch1 : +5V, 1V/Div, DC
Ch2 : +12V, 2V/Div, DC
Ch3 : V_{OUT1}, 1V/Div, DC
Ch4 : V_{OUT2}, 1V/Div, DC
Time : 1mS/Div
BW = 20MHz

Figure 3.

Linear Regulator Transient Response Optimization

The linear regulator is stable over all load current. However, the transient response can be further enhanced by connecting a RC network between the FB2 and DRIVE2 pin. Depending on the output capacitance and load current of the application, the value of this RC network is then varied. A good starting point for the resistor value is 6.8kΩ and 470pF for the capacitor.

Maximum Output Voltage of Linear Controller

The maximum drive voltage at DRIVE2 is determined by the applied voltage at 12VCC pin. Since this pin drives an external N-channel pass MOSFET, therefore the maximum output voltage of the linear regulator is dependent upon the required gate-to-source voltage to sustain the load current.

$$V_{OUT2MAX} = 12VCC - V_{GSpass}$$

Component Selection Guidelines

PWM Regulator Output Capacitor

The selection of C_{OUT} is determined by the required effective series resistance (ESR) and voltage rating rather than the actual capacitance requirement. Therefore select high performance low ESR capacitors that are intended for switching regulator applications. In some applications, multiple capacitors have to be paralled to achieve the desired ESR value. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

For high frequency decoupling, a ceramic capacitor between 0.1uF to 1uF can be connected between 5VCC and ground pin.

Application Information

Inductor Selection

The inductance of the inductor is determined by the output voltage requirement. The larger the inductance, the lower the inductor's current ripple. This will translate into lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{Fs \times L} \times \frac{V_{OUT}}{V_{IN}}$$

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

where Fs is the switching frequency of the regulator.

There is a tradeoff exists between the inductor's ripple current and the regulator load transient response time A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current and vice versa. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current.

Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some type of inductors, especially core that is make of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

PWM Regulator MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}) and maximum output current requirement.The losses in the MOSFETs have two components: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following :

$$P_{UPPER} = I_{out}^2 (1+ TC)(R_{DS(ON)})D + (0.5)(I_{out})(V_{IN})(t_{sw})F_S$$

$$P_{LOWER} = I_{out}^2 (1+ TC)(R_{DS(ON)})(1-D)$$

where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_S is the switching frequency

t_{sw} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the upper MOSFET include an additional transition loss.The switching internal, t_{sw}, is a function of the reverse transfer capacitance C_{RSS}. Figure 4 illustrates the switching waveform of the MOSFET.

The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

Linear Regulator Input/Output Capacitor Selection

The input capacitor is chosen based on its voltage rating. Under load transient condition, the input capacitor will momentarily supply the required transient current. A 1uF ceramic capacitor will be sufficient in most applications.

The output capacitor for the linear regulator is chosen to minimize any droop during load transient condition. In addition, the capacitor is chosen based on its voltage rating.

Linear Regulator MOSFET Selection

In addition to choosing the pass MOSFET for its ability to sustain the load current requirement (see Maximum Output Voltage of Linear Controller), another criteria is its efficiency of heat removal. The power dissipated by the MOSFET is given by:

$$Pdiss = Iout * (V_{IN} - V_{OUT2})$$

Application Information

where Iout is the maximum load current

V_{out2} is the nominal output voltage

In some applications, heatsink maybe required to help maintain the junction temperature of the MOSFET below its maximum rating.

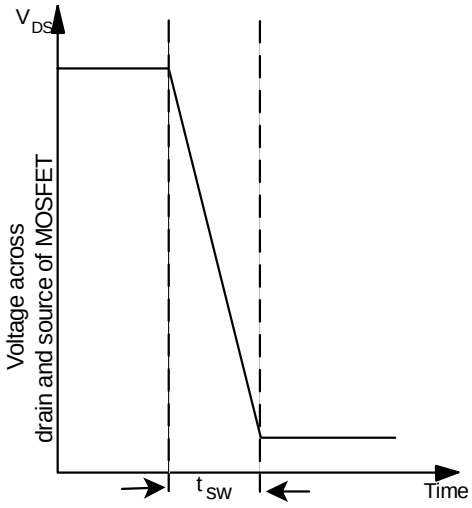


Figure 4. Switching waveform across MOSFET

Layout Considerations

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator. In general, interconnecting impedances should be minimized by using short, wide printed circuit traces. Signal and power grounds are to be kept separate and finally combined using ground plane construction or single point grounding. Figure 5 illustrates the layout, with bold lines indicating high current paths. Components along the bold lines should be placed close together. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE and the PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. There fore keep traces to these nodes as short as possible.
- Decoupling capacitor C_{IN} provides the bulk capaci tance and needs to be placed close to the drain of Q1.
- The ground return of C_{IN} must return to the combine C_{OUT} (-) terminal.
- Capacitor $C_{HF}$is to improve noise performance and a small 1uF ceramic capacitor will be sufficient. Place this capacitor close of the drain of Q1.
- Inductor L1 should be connected closely to the PHASE node.
- Bypass capacitors, C_{BP}, should be placed as close to the 5VCC and 12VCC pins.

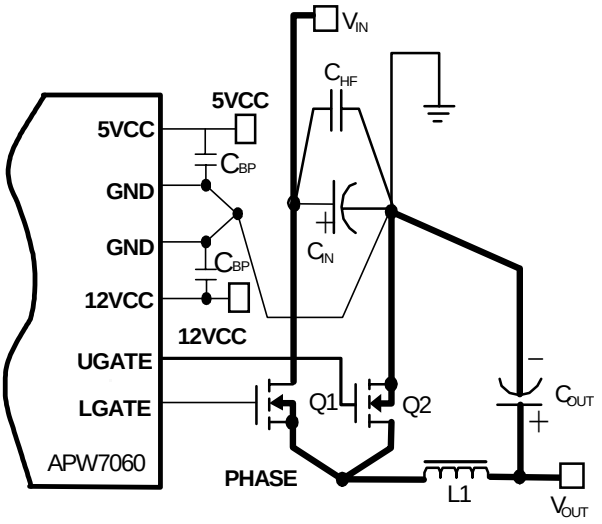
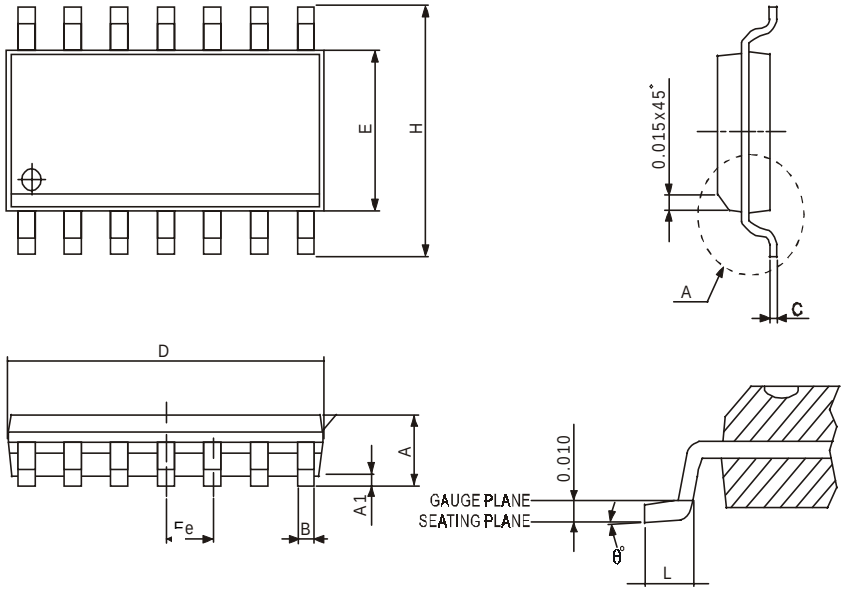


Figure 5. Recommended Layout Diagram

Package Information

SOP – 14 (150mil)



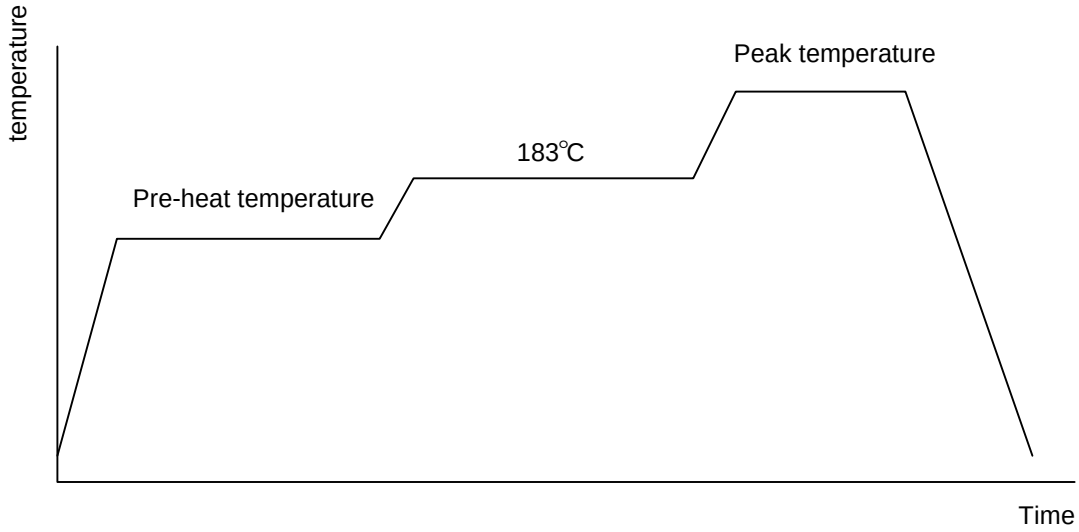
Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.477	1.732	0.058	0.068
A1	0.102	0.255	0.004	0.010
B	0.331	0.509	0.013	0.020
C	0.191	0.2496	0.0075	0.0098
D	8.558	8.762	0.336	0.344
E	3.82	3.999	0.150	0.157
e	1.274		0.050	
H	5.808	6.215	0.228	0.244
L	0.382	1.274	0.015	0.050
θ°	0°	8°	0°	8°

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.
Packaging	2500 devices per reel

Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A APRIL 1999



Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183 ℃ to Peak)	3 ℃/second max.	10 ℃ /second max.
Preheat temperature 125 ± 25 ℃)	120 seconds max.	
Temperature maintained above 183 ℃	60 ~ 150 seconds	
Time within 5 ℃ of actual peak temperature	10 ~ 20 seconds	60 seconds
Peak temperature range	220 +5/-0 ℃ or 235 +5/-0 ℃	215~ 219 ℃ or 235 +5/-0 ℃
Ramp-down rate	6 ℃ /second max.	10 ℃ /second max.
Time 25 ℃ to peak temperature	6 minutes max.	

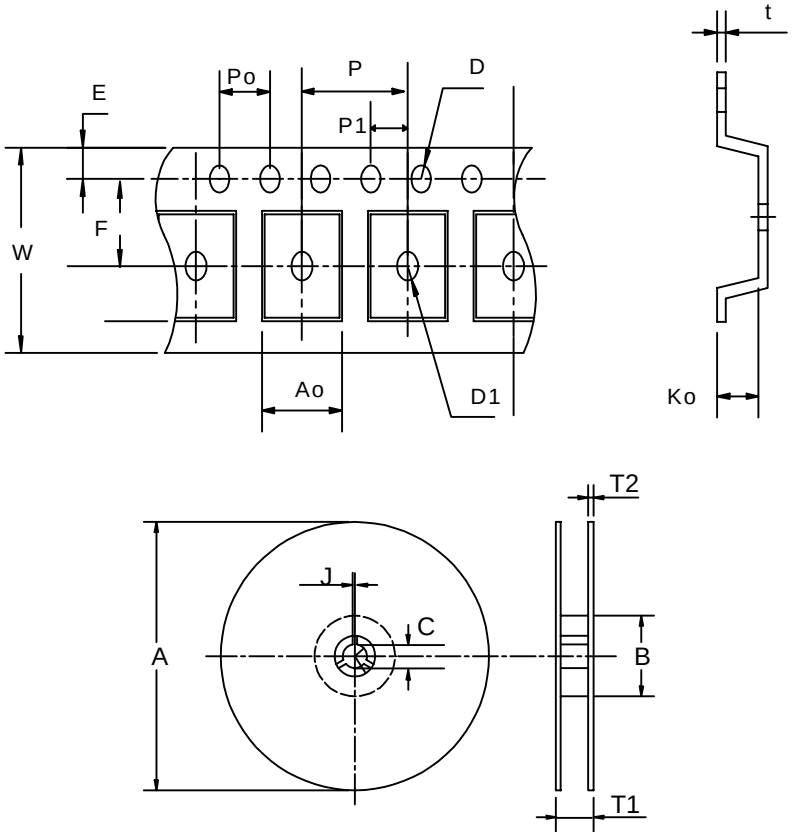
Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bags	pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm	pkg. thickness < 2.5mm and pkg. volume <
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Carrier Tape & Reel Dimension



Application	A	B	C	J	T1	T2	W	P	E
SOP-14 (150mil)	330REF	100REF	13.0 + 0.5 - 0.2	2 ± 0.5	16.5REF	2.5 ± 025	16.0 ± 0.3	8	1.75
	F	D	D1	Po	P1	Ao	Ko	t	
	7.5	ϕ0.50 + 0.1	ϕ1.50 (MIN)	4.0	2.0	6.5	2.10	0.3±0.05	

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 14	24	21.3	2500

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