GL518SM Microprocessor System Hardware Monitor

General Descriptionn

The GL518SM is a low-cost and highly integrated circuit designed in CMOS technology which serves as a hardware monitor of any microprocessor based system. The GL518SM can be used to monitor temperatures, power supply voltages and fan speeds in a PC system. By connecting to an external thermistor for remote sensing applications, the GL518SM allows more flexibility in location of the sensor. The GL518SM will generate interrupts and drive different square-like wave which allows the speaker to sound the alarm when it detects the abnormal situation. Through the I^2C bus interface, the host can program the temperature trip points and query the GL518SM about the interrupt status, current temperature, voltage and fan speed.

Features

- Remote temperature sensing scheme
- External thermistor for remote sensing
- Wide temperature detection range: -10°C to +110°C
- Programmable hysteresis and temperature set point
- 4 positive voltage monitored
- 1 voltmeter
- 2 fan speed monitored
- Auto CPU fan on/off control
- 4 types of speaker-driven signal output
- I^2C serial bus interface
- Readback capability of temperature, voltmeter and fan speed
- 16-pin SO plastic package

Key Specifications

• Supply Voltage	5 V
• Temperature Accuracy (-10°C to +110°C)	± 3 °C (max)
• Voltage Accuracy (at VIN1, VIN2 and VIN3)	± 60 mV (max)
(at AVDD)	± 75 mV (max)

Note: the measuring accuracy is based on neglecting the errors of external thermistors, linearizing and scaling resistors.

Pinning Diagram

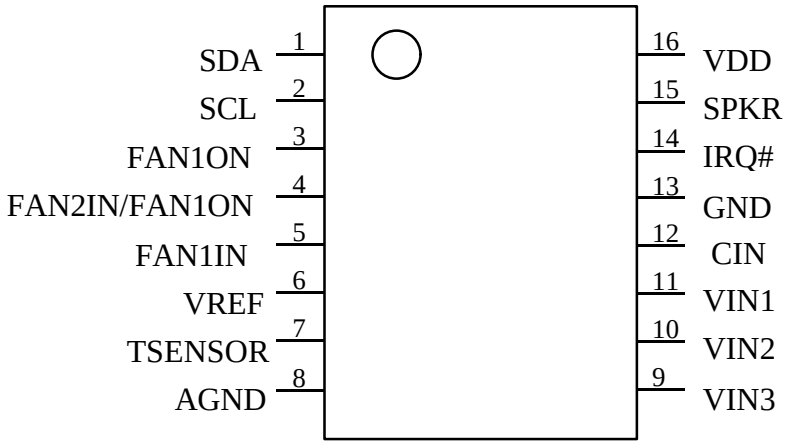


Figure 1. GL518SM pinning diagram

Pin Description

PIN	MNEMONIC	TYPE	FUNCTION
1	SDA	Digital I/O	I²C-bus serial data input/output (open drain)
2	SCL	Digital Input	I²C-bus serial clock input
3	FAN1ON	Digital Output	An active high output to turn on cooling fan 1. The output goes low while temperature is below 25°C and goes high while over 30°C. This pin is as input for user-set I²C address A0 during power on reset.
4	FAN2IN / FAN1ON	Digital I/O	Fan 2 tachometer input with amplitude 0 to VDD or Fan1 on/off auto control. This pin is multiplxed programmably, default is FAN2IN.
5	FAN1IN	Digital Input	Fan 1 tachometer input with amplitude 0 to VDD.
6	VREF	Analog I/O	Voltage reference for external thermistor
7	TSENSOR	Analog I/O	Connected to an external sensor circuit.
8	AGND	—	Analog Ground.
9	VIN3	Analog Input	Analog voltage input to be monitored.
10	VIN2	Analog Input	Analog voltage input to be monitored.
11	VIN1	Analog Input	Analog voltage input to be monitored.
12	CIN	Analog Input	Connected to an external capacitor.
13	GND	—	Ground
14	IRQ#	Digital Output	An active low output to indicate abnormal situation

			(open drain)
15	SPKR	Digital I/O	Output one of 4 types speaker-driven signal dependent on detected abnormal situation caused by temperature, voltage input and fan speed.
16	VDD	—	+5.0V power, bypass with 0.1µF capacitors.

Absolute Maximum Ratings

Positive Supply Voltage (VDD)	6.5V
Voltage on Any Input or Output Pin (except analog inputs)	-0.3V to (VDD+0.3V)
Ground Difference (GND-AGND)	±300mV
Input Current at Any Pin	±5mA
Package Input Current	± 20mA
Maximum Junction Temperature	150°C
ESD Human Body Model	2 kV

Operating Ratings

Operating Temperature Range	-40°C to +125°C
Supply Voltage (VDD)	+4.25V to +5.75V
Ground Difference (GND-AGND)	±100mV
V_{IN} Voltage Range	-0.05V to (VDD+0.05V)

DC Electrical Characteristics

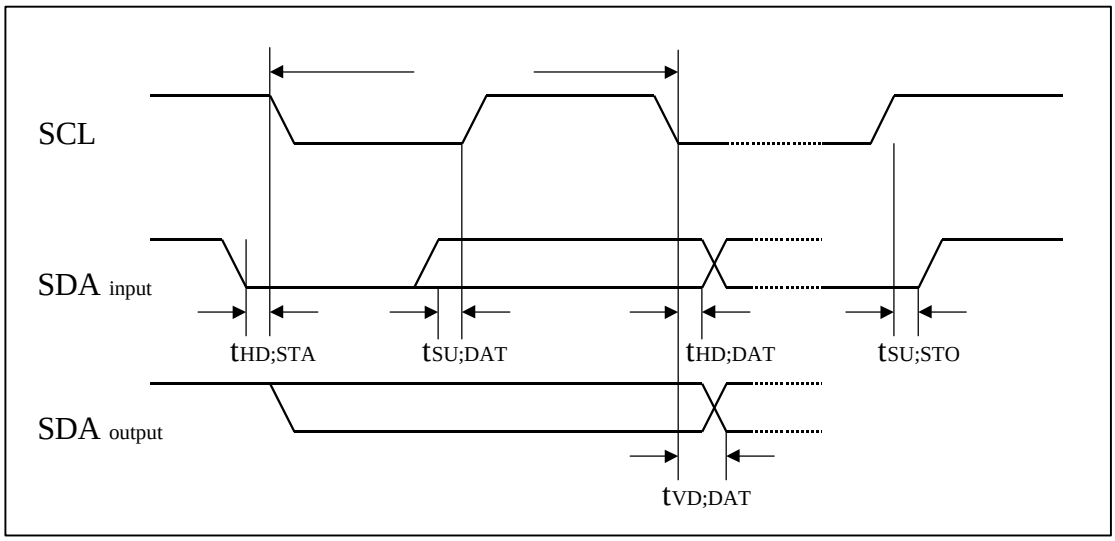
Symbol	Parameter	Conditions	Typical	Limits	Units
Power Supply Characteristics					
Icc	Supply Current		2.4	3.0	mA(max)
Analog-to-Digital Converter Characteristics					
TUE	Total Unadjusted Error			±2	%(max)
t_C	Total Monitoring Cycle Time		1.024		sec
Fan RPM-to-Digital Converter Characteristics (based on 2 pulses per revolution of the fan tachometer output)					
	Full-scale Count			255	(max)
	FAN1 and FAN2 Nominal Input RPM	Divisor =1, Fan Count = 60	8000		RPM
		Divisor = 2, Fan Count = 60	4000		RPM
		Divisor = 4, Fan Count = 60	2000		RPM

		Divisor = 8, Fan Count = 60	1000		RPM
Oscillator Frequency (CIN)					
f_{CIN}		-10°C < TA < +110°C	32		kHz
Digital Outputs (FAN1ON, FAN2IN/FAN1ON, SPKR)					
$V_{OUT(H)}$	Logical '1' Output Voltage	I_{OUT} = ±5.0 mA		2.4	V(min)
$V_{OUT(L)}$	Logical '0' Output Voltage	I_{OUT} = ±5.0 mA		0.4	V(max)
Open Drain Digital Outputs (SDA, IRQ#)					
$V_{OUT(L)}$	Logical '0' Output Voltage	I_{OUT} = -5.0 mA		0.4	V(min)
$I_{OUT(H)}$	High Level Output Current	V_{OUT} = +5.0V	0.1	100	µA(max)
Digital Inputs (FAN1IN, FAN2IN/FAN1ON)					
$V_{IN(H)}$	Logical '1' Input Voltage			2.5	V(min)
$V_{IN(L)}$	Logical '0' Input Voltage			0.8	V(max)
Serial Bus Digital Inputs (SCL, SDA)					
$V_{IN(H)}$	Logical '1' Input Voltage			2.3	V(min)
$V_{IN(L)}$	Logical '0' Input Voltage			0.6	V(max)

AC Electrical Characteristics

PARAMETER	SYMBOL	MIN.	MAX.	UIITS
SCL clock frequency	$1/f_{SCL}$	—	400	kHz
Data in set-up time	$t_{SU;DAT}$	100	—	ns
Data in hold time	$t_{HD;DAT}$	0	—	ns
SCL low to data out valid	$t_{VD;DAT}$	100	—	ns
Start condition hold time	$t_{HD;STA}$	100	—	ns
Stop condition set-up time	$t_{SU;STO}$	100	—	ns

Figure 2. Serial Bus Timing Diagram



Functional Description

1. I^2C interface

The GL518SM is a slave device on the I^2C bus with a 7-bit slave address. The six most significant bits of the slave address are “010110”, hard wired inside the chip. The LSB A0 of the address is set by pulling the pin3 high for a one, or pulling down for a zero during power on reset.

2. Analog voltage inputs

The monitored power supplies should be arranged from 0 to 4.0V. In other words, the voltage 0 to 4.0V can be directly connected to the voltage input, whereas the voltage above 4.0V, such as +12V, should be attenuated below 4.0V before connected to the chip. The VDD (5.0V) of GL518SM is self-monitored after attenuated to 2.0V within the chip. The input voltage drift range is programmable individually, where only the voltage level from VIN3 is readable by I^2C bus interface. If the input voltage drifts beyond its desired value, GL518SM will send an interrupt request and drive square-like signal to indicate the bad power supply is detected.

While the voltage drift range (the upper and lower limit of VIN1, VIN2, VIN3 and VDD) is programmed or voltmeter register is read, the voltage is determined according to:

$$\text{Voltage Level (in V)} = \text{Register Value} \times \text{ADC Resolution (in V)},$$

where the “ADC Resolution” is 19 mV.

Note that the “Voltage Level” means the voltage level exactly at the pin VIN1, VIN2 or VIN3. If the power supply to be monitored is over 4.0V as mentioned, the “Voltage Level” will mean the attenuated voltage at input pins. For VDD(+5V) monitoring, the analog input level is taken as 4.0V for it is pre-attenuated internally. Some examples about accessing the analog associated registers are shown below.

Example 1. How to get the actual voltage from the “Voltmeter” register?

If the voltmeter register is A0h, it means the voltage at VIN3 is 3.04V.

Example 2. How to set the voltage limit register when the power supply is greater than 4.0V?

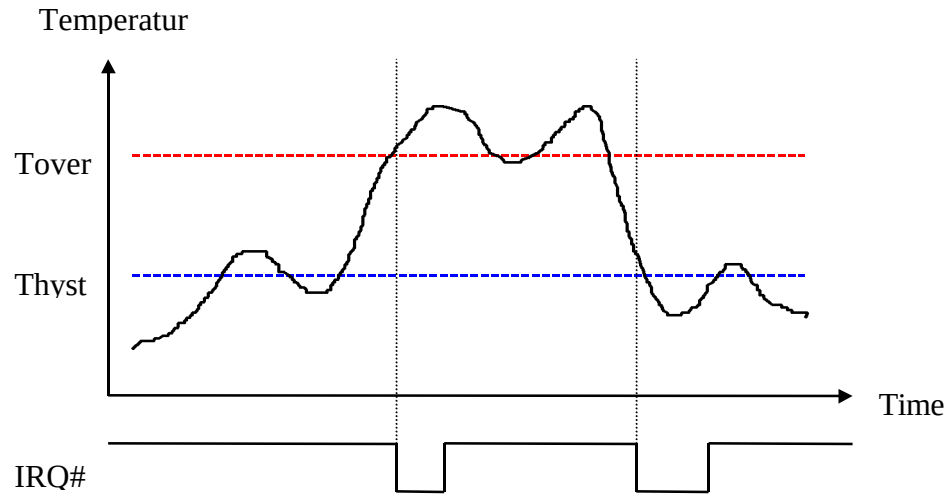
Assume the monitored voltage is 12V and attenuated to 3V before connected to VIN2. The voltage limit will be 2.85V~3.15V if ±5% drift range is presumed. Therefore the register Vin2_lmtl and Vin2_lmth should be 96h and A5h respectively.

Example 3. How to set the voltage limit register of VDD?
Assume the ±5% drift range of VDD is set, the voltage limit will be 3.8V~4.2V for the attenuated analog input of VDD is taken as 4.0V internally. Therefore the register VDD_lmtl and VDD_lmth should be C8h and DDh respectively.

3. Temperature sensing scheme with an external thermistor
The temperature sensing scheme of GL518SM supports two interrupt modes, "Interrupt" and "Comparator" mode. The default is "Comparator" mode.

(1) "Interrupt" mode:
The temperature over Tover causes an interrupt that will not deassert until reset by reading Interrupt Status Register. Another interrupt will occur if the temperature goes below Thyst. Again it will remain active indefinitely until reset by reading Interrupt Status Register.

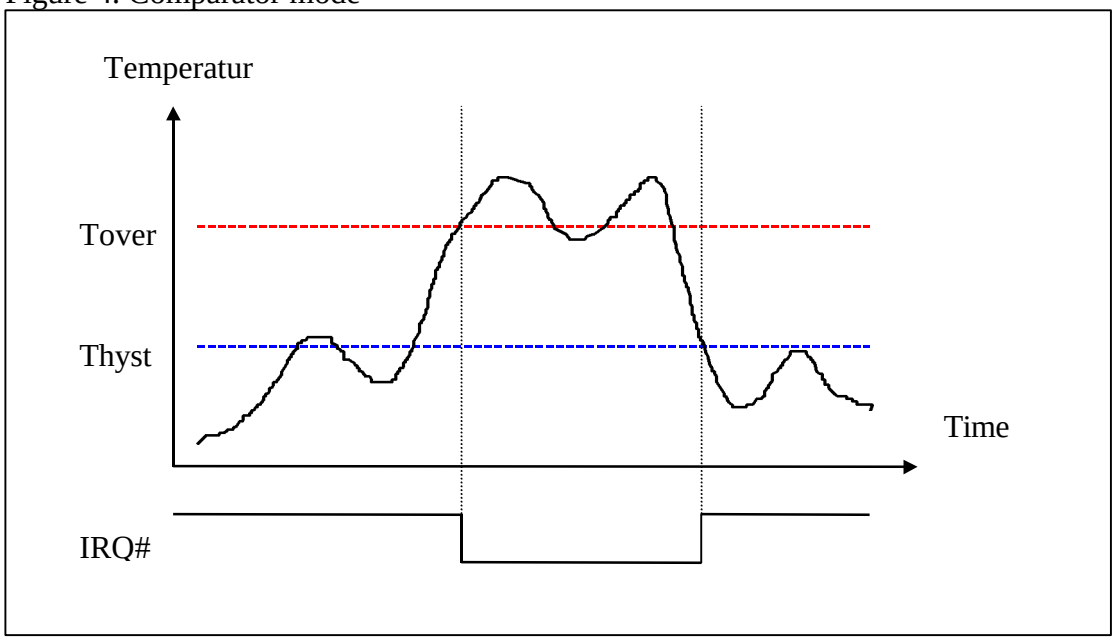
Figure 3. Interrupt mode



Note: IRQ# deasserts only when Interrupt Status Register is read.

(2) "Comparator" mode:
In this mode, the IRQ# signal behaves like a thermostat which goes low when temperature exceeds the Tover limit, and goes high when the temperature drops below Thyst limit. The interrupt will deassert after the Interrupt Status Register is read, whereas the next detect will set the interrupt again until the temperature is below Thyst.

Figure 4. Comparator mode



4. Temperature Data Format

The temperature data is represented in an unsigned 8-bit number, which maps the measured temperature in °C by subtracting an offset. The data format applies to all the registers associated with temperature including “Temperature”, “Temp_Over” and “Temp_Hyst”. The actual temperature can be represented in the following equation:

Temperature (°C) = Register Value - Offset,

where the Offset in decimal is 119 for temperature associated registers.

5. On/Off of Cooling fan

When the internal register bit Fan1auto is set to one, the auto control of fan 1 is enabled where the on/off of fan 1 is determined by the temperature sensed by the external thermister. In this mode, the pin FAN1ON goes high if temperature is over 30°C and goes low if under 25°C. The pin FAN1ON outputs high if the auto control is disabled. In thermal management, FAN1ON output can be used to automatically turn a cooling fan on or off .

6. Fan Inputs

The Fan Inputs are sampled by an internal 16 KHz clock. The maximum count for one period of the fan input is 255. The default divisor is set to 8 and the default count limit is 64h for both monitored fans. For a fan with 2 pulses per revolution, the default

setting provides a lower speed limit of 600 rpm. The fan speed is determined according to:

$$RPM = 960000 / (Count * Divisor * p),$$

where p is the pulse number per revolution for the monitored fan.

7. Speaker-driven output SPKR

The pin SPKR sends square-like wave to drive PC speaker in different tone if the abnormal situation of system is detected. There are 4 sounds to differentiate the abnormal situation including user-defined event, power alarm, temperature alarm and cooling fan alarm.

8. Register Access

The data registers in GL518SM are selected by the Pointer register which resets to 00h after power on and stores whatever the last contents it was set to. Writing to the GL518SM will always consist of the I^2C bus address byte, the Pointer byte and then the data byte.

Reading the GL518SM may take place in two cases:

i. If the Pointer register needs unchanged, the read can simply consist of an address byte, followed by the data byte sent from the GL518SM.
ii. If the Pointer register needs to be set, then the read will proceed by first writing to the GL518SM with the address byte, followed by the Pointer byte. Then an I^2C bus repeated start, followed by the data byte sent form the GL518SM will accomplish the read.

If a two-byte register is to be accessed, the first data byte is always the most significant byte and the second, the least significant byte. Figure 4 and Figure 5 show the data transfer sequence of GL518SM by I^2C bus interface.

Figure 5. Timing Diagram of I²C Write for GL518SM

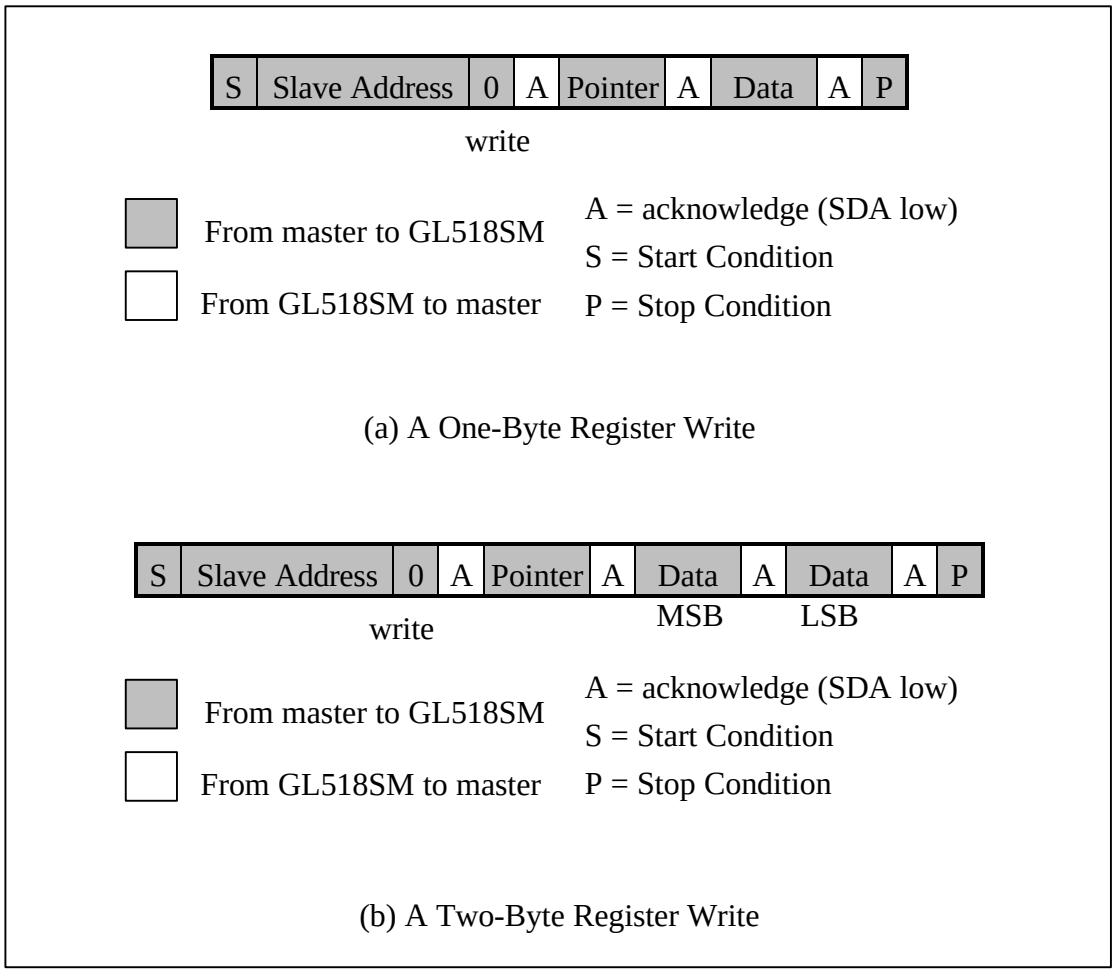
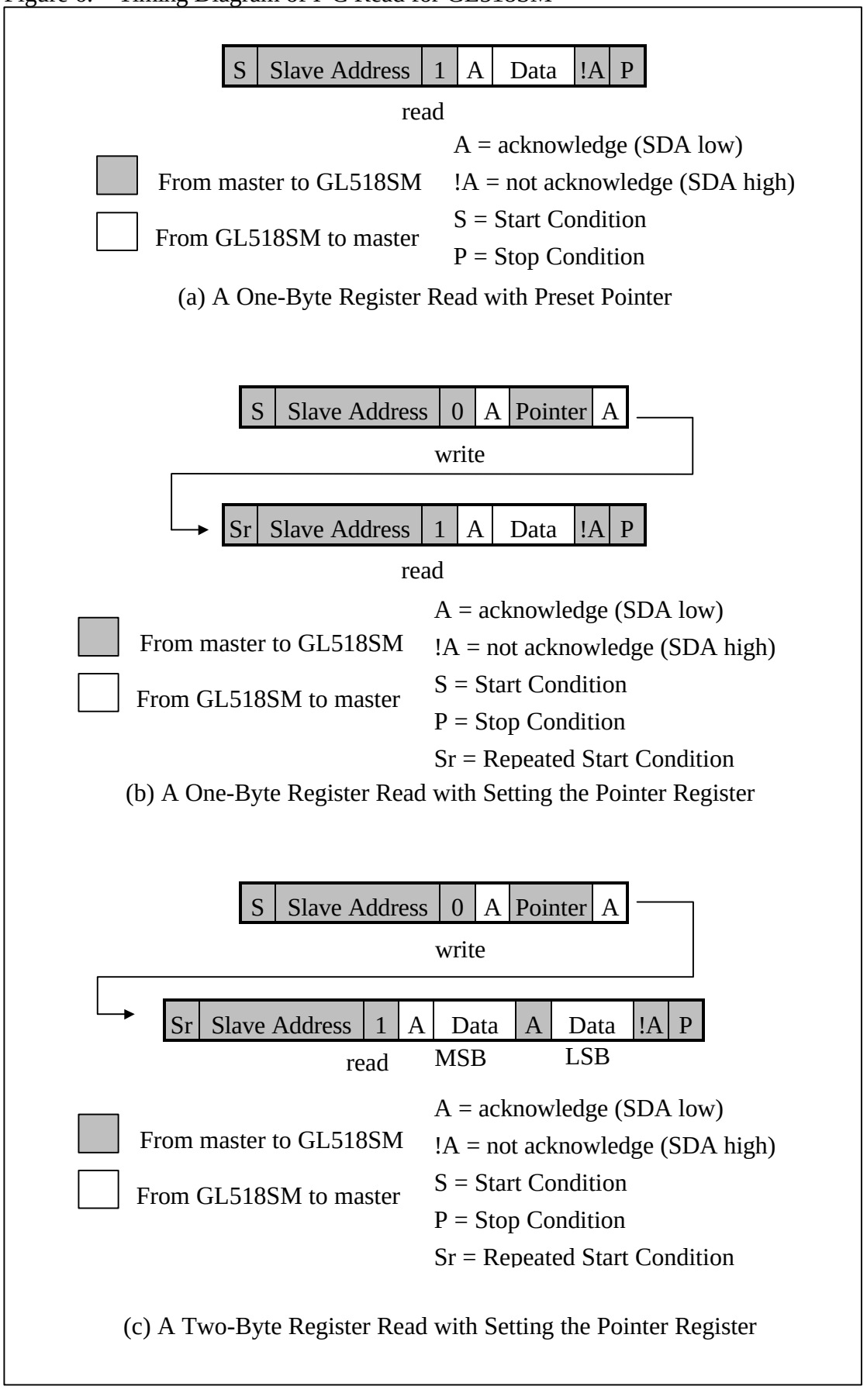


Figure 6. Timing Diagram of I²C Read for GL518SM



9. NAND Tree Tests

A NAND tree is built in the GL518SM for Automated Test Equipment board level connectivity testing. The NAND tree test mode is entered by pulling down the IRQ# pin while power on reset. In this mode, all pins except VDD, GND, AGND and SPKR are high impedant which can be forced to 0 or 5V to accomplish NAND tree tests. The toggled output of the NAND tree is monitored on the SPKR pin.

Registers

1. POINTER REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved			Regsel4	Regsel3	Regsel2	Regsel1	Regsel0

D[7:5]: Must be zero while accessed.

D[4:0]: Regsel[4:0] selects which register to be accessed. The pointers 10010b -- 11110b are undefined.

Regsel[4:0]					Register	Byte	Attribute
0	0	0	0	0	ChipID	1	Read Only
0	0	0	0	1	Revision	1	Read Only
0	0	0	1	0	VenderID	1	R/W
0	0	0	1	1	Configuration	1	R/W
0	0	1	0	0	Temperature	1	Read Only
0	0	1	0	1	Temp_Over	1	R/W
0	0	1	1	0	Temp_Hyst	1	R/W
0	0	1	1	1	Fan1_Count Fan2_Count	2	Read Only
0	1	0	0	0	Fan1_Limit Fan2_Limit	2	R/W
0	1	0	0	1	Vin1_lmth Vin1_lmtl	2	R/W
0	1	0	1	0	Vin2_lmth Vin2_lmtl	2	R/W
0	1	0	1	1	Vin3_lmth Vin3_lmtl	2	R/W
0	1	1	0	0	VDD_lmth VDD_lmtl	2	R/W
0	1	1	0	1	Voltmeter	1	Read Only
0	1	1	1	0	Undefined		
0	1	1	1	1	Misc	1	R/W
1	0	0	0	0	Alarm	1	R/W
1	0	0	0	1	Mask	1	R/W
1	0	0	1	0	Interrupt Status	1	Read Only
1	1	1	1	1	Test	1	R/W

Index 00h: CHIPID REGISTER (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
ChipID7	ChipID6	ChipID5	ChipID4	ChipID3	ChipID2	ChipID1	ChipID0

D[7:0]: The identification code, 80h, of GL518SM, read only.

Index 01h: REVISION REGISTER (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0

D[7:0]: The revision of GL518SM, read only.

Index 02h: VENDER ID REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0

D[7:0]: VID[7:0], vender ID.

Index 03h: CONFIGURATION REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Init	Start	ClearST	NoFan2	Tint	Intclr	Reserved	Reserved

D7: Init, setting a one to this bit restores power on default value to all registers. This bit also clears itself since its default value is zero.
D6: Start, a one enables start of monitoring after 2 seconds, a zero puts GL518SM in standby mode immediately.
D5: ClearST, setting a one to this bit will clear interrupt status register.
D4: NoFan2, a one causes pin FAN2IN/FAN1ON to function as FAN1ON, whereas a zero causes it to function as FAN2IN.
D3: Tint, a zero enables temperature comparator mode, whereas a one enables interrupt mode.
D2: Intclr, a one disables the output of IRQ# and SPKR without affecting the contents of Interrupt Status Register.
D[1:0]: Reserved.

Index 04h: TEMPERATURE REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

D[7:0]: Temp[7:0], an unsigned integer mapping current temperature with 1°C resolution. The reported temperature is sensed by the external thermistor.

Index 05h: Temp_Over REGISTER (default C7h, Temp_Over=80°C)

D7	D6	D5	D4	D3	D2	D1	D0
Tover7	Tover6	Tover5	Tover4	Tover3	Tover2	Tover1	Tover0

D[7:0]: Tover[7:0], over-temperature threshold of the temperature sensed by the external thermistor.

Index 06h: Temp_Hyst REGISTER (default C2h, Temp_Hyst=75°C)

D7	D6	D5	D4	D3	D2	D1	D0
Thyst7	Thyst6	Thyst5	Thyst4	Thyst3	Thyst2	Thyst1	Thyst0

D[7:0]: Thyst[7:0], hysterisis threshold of temperature sensed by the external thermistor.

Index 07h: Fan_Count REGISTER (default 0000h)

D15	D14	D13	D12	D11	D10	D9	D8
Fan1cnt7	Fan1cnt6	Fan1cnt5	Fan1cnt4	Fan1cnt3	Fan1cnt2	Fan1cnt1	Fan1cnt0

D7	D6	D5	D4	D3	D2	D1	D0
Fan2cnt7	Fan2cnt6	Fan2cnt5	Fan2cnt4	Fan2cnt3	Fan2cnt2	Fan2cnt1	Fan2cnt0

D[15:8]: Fan1cnt[7:0], an unsigned integer mapping the fan 1 speed. A higher fan speed causes a lower count.
D[7:0]: Fan2cnt[7:0], an unsigned integer mapping the fan 2 speed. A higher fan speed causes a lower count.

Index 08h: Fan_Limit REGISTER (default 6464h)

D15	D14	D13	D12	D11	D10	D9	D8
Fan1lmt7	Fan1lmt6	Fan1lmt5	Fan1lmt4	Fan1lmt3	Fan1lmt2	Fan1lmt1	Fan1lmt0

D7	D6	D5	D4	D3	D2	D1	D0
Fan2lmt7	Fan2lmt6	Fan2lmt5	Fan2lmt4	Fan2lmt3	Fan2lmt2	Fan2lmt1	Fan2lmt0

D[15:8]: The lower speed limit to indicate a fan 1 failure.
D[7:0]: The lower speed limit to indicate a fan 2 failure.

Index 09h: Vin1_Limit REGISTER (default DAC5h)

D15	D14	D13	D12	D11	D10	D9	D8
Vin1H7	Vin1H6	Vin1H5	Vin1H4	Vin1H3	Vin1H2	Vin1H1	Vin1H0

D7	D6	D5	D4	D3	D2	D1	D0
Vin1L7	Vin1L6	Vin1L5	Vin1L4	Vin1L3	Vin1L2	Vin1L1	Vin1L0

D[15:8]: The high limit of voltage from VIN1.

D[7:0]: The low limit of voltage from VIN1.

Index 0Ah: Vin2_Limit REGISTER (default DAC5h)

D15	D14	D13	D12	D11	D10	D9	D8
Vin2H7	Vin2H6	Vin2H5	Vin2H4	Vin2H3	Vin2H2	Vin2H1	Vin2H0

D7	D6	D5	D4	D3	D2	D1	D0
Vin2L7	Vin2L6	Vin2L5	Vin2L4	Vin2L3	Vin2L2	Vin2L1	Vin2L0

D[15:8]: The high limit of voltage from VIN2.

D[7:0]: The low limit of voltage from VIN2.

Index 0Bh: Vin3_Limit REGISTER (default DAC5h)

D15	D14	D13	D12	D11	D10	D9	D8
Vin3H7	Vin3H6	Vin3H5	Vin3H4	Vin3H3	Vin3H2	Vin3H1	Vin3H0

D7	D6	D5	D4	D3	D2	D1	D0
Vin3L7	Vin3L6	Vin3L5	Vin3L4	Vin3L3	Vin3L2	Vin3L1	Vin3L0

D[15:8]: The high limit of voltage from VIN3.

D[7:0]: The low limit of voltage from VIN3.

Index 0Ch: VDD_Limit REGISTER (default DAC5h)

D15	D14	D13	D12	D11	D10	D9	D8
VDDH7	VDDH6	VDDH5	VDDH4	VDDH3	VDDH2	VDDH1	VDDH0

D7	D6	D5	D4	D3	D2	D1	D0
VDDL7	VDDL6	VDDL5	VDDL4	VDDL3	VDDL2	VDDL1	VDDL0

D[15:8]: The high limit of voltage from VDD.

D[7:0]: The low limit of voltage from VDD.

Index 0Dh: VOLTMETER REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Volt7	Volt6	Volt5	Volt4	Volt3	Volt2	Volt1	Volt0

D[7:0]: Volt[7:0], a positive value of voltage with resolution 19 mV.

Index 0Fh: MISC. REGISTER (default F8h)

D7	D6	D5	D4	D3	D2	D1	D0
Fan1Div1	Fan1Div0	Fan2Div1	Fan2Div0	Fan1auto	Reserved	Reserved	Reserved

D[7:6]: Fan1Div[1:0], fan 1 divisor select.

D[5:4]: Fan2Div[1:0], fan 2 divisor select. The select table of fan1 and fan2 are both the same and shown below:

FanDiv1	FanDiv0	Divisor
0	0	1
0	1	2
1	0	4
1	1	8

D3: Fan1auto, a zero forces pin FAN1ON to high, whereas a one enables the auto on/off control of fan 1.

D[2:0]: Reserved.

Index 10h: ALARM REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Ualarm	Fan2SPK	Fan1SPK	TempSPK	Vin3SPK	Vin2SPK	Vin1SPK	VDDSPK

D7: Ualarm, alarm of a user-defined event. A one forces pin SPKR to output a square wave signal.

D6: Fan2SPK, a one enables SPKR output by Fan2 monitoring.

D5: Fan1SPK, a one enables SPKR output by Fan1 monitoring.

D4: TempSPK, a one enables SPKR output by temperature monitoring.

D3: Vin3SPK, a one enables SPKR output by voltage VIN3 monitoring.

D2: Vin2SPK, a one enables SPKR output by voltage VIN2 monitoring.

D1: Vin1SPK , a one enables SPKR output by voltage VIN1 monitoring.

D0: VDDSPK, a one enables SPKR output by voltage VDD monitoring.

Index 11h: MASK REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Fan2EN	Fan1EN	TempEN	Vin3EN	Vin2EN	Vin1EN	VDDEN

D7: Reserved

D6: Fan2EN, a one enables interrupt output by fan 2 monitoring.

D5: Fan1EN, a one enables interrupt output by fan 1 monitoring.

D4: TempEN, a one enables interrupt output by temperature monitoring.

D3: Vin3EN, a one enables interrupt output by VIN3 monitoring.
D2: Vin2EN, a one enables interrupt output by VIN2 monitoring.
D1: Vin2EN, a one enables interrupt output by VIN1 monitoring.
D0: VDDEN, a one enables interrupt output by VDD monitoring.

Index 12h: INTERRUPT STATUS REGISTER (default 00h)

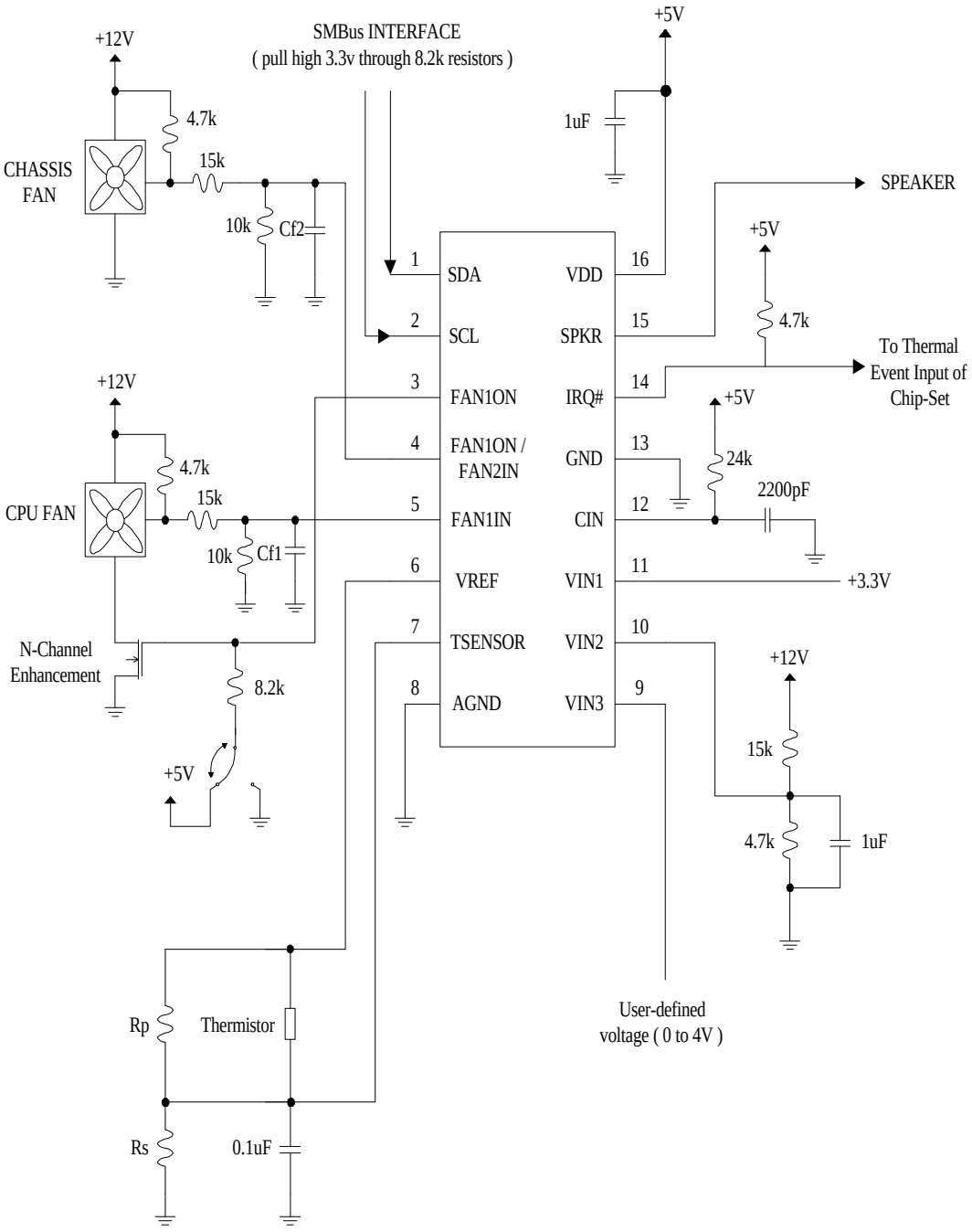
D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Fan2ST	Fan1ST	TempST	Vin3ST	Vin2ST	Vin1ST	VDDST

D7: Reserved.
D6: Fan2ST, a one indicates the speed of fan 2 has exceeded its lower limit.
D5: Fan1ST, a one indicates the speed of fan 1 has exceeded its lower limit.
D4: TempST, a one indicates the temperature above Tover or below Thyst has been detected.
D3: Vin3ST, a one indicates the voltage from VIN3 has exceeded its error limit.
D2: Vin2ST, a one indicates the voltage from VIN2 has exceeded its error limit.
D1: Vin1ST, a one indicates the voltage from VIN1 has exceeded its error limit.
D0: VDDST, a one indicates the voltage from VDD has exceeded its error limit.

Index 1Fh: TEST REGISTER (default 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Test7	Test6	Test5	Test4	Test3	Test2	Test1	Test0

TYPICAL APPLICATION



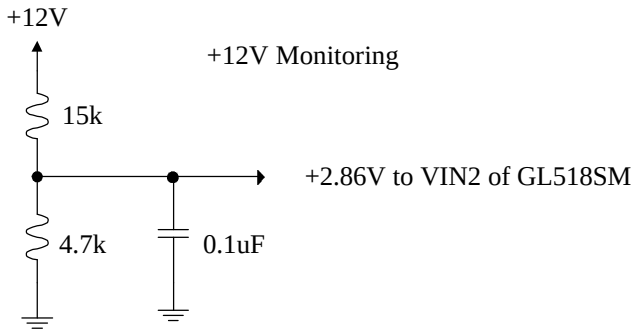
Application Note:

1. The chip is configured to monitor 1 temperature, 2 fans and 4 positive power supplies in the application.

2. The recommended thermistor models and corresponding linearizing resistors are listed below. The values of resistors are computed on neglecting the ingenerate errors of resistors and thermistor. For an optimized temperature precision, the resistors, Rp and Rs, are recommended to offer within ±1% tolerance. Other thermistor models not shown in the table are allowed but the linearizing resistors need changed for optimized measuring precision.

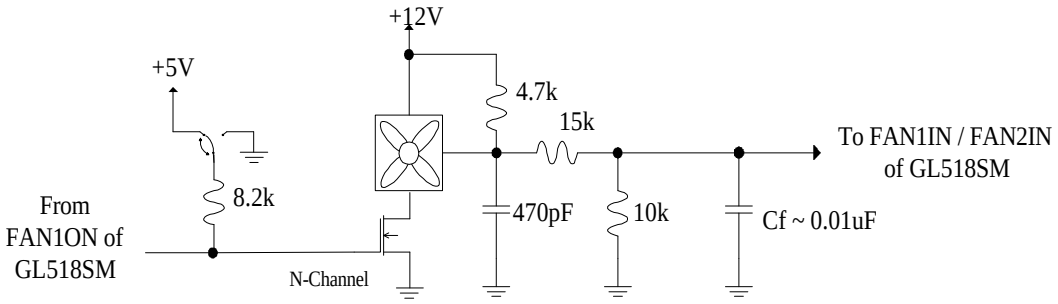
Thermistor Model	Rp	Rs
FENWAL 135-103 LAG-J01	3.9k	3.6k
FENWAL 135-103 LAF-J01	3.9k	3.6k
SEMITEC 103 CT-4	6.8k	5.1k
SEMITEC 103 AT	6.2k	4.7k
YMEX 186-103 YMD-J	3.9k	3.6k
YMEX 186-103 YMC-H	6.2k	4.7k
YMEX 186-103 YMD-JW	5.6k	4.7k
YMEX 286-S103 CIG-H	5.6k	4.7k
YMEX 186-103 YMS-J	5.6k	4.7k

3. Voltage Scaling:
   The power supply to be monitored should be ranged from 0 to 4.0V. In other words, the voltage 0 to 4.0V can be directly connected to voltage input of GL518SM, whereas the voltage above 4.0V, such as 12V, should be attenuated below 4.0V before connected to this chip. The scaling resistor values for +12V input are recommended as below,

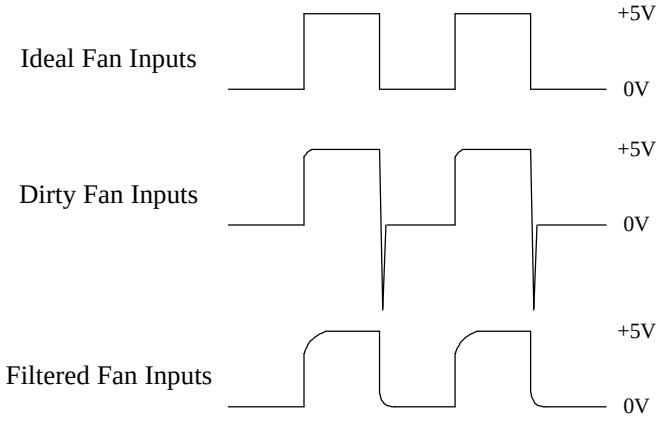


4. Fan Inputs and Fan ON/OFF Control:

   The fan inputs should be connected as illustrated below,



- If the fan inputs are directly pulled high to +5V through resistors in the above diagram, a dc level near +12V will appear at the fan inputs when the fans are turned off. This signal level may lead to damage to the chips.
- The LSB of GL518SM SMBus address is determined by pulling the 8.2k resistor high or low while power on reset. The slave address is 5Ah if this pin is pulled high, and 58h if low.
- The unused fan inputs should be terminated to ground using 10k resistors.
- The capacitor Cf are used to filter the undershoot of fan inputs if needed. The values depend on the undershoot and input threshold at pin FAN1IN/FAN2IN. Be sure the inputs meet the operating ratings, -0.3V ~ VDD+0.3V.



5. Chip Clock:

   The R and C external to pin CIN is adjustable while the internal circuit is oscillated at 32KHz ideally. Since the detected fan inputs are sampled by the chip clock, the error of clock rate will respond the error of computed fan speed.

6. Interrupt Output:

   The IRQ# can be programmed to generate only when the detected CPU temperature exceeds the over temperature limit. In temperature comparator mode, the GL518SM will automatically assert/deassert the IRQ# output depending on the detected temperature. By connecting the IRQ# to the Thermal Detect Input of chip-sets, the GL518SM can be used to start the Hardware Clock Throttle mode. The IRQ# pin of GL518SM is open-drain and should be pulled high externally to operate properly.

7. SMBus Loading:

   The bus loading should be considered since there are usually more than one SMBus-agent component in the system.

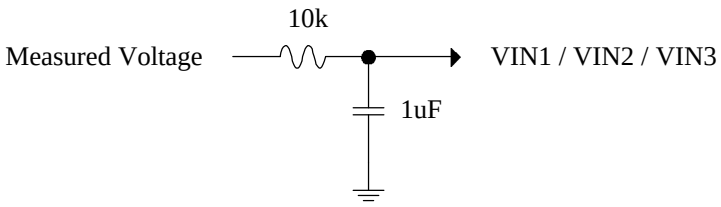
   - The components should be placed closely to each other on the board to minimize the bus loading effect.
   - The values of pull-high resistors are adjusted to meet the rise and fall time condition.
   - The small capacitors are added if the bus loading of these two siganl is severely unbalanced.

8. Bypass Capacitors:

   Bypass capacitors are needed at the pin VDD and should be placed near the chip as closely as possible.

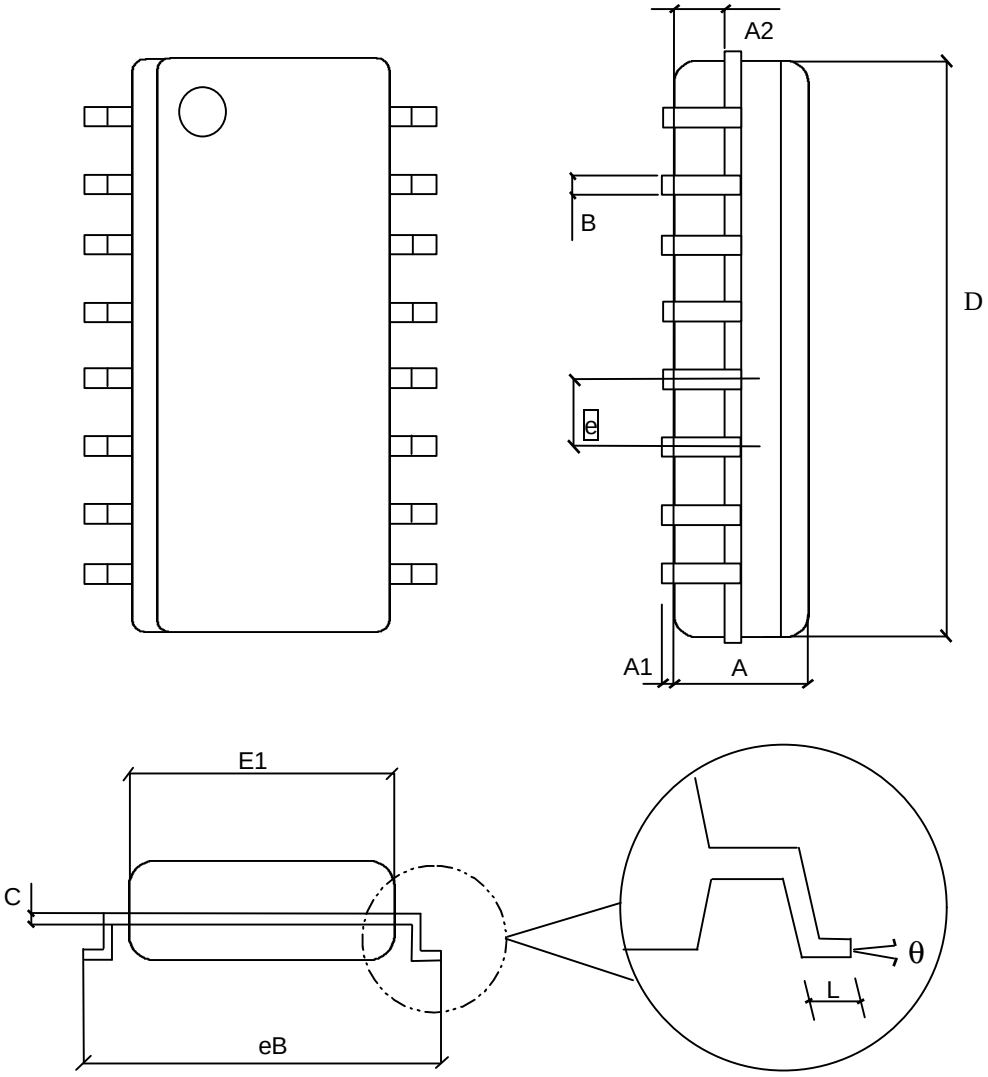
9. Anti-aliasing Filters:

   An anti-aliasing filter is recommended to insert at pin VIN1, VIN2 and VIN3 for a noisy environment. The referenced circuit is as below where the values of R and C are selected so that $R \times C > 5 \times 10^{-4}$.



10. If fan 2 is removed, pin 4 can also be configured to control on/off of fan 1, the same function as pin 3.

The Package Outline Dimension of GL518SM (SOP 16 Pins)



Symbol	Dimension in mils			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	---	58	---	---	1.473	---
A1	6	---	---	0.152	---	---
A2	---	24	---	---	0.610	---
B	---	16	---	---	0.406	---
C	---	8	---	---	0.203	---
D	388	390	392	9.855	9.906	9.957
E1	152	154	156	3.861	3.912	3.962
e	---	50	---	---	1.270	---
eB	---	238	---	---	6.045	---
L	25	---	---	0.635	---	---
θ	0°	3°	6°	0°	3°	6°