TTU056/TTR056 Target Spec

General Description

TTU056/TTR056 is an advanced 4-bit T416 microcontroller. It contains 1K*16 ROM & 64-nibble RAM, which is designed for multiple I/O products application. The device is suitable for application in family appliance, consumer product.

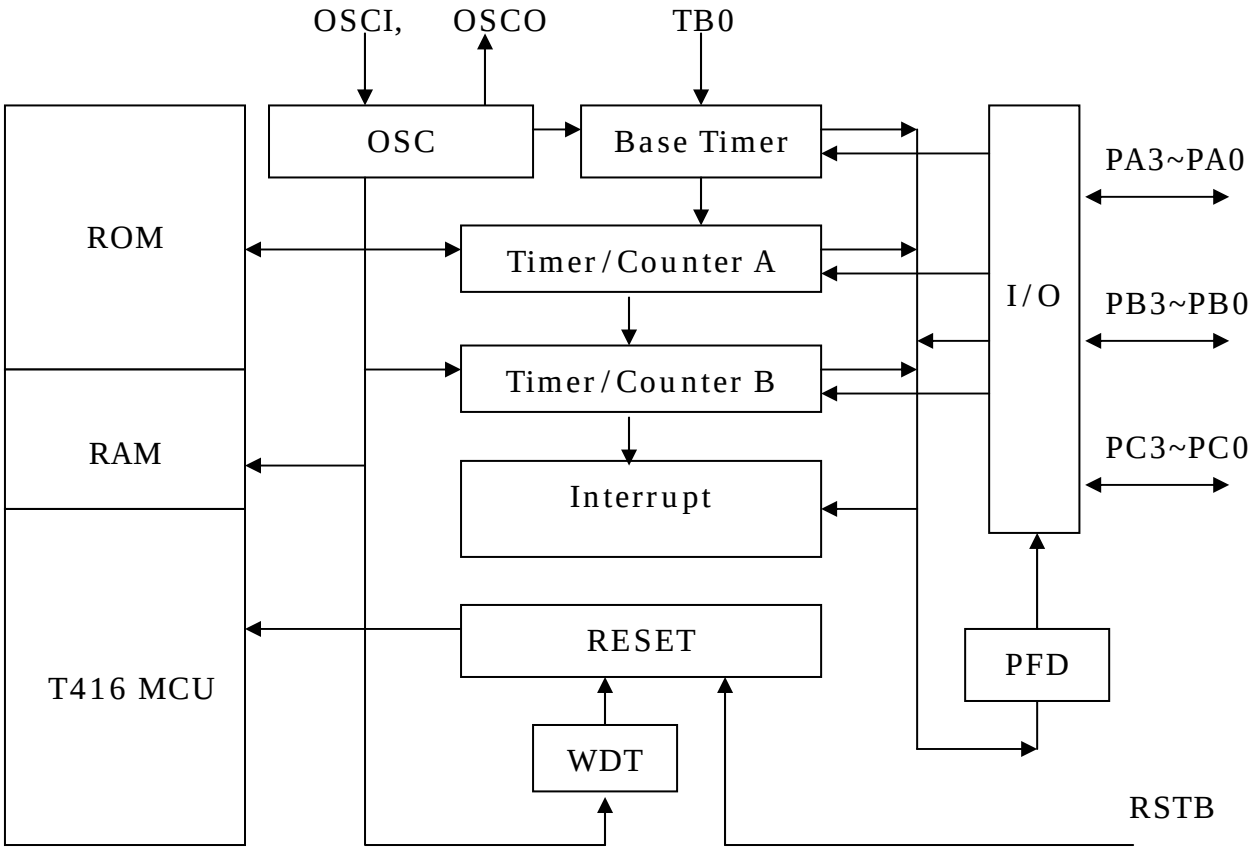
Features

1. 4-bit T416 MCU core
2. 0.5um 1p2m CMOS process
3. 2-level stack
4. Operating voltage: 2.2V~5.5V for TTU056 (2.5V~5.5V for TTR056)
5. Operating frequency:
   - ✧ Resonator mode 1MHz~8MHz
   - ✧ RC mode 400KHz~4MHz
   - ✧ External clock mode
6. 1K*16 program ROM
7. 64*4 SRAM
8. 12 general programmable I/O pins
   - ✧ All I/O ports support keyboard wakeup function by software program except PA0
   - ✧ PA0 can be used as external interrupt
   - ✧ PA1 & PC3 can be used as timer/counter A & B clock input
   - ✧ One-pin (PC0) or two-pin (PC0 & PC1) buzzer output can be selected by mask
   - ✧ Buzzer frequency selection by mask
9. Two 8-bit auto-reload timer/counter & one base timer
   - ✧ External or internal clock source selected by software programming
10. Built-in software control for power saving function
11. Built-in watch dog timer reset circuit
12. Provides 4 interrupt sources
    - ✧ External: PA0/INT0
    - ✧ Internal: Timer/counter A, Timer/counter B & Base timer

Applications

1. Household electric appliances
2. Consumer products
3. Toy controller

Block Diagram



Functional Description

Memory Map

000_H~$3FF_H$ Program ROM [1K*16]

020_H~$05F_H$ Internal RAM [64*4]

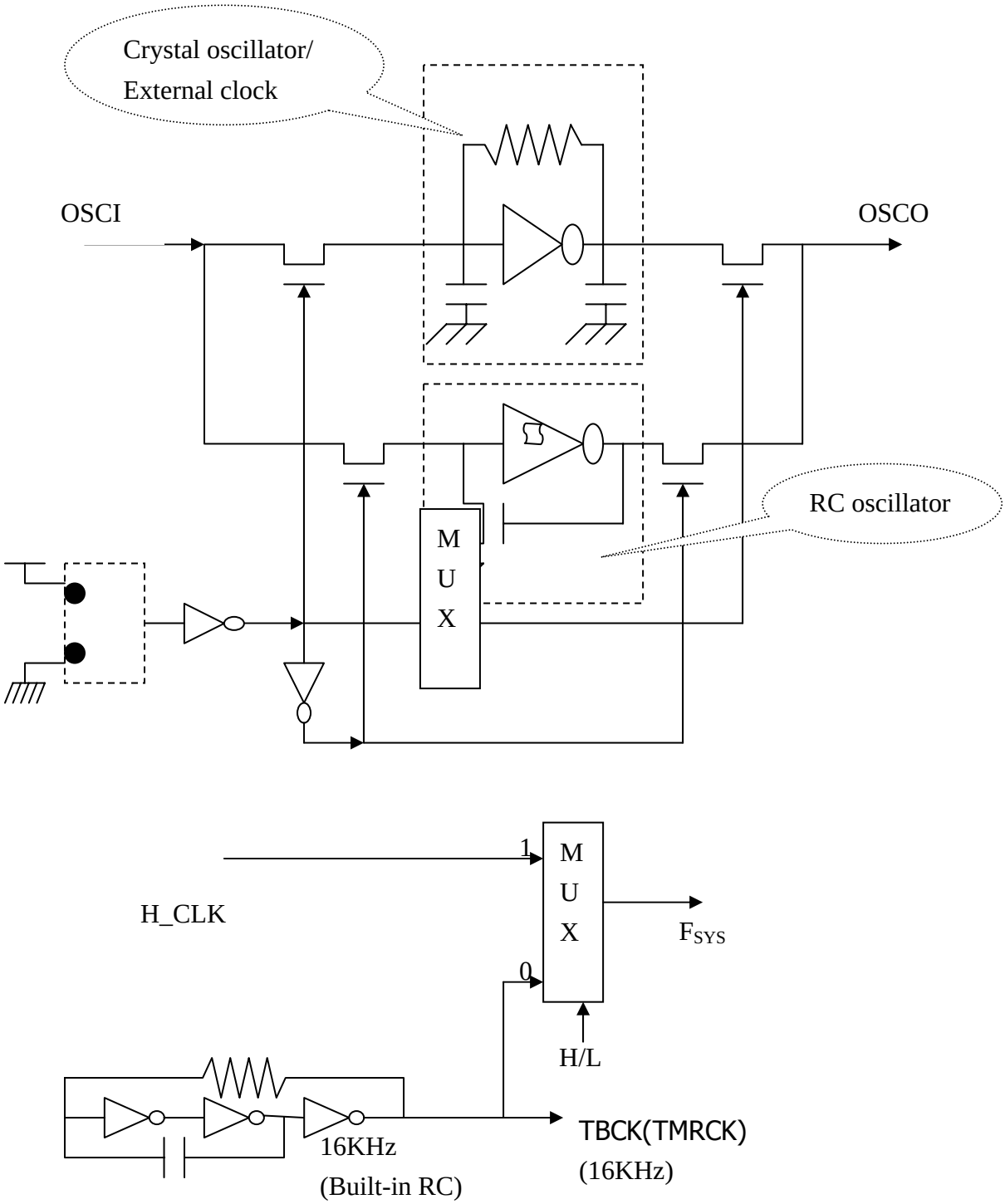
CPU Control Register

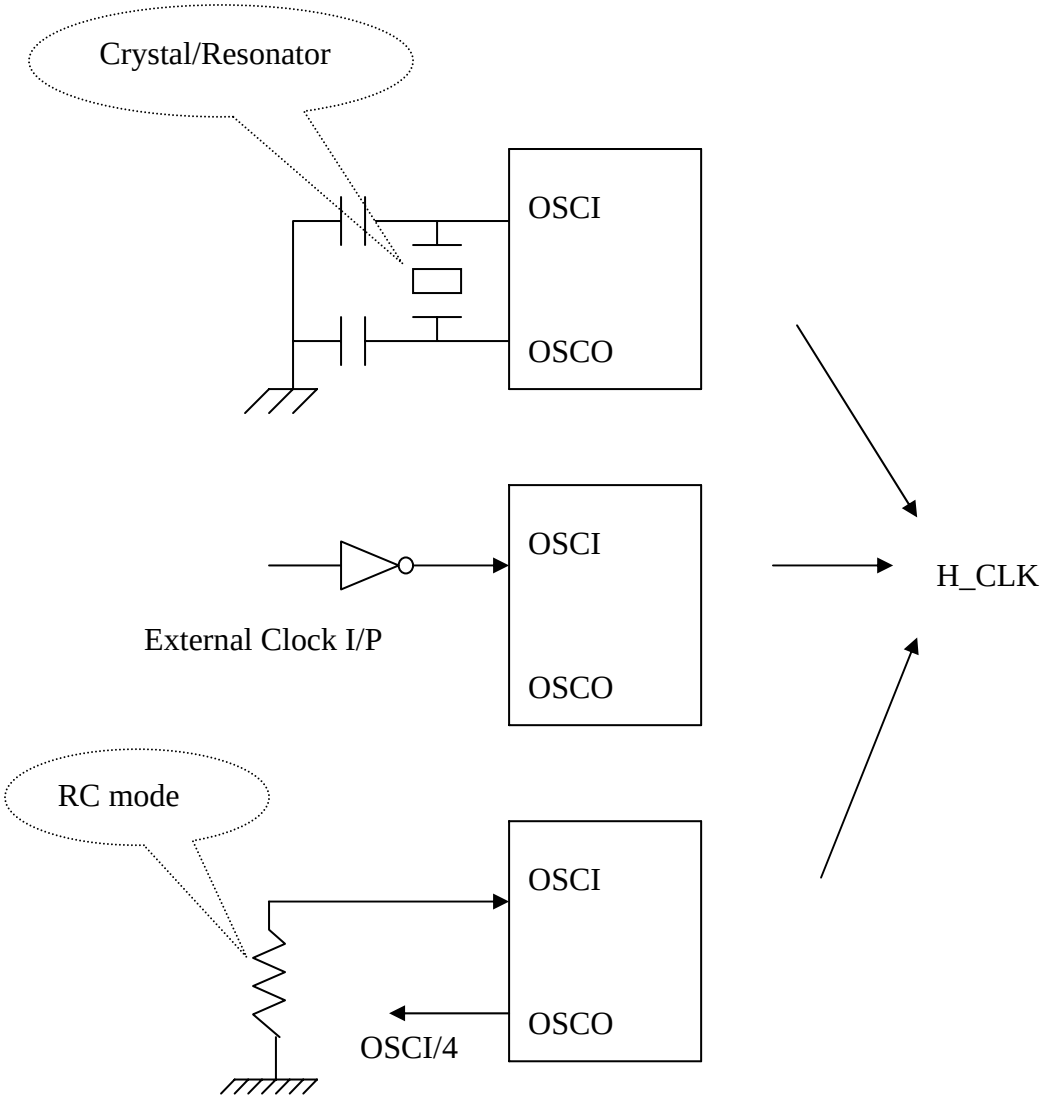
Address	Symbol	R/W	Default	Description
000_H	DP1			
001_H	ACC			
002_H	TB1			
003_H	TB2			
004_H	TB3			
005_H	DPL			
006_H	DPM			
007_H	DPH			
008_H	PS	R/W	X100	CPU power saving register
009_H	INTF	R/W	0000	Interrupt request flag register
$00A_H$	INTC	R/W	0000	Interrupt control register
$00B_H$	PAC	R/W	1111	I/O port A control register
$00C_H$	PA	R/W	1111	I/O port A register
$00D_H$	PBC	R/W	1111	I/O port B control register
$00E_H$	PB	R/W	1111	I/O port B register
$00F_H$	PCC	R/W	1111	I/O port C control register
010_H	PC	R/W	1111	I/O port C register
011_H				Reserved
012_H				
013_H				
014_H				
015_H	TBC	R/W	0000	Time base control register
016_H	TMAL	R/W	0000	Timer/counter A data low register
017_H	TMAH	R/W	0000	Timer/counter A data high register
018_H	TMAC	R/W	0000	Timer/counter A control register
019_H	TMBL	R/W	0000	Timer/counter B data low register
$01A_H$	TMBH	R/W	0000	Timer/counter B data high register
$01B_H$	TMBC	R/W	0000	Timer/counter B control register
$01C_H$				Reserved
$01D_H$				
$01E_H$				
$01F_H$	MFC	R/W	0000	Multi-function control register

1. Oscillators

The TTU056 (TTR056) can be operated in 3 different oscillator modes; resonator mode, RC mode & external clock mode. The oscillator mode can be defined by mask option.

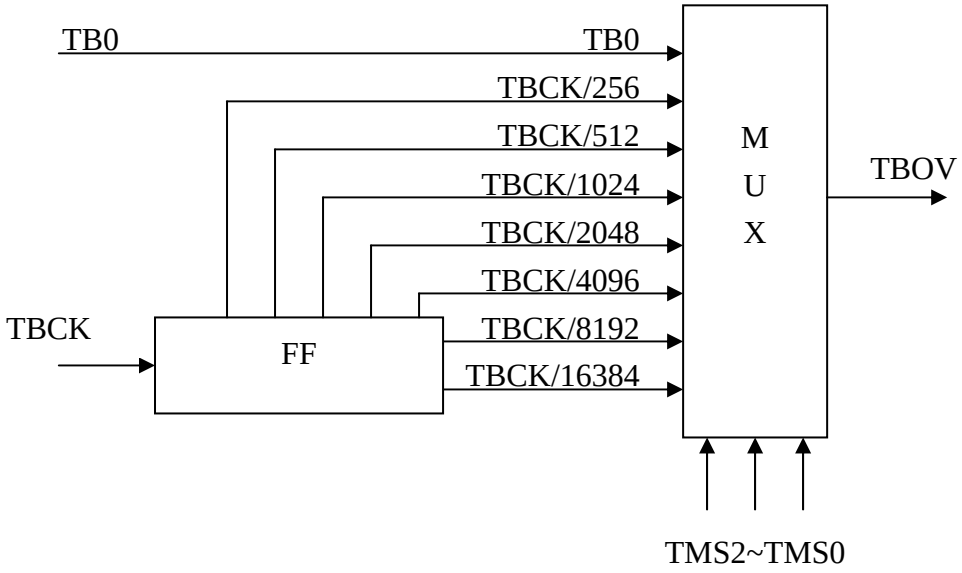
- ✧ Resonator/crystal mode (1MHz~8MHz oscillator)
  A 1MHz~8MHz crystal across OSCI and OSCO, capacitors are connected between OSCI/OSCO and ground.
- ✧ RC mode (400KHz~4MHz oscillator)
  The external R connected OSCI and ground to formalize the oscillator to TTU056 (TTR056). The oscillator frequency divided by 4 is available on OSCO to synchronize other logic or used for testing purpose. The recommend value of R_{ext} between 60KΩ and 500KΩ, for the R_{ext} too low (under 2KΩ) the oscillator will become unstable or stop, too high (over 1MΩ) the oscillator becomes sensitive to noise, humidity.
- ✧ External clock mode (DC~8MHz)
  The TTU056 (TTR056) supports the external clock direct input. For the clock source direct input the crystal oscillator cell, so it needs the same wakeup time as crystal mode from power on or power saving mode.
- ✧ System high speed/low speed mode (Built-in 16KHz RC oscillator)
  The TTU056 (TTR056) was built-in an internal 16KHz RC oscillator for low speed & low power consumption consideration, which was controlled by H/L bit in PS register. In the normal operation, the system clock comes from OSCO (external crystal, resonator or RC and H/L=1 in the meantime).


Crystal oscillator/
External clock
OSCI
OSCO
RC oscillator
M
U
X
1
M
U
X
H_CLK
FSYS
0
H/L
16KHz
(Built-in RC)
TBCK(TMRCK)
(16KHz)


Crystal/Resonator
OSCI
OSCO
OSCI
OSCO
External Clock I/P
H_CLK
RC mode
OSCI
OSCO
OSCI/4

2. Base Timer

The base timer clock source comes from 16KHz internal RC oscillator and time base overflow is selected by TMS2~TMS0 in TBC register.



✧ TBC[015_H], Time base control register[R/W], default value [0000]

Bit3	Bit2	Bit1	Bit0
-	TMS2	TMS1	TMS0

Bit3: reserved, read as 0.

TMS2 ~ TMS0: Base timer overflow frequency selection bits.

TMS2	TMS1	TMS0	Base timer overflow frequency (TBOV)
0	0	0	TB0
0	0	1	TBCK/256
0	1	0	TBCK/512
0	1	1	TBCK/1024
1	0	0	TBCK/2048
1	0	1	TBCK/4096
1	1	0	TBCK/8192
1	1	1	TBCK/16384

3. Timer/Counter

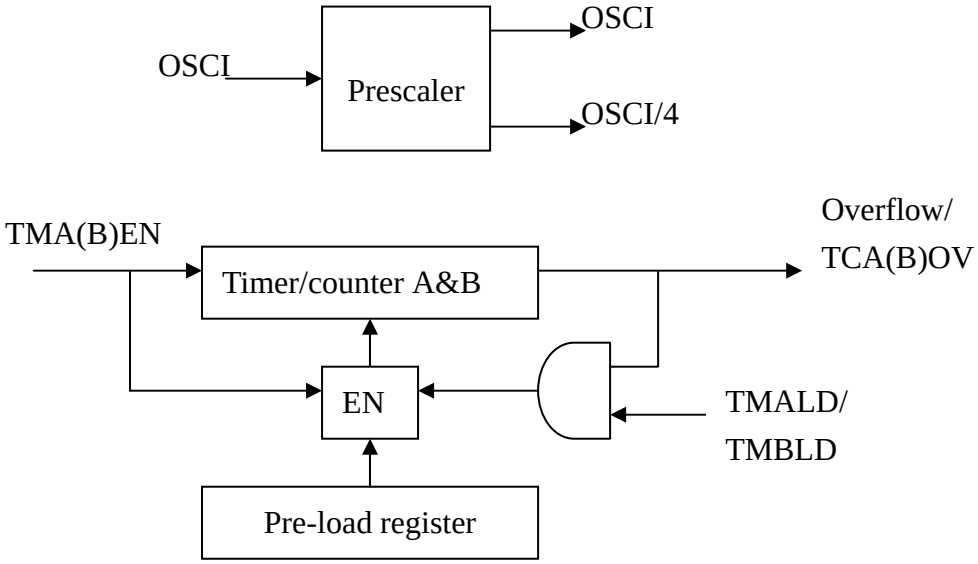
Two 8-bits timer/counters (TMRA & TMRB) with 4 clock sources each are implemented in this chip. The clock sources of TMRA & TMRB are defined by the timer control registers TMAC & TMBC.

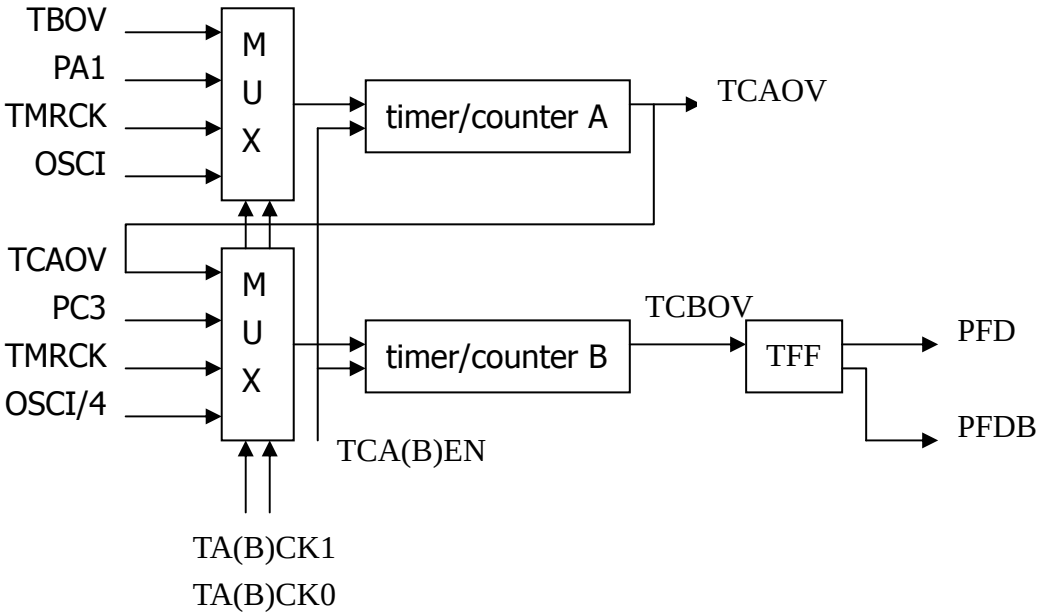
The timer/counter A & B can be cascaded to form a 16-bit timer/counter when the clock source of timer/counter B set to TCAOV. In the 16-bit timer application, "TMAEN" will enable the 16-bit timer/counter and TCBOV will reload the contents in the pre-load register into timer/counter, if TMBLD in TMBC is enabled.

Write TMA/BH(L) register only the data into pre-load register. The data in the pre-load register will be changed when writing TMA/BH(L). The data in pre-load registers will be auto-loaded into timer/counter A(B) and start into counting when writing TMA(B)C register bit0 "TMA(B)EN" to 1 enables the timer, otherwise the timer is on the off-duty situation.

Timer counts the current contents and generates an overflow flag. For example, the programmer writing "FE_H" into timer/counter will count 254 times timer clock and generate an overflow flag at the same time. The content "00_H" will count 256 clocks. When the overflow interrupt generates will reload the content in the pre-load register into timer, if the TMA(B)LD is enabled.

When the timer is counting, writing data will only keep into the pre-load register. The timer will still operate until overflow and then reload the new data into timer depending on TMA(B)LD is enabled or disabled.





✧ TMAC[018_H], Timer/counter A control register[R/W], default value [0000]

Bit3	Bit2	Bit1	Bit0
TMALD	TACK1	TACK0	TMAEN

TMALD: Timer/counter A auto-reload enabled. (0:disable; 1:enable)

TACK1 & TACK0: Timer/counter A clock source selection bits.

TMAEN: Timer/counter A counting enabled. (0:disable; 1:enable)

✧ TMBC[$01B_H$], Timer/counter B control register[R/W], default value [0000]

Bit3	Bit2	Bit1	Bit0
TMBLD	TBCK1	TBCK0	TMBEN

TMBLD: Timer/counter B auto-reload enabled. (0:disable; 1:enable)

TBCK1 & TBCK0: Timer/counter B clock source selection bits.

TMBEN: Timer/counter B counting enabled. (0:disable; 1:enable)

TA(B)CK1	TA(B)CK0	Timer A	Timer B
0	0	OSCI	OSCI/4
0	1	TMRCK	TMRCK
1	0	PA1	PC3
1	1	TBOV	TCAOV

TBOV: Time base overflow.

TCAOV: Timer/counter A overflow.

TMRCK (TBCK): Built-in internal 16KHz RC oscillator.

✧ TMAL[016_H], Timer/counter A data low register[R/W], default value [0000]

Bit3	Bit2	Bit1	Bit0
TMA3	TMA2	TMA1	TMA0

TMA3~TMA0 are the low data of the timer/counter A.

✧ TMAH[017_H], Timer/counter A data high register[R/W], default value [0000],

Bit3	Bit2	Bit1	Bit0
TMA7	TMA6	TMA5	TMA4

TMA7~TMA4 are the high data of the timer/counter A.

✧ TMBL[019_H], Timer/counter B data low register[R/W], default value [0000],

Bit3	Bit2	Bit1	Bit0
TMB3	TMB2	TMB1	TMB0

TMB3~TMB0 are the low data of the timer/counter B.

✧ TMBH[$01A_H$], Timer/counter B data high register[R/W], default value [0000],

Bit3	Bit2	Bit1	Bit0
TMB7	TMB6	TMB5	TMB4

TMB7~TMB4 are the high data of the timer/counter B.

When the register is read, only the content of the timer/counter be read; when the register is written, only writing into the pre-load register.

4. Power saving mode (Stop mode & Sleep mode)

The CPU enters stop mode or sleep mode is operated by writing CPU power saving register PS [008_H]. During the power saving mode, CPU holds the internal status of the system. In stop mode, the oscillator clock will be stopped and system need a warm-up time for the stability of system clock running after wake up.

✧ Power saving mode condition & Release

	Stop mode	Sleep mode
Oscillator	Stopped	Operated
CPU internal status	Retain the status	
Memory, Flag, Register, I/O	Retain the status	
Program counter	Hold the executed address	
Timers	Stopped & Retain	Operated
Watchdog Timer	Retain the status	
Release Condition	RSTB, PA0INT, Keyboard wakeup	RSTB, PA0INT, TMAINT, TMBINT, BTINT, Keyboard Wakeup

✧ PS[008_H], CPU power saving register[R/W] , default value [X100]

Bit3	Bit2	Bit1	Bit0
-	H/L	SLP	STP

Bit3: Reserved, don't care; read as 0 or 1.

H/L: System clock selection. (0: internal 16K RC or external RTC; 1: OSCO)

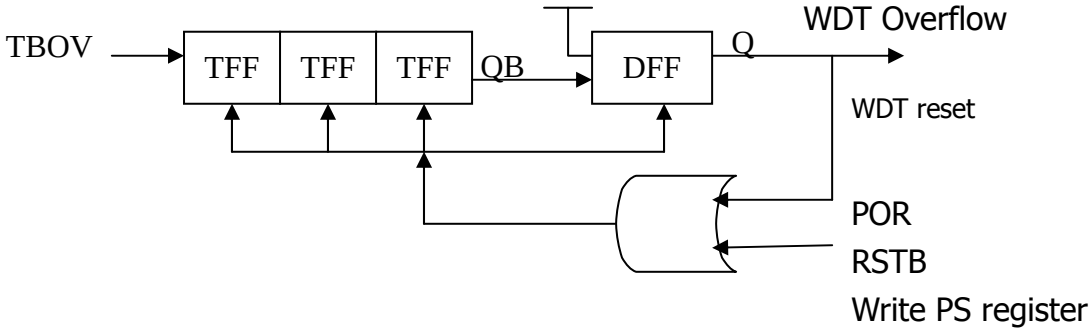
SLP: Into sleep mode. (0: inactive; 1: active)

STP: Into stop mode. (0: inactive; 1: active)

The SLP & STP bits will be cleared to "0" automatically, when the release conditions occur.

5. Watchdog timer

The watchdog timer frequency comes from time base overflow (TBOV). The watchdog timer is always enabled in this chip. After 7 TBOV clock raising edges, the chip will generate the watchdog overflow signal. User can use the time up signal to prevent a software malfunction or sequence from jumping to an unknown location when system is fail. Normally, the watchdog time up signal initializes the chip reset under normal operation. The chip also provides clear watchdog command that is the programmer writes any data to PS register [008_H] can clear the watchdog timer counter only.



6. IO Port

There are total 12 general I/O ports (PA3~PA0, PB3~PB0 & PC3~PC0) in this chip. All I/O ports can be used for input & output operations under software control. All the ports can be defined as keyboard wake-up interrupt individually by programming data registers & control registers, except PA0. The corresponding port set to input mode and enable the pull-high resistor will actuate the keyboard wakeup function simultaneously. The PA0 can be used as external interrupt (INT0); the PA1 & PC3 can be as the timer/counter A & B clock source. The buzzer outputs are pins shared with PC1 (BZB) & PC0 (BZ). If the PC1 & PC0 set to be output mode and the BZEN bit in MFC register set to "1", the buzzer function be enabled and the frequencies output selected by mask.

✧ PAC [$00B_H$], I/O port A control register[R/W], default value 1111

Bit3	Bit2	Bit1	Bit0
PAC3	PAC2	PAC1	PAC0

PAC3~PAC0: PA3~PA0 I/O control bit. (0: output, 1: input)

✧ PA [$00C_H$], I/O port A register[R/W], default value 1111

Bit3	Bit2	Bit1	Bit0
PA3	PA2	PA1	PA0

PA3~PA0 are the data value of the I/O port A.

✧ PBC [$00D_H$], I/O port B control register[R/W], default value 1111

Bit3	Bit2	Bit1	Bit0
PBC3	PBC2	PBC1	PBC0

PBC3~PBC0: PB3~PB0 I/O control bit. (0: output, 1: input)

✧ PB [$00E_H$], I/O port B register[R/W], default value 1111

Bit3	Bit2	Bit1	Bit0
PB3	PB2	PB1	PB0

PB3~PB0 are the data value of the I/O port B.

✧ PCC [$00F_H$], I/O port C control register[R/W], default value 1111

Bit3	Bit2	Bit1	Bit0
PCC3	PCC2	PCC1	PCC0

PCC3~PCC0: PC3~PC0 I/O control bit. (0: output, 1: input)

✧ PC [010_H], I/O port C register[R/W], default value 1111

Bit3	Bit2	Bit1	Bit0
PC3	PC2	PC1	PC0

PC3~PC0 are the data value of the I/O port C.

When writing PA/PB/PC, data are written into the PA/PB/PC registers.

When reading PA/PB/PC & PA/PB/PC in input mode, the states in PA/PB/PC pads are read.

When reading PA/PB/PC & PA/PB/PC in output mode, the data in PA/PB/PC registers are read.

When the PA/PB/PC ports are set to input mode (PACx/PBCx/PCCx=1), the PA/PB/PC register (PAx/PBx/PCx) be as the control bits to control the pull-high resistors enabled/disabled.

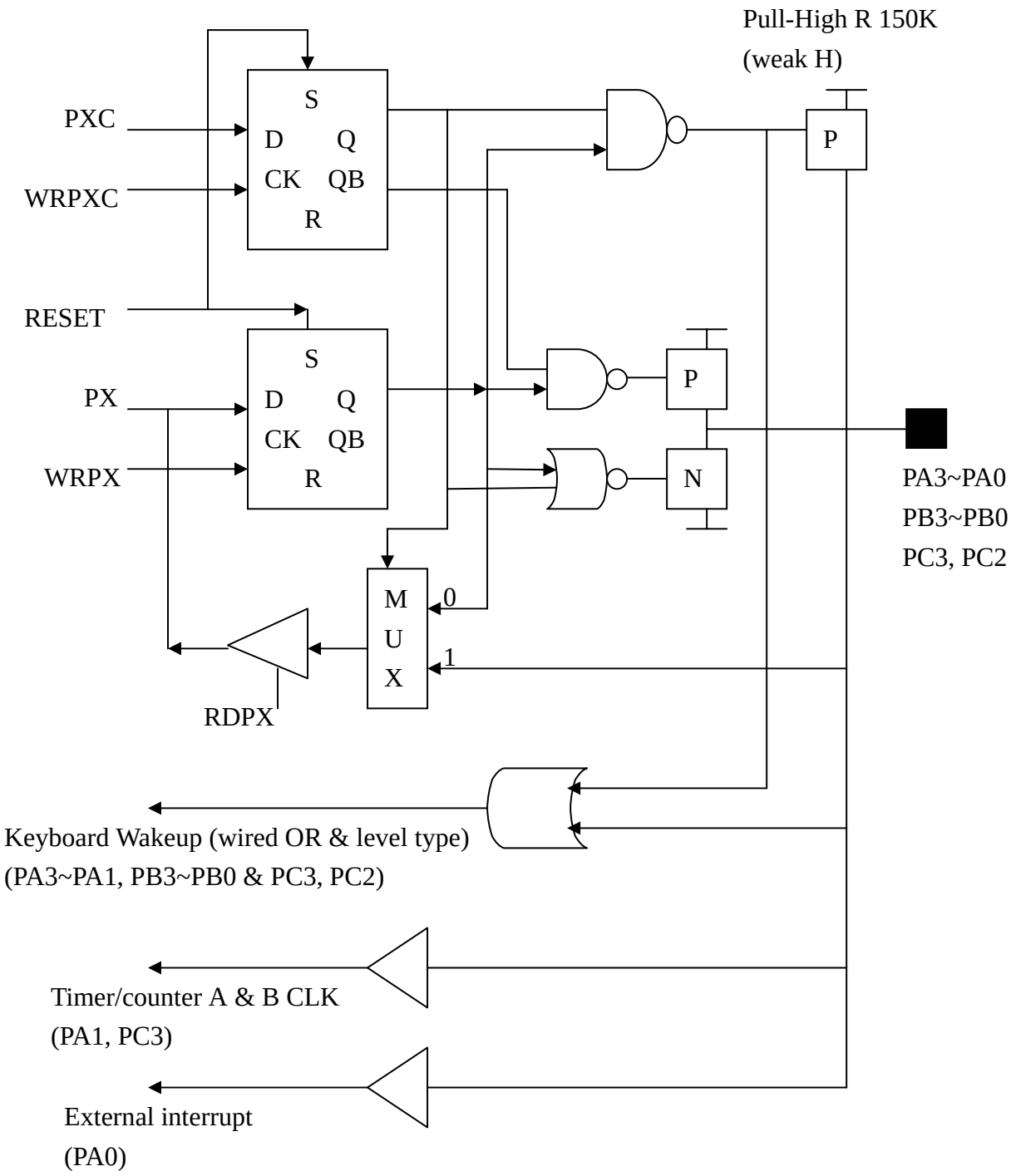
✧ MFC [$01F_H$], Multi-function control register [R/W], default 0000

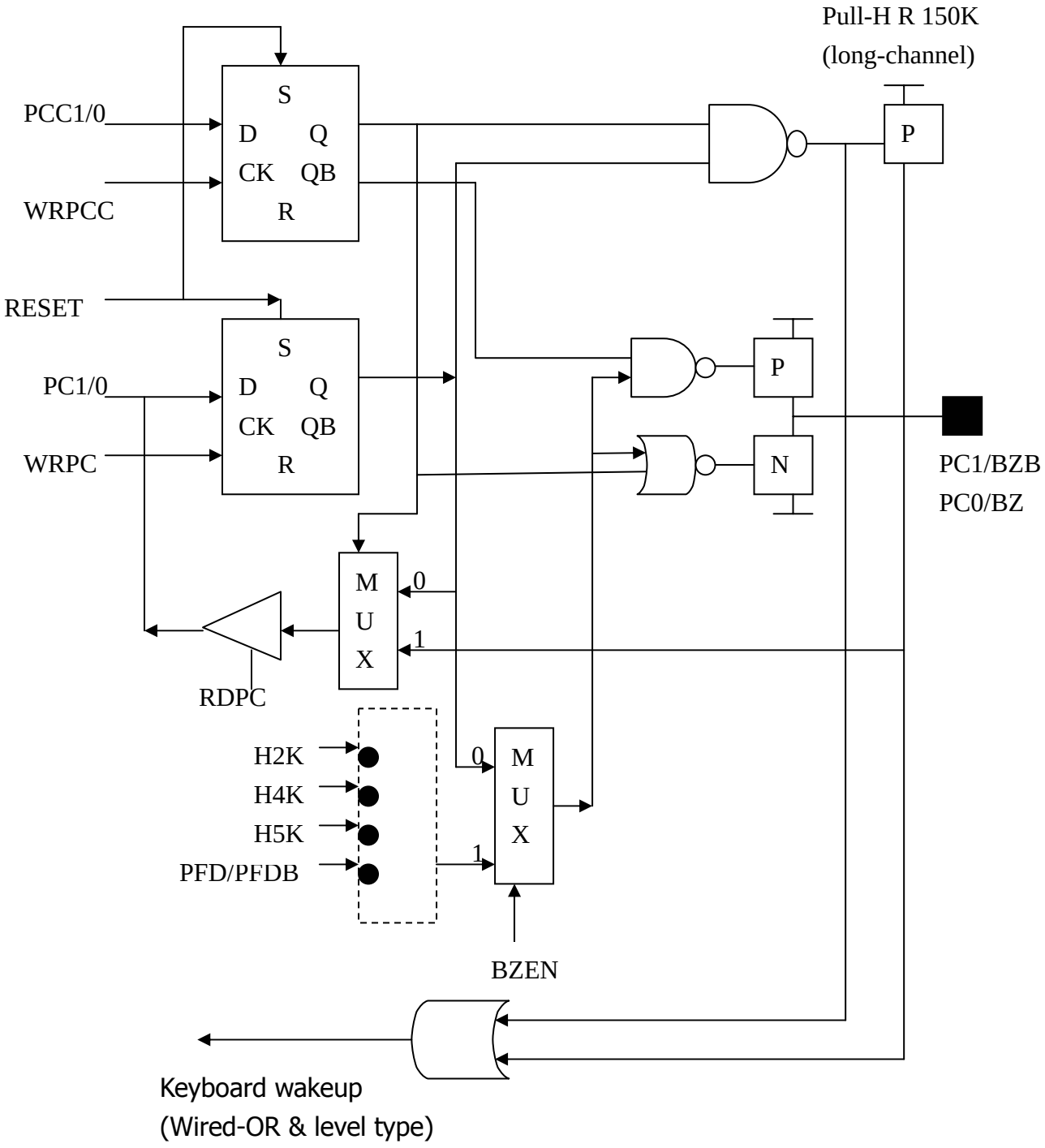
Bit3	Bit2	Bit1	Bit0
-	-	-	BZEN

Bit3~Bit1: reserved, read as 0.

BZEN: Enable buzzer function. (0: disable; 1: enable)

If the PC1 selected as I/O type by mask option, the buzzer enable will actuate one-pin buzzer function, otherwise two-pin buzzer function will be activated.


Pull-High R 150K
(weak H)
PXC
WRPXC
RESET
PX
WRPX
S
D Q
CK QB
R
P
N
M
U
X
0
1
RDPX
PA3~PA0
PB3~PB0
PC3, PC2
Keyboard Wakeup (wired OR & level type)
(PA3~PA1, PB3~PB0 & PC3, PC2)
Timer/counter A & B CLK
(PA1, PC3)
External interrupt
(PA0)


Pull-H R 150K
(long-channel)
PCC1/0
WRPCC
S
D Q
CK QB
R
P
RESET
PC1/0
WRPC
S
D Q
CK QB
R
P
N
PC1/BZB
PC0/BZ
M
U
X
0
1
RDPC
H2K
H4K
H5K
PFD/PFDB
0
1
M
U
X
BZEN
Keyboard wakeup
(Wired-OR & level type)

7. Interrupts

The chip provides total 4 interrupt sources. They are PA0 INT (PA0INT), timer/counter A INT (TMAINT), timer/counter B INT (TMBINT) & base timer INT (BTINT). The interrupt control register INTC contains the interrupt control bits to enable and disable corresponding interrupt and the corresponding interrupt request flags in the INTF register.

If the interrupt needs service, the programmer may set the corresponding bit to allow interrupt nesting. PA0 interrupts are triggered by a high to low transition and set the related interrupt request flags (FPA0). The internal timer/counter A & B interrupt is initialized by setting FTMA or FTMB to 1 individually, resulting from the timer overflow. The base timer INT (BTINT) was provided from TBCK/256 to TBCK/16384 or external TB0 input which was optioned by TBC register.

When the corresponding interrupt enable bits are set to 1, the chip will active the interrupt service. If certain interrupt needs service, the corresponding service flag may set 1 to alert the interrupt service. Then CPU reads the service flag and proceeds with the interrupt service. After CPU writes the corresponding bits to 0 in the INTF register, the service flag will be cleared to 0 to allow other interrupt requests happen; the CPU writes "1" in the register will not change the corresponding data in the register.

✧ INTF [009_H], interrupt request flag register [R/W], default 0000

Bit3	Bit2	Bit1	Bit0
FPA0	FTMA	FTMB	FBT

FPA0: PA0 interrupt request flag. (0: inactive; 1: active)

FTMA: Timer/counter A interrupt request flag. (0: inactive; 1: active)

FTMB: Timer/counter B interrupt request flag. (0: inactive; 1: active)

FBT: Base timer interrupt request flag. (0: inactive; 1: active)

✧ INTC [$00A_H$], interrupt control register [R/W], default 0000

Bit3	Bit2	Bit1	Bit0
PA0IE	TMAIE	TMBIE	BTIE

PA0IE: Enable PA0 interrupt. (0: disable; 1: enable)

TMAIE: Enable timer/counter A interrupt. (0: disable; 1: enable)

TMBIE: Enable timer/counter B interrupt. (0: disable; 1: enable)

BTIE: Enable base timer interrupt. (0: disable; 1: enable)

8. RESET

The chip has three kinds of reset source as follow

- POR (power on reset)
- External reset
- Watchdog timer reset

POR (power on reset)

The chip provides automatic reset function when the power is turned on.

External Reset (RSTB)

This is one kind of system resetting signal, but only operated device externally. When the chip acknowledged the low level from the pin RSTB exceed 4 system clocks, it will generate the reset signal to reset CPU & all the peripheral back to their initial state (default values).

Watchdog timer reset

The watchdog timer is always enabled in this chip. The reset signal will generate automatically when the watchdog timer is overflow. Normally, the watchdog time up signal initializes the chip reset under normal operation.

Mask Option Table:

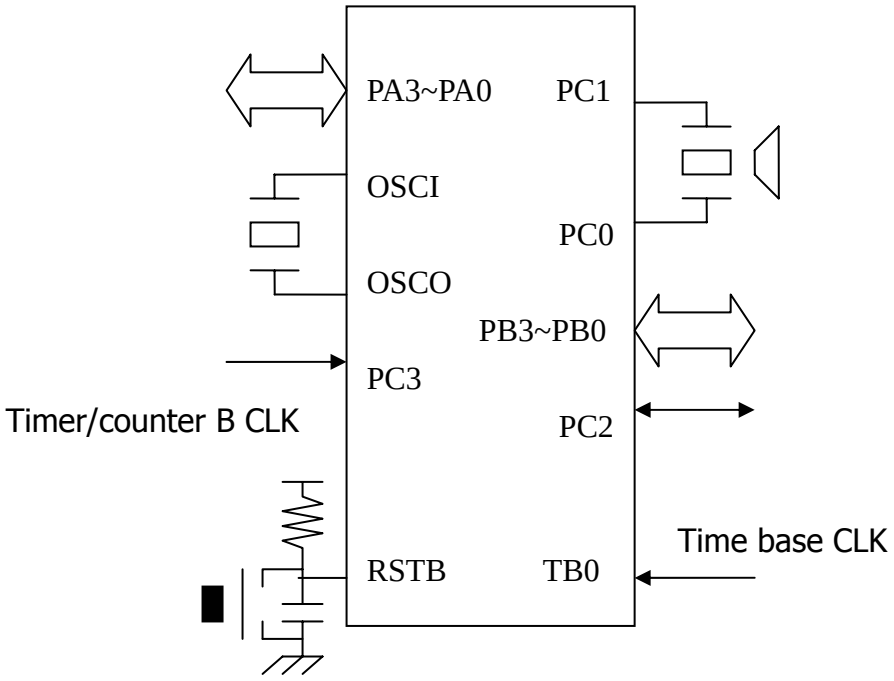
The following table shows the mask option in this chip. All the mask options must define to ensure proper function.

Function	Option			
Oscillator selection	Crystal/resonator mode External clock mode		RC mode	
PC1 function selection	I/O		Buzzer	
Buzzer freq selection	2KHz	4KHz	5.3KHz	PFD/PFDB

Pin Description

Pin Name	I/O	Description
V_{DD}		Positive power supply
V_{SS}		Negative power supply, ground
OSCI	I	Crystal type: crystal input RC type: RC oscillator input External clock input
OSCO	O	Crystal type: crystal output RC type: Oscillator frequency divided by 4 is available on OSCO to synchronize other logic or used for testing purpose.
PA3 PA2 PA1 PA0/INT0	I/O	Bidirectional 4-bits I/O port, PA0 can be used as external interrupt. PA1 can be used as timer/counter A clock input PA3~PA0 used as general I/O pins. PA3~PA1 can be defined as keyboard wakeup by software program.
PB3~PB0	I/O	Bidirectional 4-bits I/O port, PB3~PB0 used as general I/O pins. All PB pins can be defined as keyboard wakeup by software program.
PC3 PC2 PC1/BZB PC0/BZ	I/O	Bidirectional 4-bits I/O port, PC1 & PC0 can be used as buzzer output or general I/O port. PC3 used as general I/O pins or timer/counter B clock input. All PC pins can be defined as keyboard wakeup by software program.
TB0	I	TB0 can be used as base timer external clock source. Internal pull-H R
RSTB	I	External reset input, active low

Application Circuit



DC Characteristics

(Ta=25°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	V_{DD1}	F_{OSC}=4MHz (LVR OFF/TTU056)	2.2	3.0	5.5	V
	V_{DD2}	F_{OSC}=4MHz (LVR OFF/TTR056)	2.5	3.0	5.5	
Operating Current	I_{dd1}	V_{DD}=5.0V, F_{OSC}=8MHz, I/O no load	-	3.0	4.0	mA
	I_{dd2}	V_{DD}=5.0V, F_{OSC}=4MHz, I/O no load	-	1.5	2.0	
	I_{dd3}	V_{DD}=3.0V, F_{OSC}=32768Hz, I/O no load	-	20	30	uA
Standby Current	I_{STB}	I/O no load, F_{OSC} stop	-	-	1.0	uA
PA, PB, PC, TB0 Input Low Voltage	V_{IL}		0	-	0.2	V_{DD}
PA, PB, PC, TB0 Input High Voltage	V_{IH}		0.8	-	1.0	V_{DD}
PA, PB, PC Sink Current	I_{OL}	V_{DD}=5.0V, V_{OL}=0.6V	-	20	-	mA
PA, PB, PC Source Current	I_{OH}	V_{DD}=5.0V, V_{OH}=Vdd-0.7V	-	-10	-	mA
PA, PB, PC Pull-High R	R_{PH1}	V_{DD}=5.0V	100	150	200	KΩ
TB0 Pull-High R	R_{PH2}	V_{DD}=5.0V	25	50	75	KΩ

AC Characteristics

Parameter	Test Condition		Min	Typ	Max	Unit
Oscillator Frequency	F_{OSC1}(Crystal)	V_{DD}=5.0V	1M	-	8M	Hz
	F_{OSC2}(RC)		400K	-	4M	
	F_{OSC3}	V_{DD}=3.0V	-	-	1M	
System Startup Period	T_{OSC1}	Power-up	-	2048	-	TBCK
	T_{OSC2} (Crystal)	Wake-up from STOP mode	-	1024	-	
	T_{OSC3} (RC)		-	128	-	
	T_{OSC4} (Internal 16KHz RC)		-	128	-	
	T_{OSC5}	Wake-up from SLEEP mode	-	128	-	

Order Information

a. Package form : TTU(R)056-zzz
b. Chip form : TCU(R)056-zzz
c. Wafer base : TDU(R)056-zzz

Revise History

yyyy /mm/dd
-