PFC / Flyback PWM Controller **SG6901A**

FEATURES OVERVIEW

- Interleaved PFC/PWM switching
- Low start-up and operating current
- Innovative switching charge multiplier-divider
- Multi-vector control for improved PFC output transient response
- Average-current-mode control for PFC
- Programmable two-level PFC output voltage
- PFC over-voltage and under-voltage protections
- PFC and PWM feedback open-loop protection
- Cycle-by-cycle current limiting for PFC/PWM
- Slope compensation for PWM
- Constant power limit for PWM
- Brownout protection
- Over-temperature protection (OTP)

APPLICATIONS

- Switching Power Supplies with Active PFC and Standby Power
- High-Power Adaptors

DESCRIPTION

The highly integrated SG6901A is designed for power supplies with boost PFC and flyback PWM. It requires very few external components to achieve versatile protections. It is available in a 20-pin SOP package.

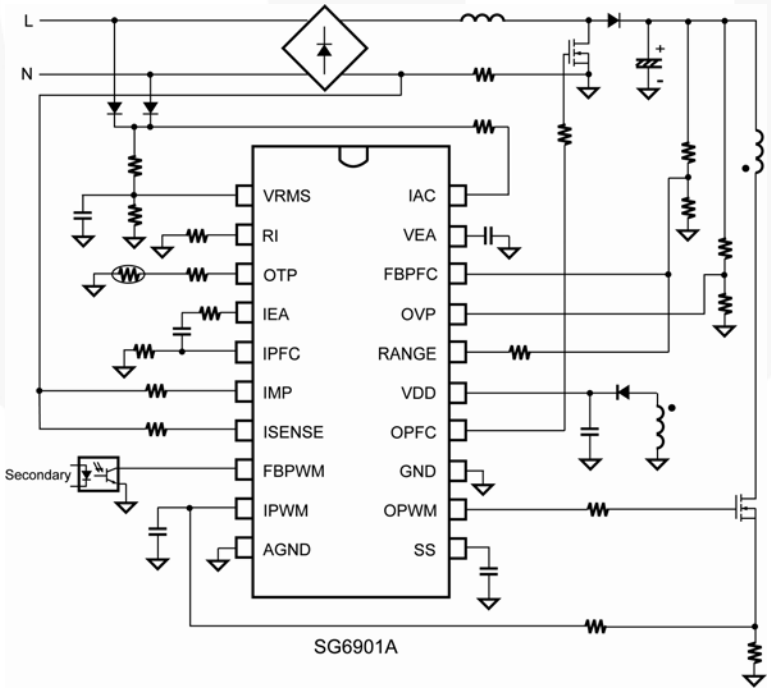
The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6901A shuts off PFC to prevent extra-high voltage on output. Programmable two-level output voltage control reduces the PFC output voltage at low line input to increase the efficiency of the power supply.

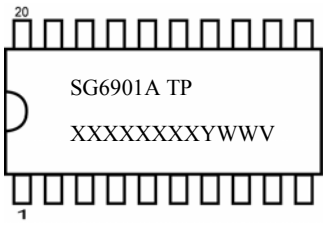
For the flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Built-in line-voltage compensation maintains constant output-power limit. Hiccup operation during output overloading is also guaranteed.

In addition, SG6901A provides protection functions, such as brownout and RI pin open/short protection.

Typical Application

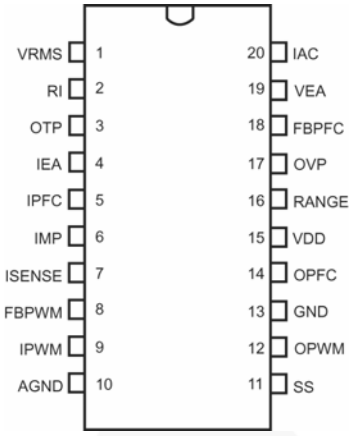


MARKING DIAGRAMS



T: S=SOP
P : Z=Lead Free
Null=regular package
XXXXXXXX: Wafer Lot
Y: Year; WW: Week
V: Assembly Location

PIN CONFIGURATION



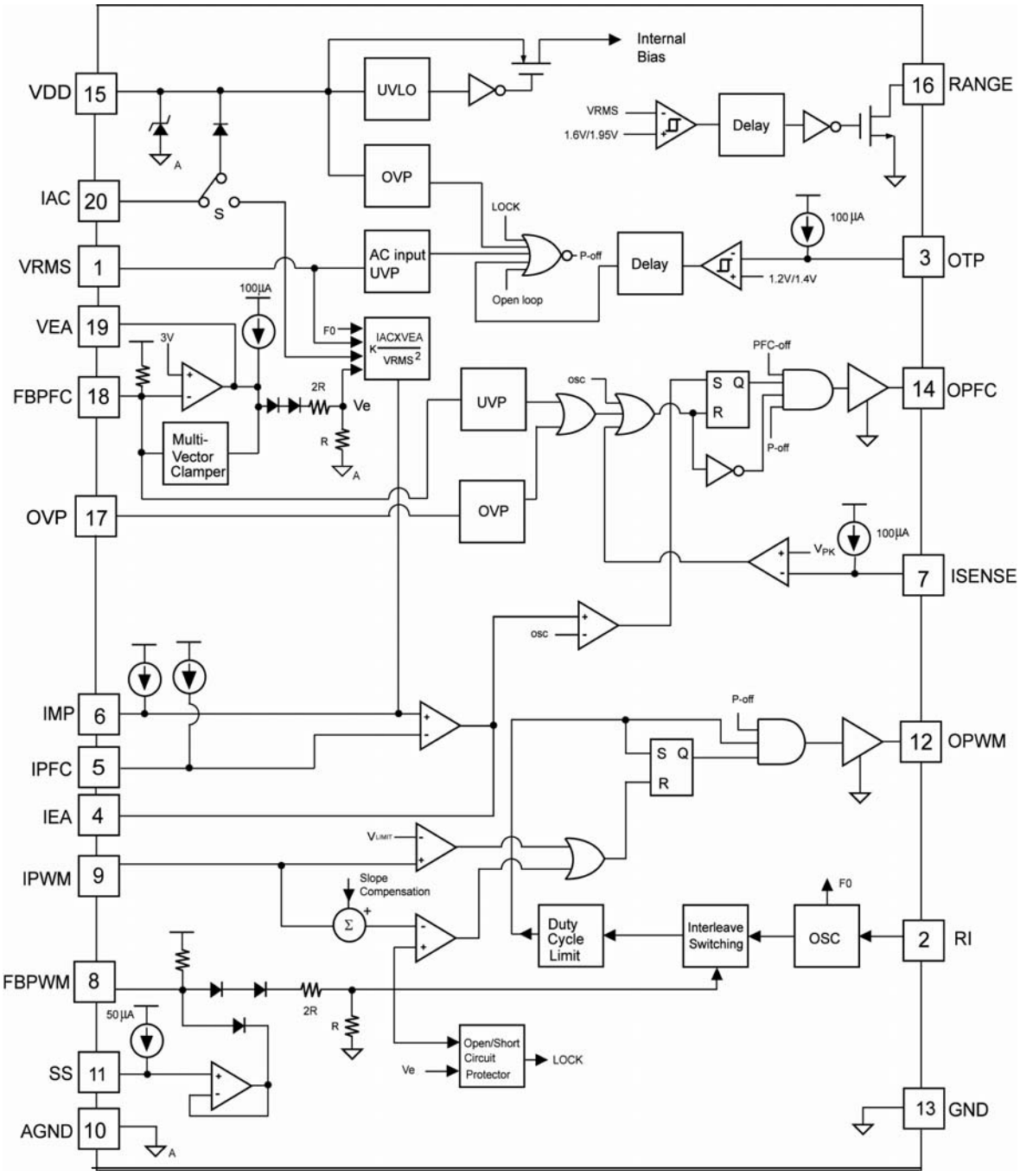
ORDERING INFORMATION

Part Number	Pb-Free	Package
SG6901ASZ		20-pin SOP

PIN DESCRIPTIONS

Name	Pin No.	Type	Function
VRMS	1	Line-Voltage Detection	Line voltage detection. The pin is used for PFC multiplier, RANGE control of PFC output voltage, and brownout protection. For brownout protection, the controller is disabled after a delay time when the VRMS voltage drops below a threshold.
RI	2	Oscillator Setting	Reference setting. One resistor connected between RI and ground determines the switching frequency. The switching frequency is equal to [1560 / RI] KHz, where RI is in KΩ. For example, if R_I is equal to 24KΩ, the switching frequency is 65KHz.
OTP	3	Over Temperature Protection	This pin supplies an over-temperature protection signal. A constant current is output from this pin. An external NTC thermistor must be connected from this pin to ground. The impedance of the NTC thermistor decreases whenever the temperature increases. Once the voltage of the OTP pin drops below the OTP threshold, the SG6901A is disabled.
IEA	4	Output for PFC Current Amplifier	This is the output of the PFC current amplifier. The signal from this pin is compared with an internal sawtooth and determines the pulse width for PFC gate drive.
IPFC	5	Inverting Input for PFC Current Amplifier	The inverting input of the PFC current amplifier. Proper external compensation circuits result in excellent input power factor via average-current-mode control.
IMP	6	Non-inverting Input for PFC Current Amplifier	The non-inverting input of the PFC current amplifier and the output of multiplier. Proper external compensation circuits will result in excellent input power factor via average-current-mode control.
ISENSE	7	Peak Current Limit Setting for PFC	The peak-current setting for PFC.
FBPWM	8	PWM Feedback Input	The control input for voltage-loop feedback of PWM stage. It is internally pulled high through a 6.5kΩ resistance. Usually an external opto-coupler from secondary feedback circuit is connected to this pin.
IPWM	9	PWM Current Sense	The current-sense input for the flyback PWM. Via a current sense resistor, this pin provides the control input for peak-current-mode control and cycle-by-cycle current limiting.
AGND	10	Ground	Signal ground.
SS	11	PWM Soft-Start	During startup, the SS pin will charge an external capacitor with a 50μA (RI=24KΩ) constant current source. The voltage on FBPWM will be clamped by SS during startup. In the event of a protection condition occurring and/or PWM being disabled, the SS pin will be quickly discharged.
OPWM	12	PWM Gate Drive	The totem-pole output drive for the Flyback PWM MOSFET. This pin is internally clamped under 17V to protect the MOSFET.
GND	13	Ground	Power ground.
OPFC	14	PFC Gate Drive	The totem-pole output drive for the PFC MOSFET. This pin is internally clamped under 17V to protect the MOSFET.
VDD	15	Supply	The power supply pin.
RANGE	16	PFC Output Voltage Control	Two-level output voltage setting for PFC. The PFC output voltage at low line can be reduced to improve efficiency. The RANGE pin has high impedance whenever the V_{RMS} voltage is lower than a threshold.
OVP	17	PFC Over-Voltage Input	The PFC stage over voltage input. The comparator disables the PFC output driver if the voltage at this input exceeds a threshold. This pin can be connected to FBPFC or it can be connected to the PFC boost output through a divider network.
FBPFC	18	Voltage Feedback Input for PFC	The feedback input for PFC voltage loop. The inverting input of PFC error amplifier. This pin is connected to the PFC output through a divider network.
VEA	19	Error Amplifier Output for PFC Voltage Feedback Loop	The error amplifier output for PFC voltage feedback loop. A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value results in a narrow bandwidth and improves the power factor.
IAC	20	Input AC Current	This input is used to provide current reference for the multiplier.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{VDD}	DC Supply Voltage*	25	V
I_{AC}	Input AC Current	2	mA
V_{High}	OPWM, OPFC, IAC	-0.3 to +25.0	V
V_{Low}	Others	-0.3 to +7.0	V
P_D	Power Dissipation at T_A < 50°C	1.15	W
T_J	Operating Junction Temperature	-40 to +125	°C
T_{STG}	Storage Temperature Range	-55 to +150	°C
$R_{\theta JC}$	Thermal Resistance (Junction-to-Case)	23.64	°C/W
T_L	Lead Temperature (Wave Soldering or Infrared, 10 Seconds)	260	°C
$V_{ESD,HBM}$	Electrostatic Discharge Capability, Human Body Model	4.5	KV
$V_{ESD,MM}$	Electrostatic Discharge Capability, Machine model	250	V

*All voltage values, except differential voltages, are given with respect to GND pin.

*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
T_A	Operating Ambient Temperature*	-20 to +85	°C

*For proper operation.

ELECTRICAL CHARACTERISTICS

V_{DD}=15V, T_A=25°C unless otherwise noted.

V_{DD} Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD-OP}	Continuously Operating Voltage				20	V
I_{DD-ST}	Start-up Current	0V < V_{DD} < V_{DD-ON}		10	25	μA
I_{DD-OP}	Operating Current	V_{DD}=15V; OPFC, OPWM open; R_I=24KΩ		6	10	mA
V_{DD-ON}	Start Threshold Voltage		11	12	13	V
V_{DD-OFF}	Minimum Operating Voltage		9	10	11	V
V_{DD-OVP}	V_{DD} OVP Threshold		23.5	24.5	25.5	V
$t_{D-VDDOVP}$	Debounce Time of V_{DD} OVP		8		25	μs

Oscillator Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{OSC}	PWM Frequency	R_I=24KΩ	62	65	68	KHz
R_I	RI Pin Resistance Range		15.6		47.0	KΩ
RI_{OPEN}	RI Pin Open Protection If R_I > RI_{open} , SG6901A Turns Off			200		KΩ
RI_{SHORT}	RI Pin Short Protection If R_I < RI_{short} , SG6901A Turns Off			2		KΩ

VRMS for UVP and RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{RMS-UVP-1}$	RMS AC Voltage Under-Voltage Protection Threshold (with t_{UVP} delay)		0.75	0.8	0.85	V
$V_{RMS-UVP-2}$	Recovery Level on V_{RMS}		$V_{RMS-UVP-1}$ + 0.16V	$V_{RMS-UVP-1}$ + 0.18V	$V_{RMS-UVP-1}$ + 0.2V	V
t_{D-PWM}	When UVP Occurs, Interval from PFC Off to PWM Off		$t_{UVP-Min}$+9		$t_{UVP-Min}$+14	ms
t_{UVP}	Under-Voltage Protection Delay Time*		150	195	240	ms
V_{RMS-H}	High V_{RMS} Threshold for RANGE Comparator		1.90	1.95	2.00	V
V_{RMS-L}	Low V_{RMS} Threshold for RANGE Comparator		1.55	1.60	1.65	V
t_{RANGE}	Range-Enable Delay Time		140	170	200	ms
V_{OL}	Output Low Voltage of RANGE Pin	I_o=1mA			0.5	V
I_{OH}	Output High Leakage Current of RANGE Pin	RANGE=5V			50	nA

* No delay for start-up.

PFC Stage

Voltage Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{REF}	Reference Voltage		2.95	3.00	3.05	V
Av	Open-Loop Gain			60		dB
Z_o	Output Impedance			110		KΩ
OVP_{PFC}	PFC Over-Voltage Protection (OVP Pin)		3.20	3.25	3.30	V
$\triangle OVP_{PFC}$	PFC Feedback Voltage Protection Hysteresis		60	90	120	mV
$t_{OVP-PFC}$	Debounce Time of PFC OVP		40	70	120	μs
$V_{FBPFC-H}$	Clamp-High Feedback Voltage		3.10	3.15	3.20	V
$G_{FBPFC-H}$	Clamp-High Gain			0.5		μA/mV
$V_{FBPFC-L}$	Clamp-Low Feedback Voltage		2.75	2.85	2.90	V
$G_{FBPFC-L}$	Clamp-Low Gain			6.5		mA/mV
$I_{FBPFC-L}$	Maximum Source Current		1.5	2.0		mA
$I_{FBPFC-H}$	Maximum Sink Current		70	110		μA
UVP_{FBPFC}	PFC Feedback Under-Voltage Protection		0.35	0.40	0.45	V
$t_{UVP-FBPFC}$	Debounce Time of PFC UVP		40	70	120	μs

Current Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OFFSET}	Input Offset Voltage ((-) > (+))			8		mV
A_I	Open-Loop Gain			60		dB
BW	Unit Gain Bandwidth			1.5		MHz
CMRR	Common Mode Rejection Ratio	V_{CM}=0 to +1.5V		70		dB
$V_{OUT-HIGH}$	Output High Voltage		3.2			V
$V_{OUT-LOW}$	Output Low Voltage				0.2	V
I_{MR1}, I_{MR2}	Reference Current Source	R_I=24KΩ (I_{MR}=20+I_{RI}•0.8)	50		70	μA
I_L	Maximum Source Current		3			mA
I_H	Maximum Sink Current			0.25		mA

Peak Current Limit

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_P	Constant Current Output	R_I=24KΩ	90	100	110	μA
V_{PK}	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit (V_{SENSE} < V_{PK})	V_{RMS}=1.05V	0.15	0.20	0.25	V
		V_{RMS}=3V	0.35	0.40	0.45	V
t_{PD-PFC}	Propagation Delay				200	ns
$t_{LEB-PFC}$	Leading-Edge Blanking Time		270	350	450	ns

Multiplier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AC}	Input AC Current	Multiplier Linear Range	0		360	μA
I_{MO-max}	Maximum Multiplier Current Output	R_I=24KΩ		250		μA
I_{MO-1}	Multiplier Current Output (Low-line, High-power)	V_{RMS}=1.05V; I_{AC}=90μA; V_{EA}=7.5V; R_I=24KΩ	200	250	280	μA
I_{MO-2}	Multiplier Current Output (High-line, High-power)	V_{RMS}=3V; I_{AC}=264μA; V_{EA}=7.5V; R_I=24KΩ	65	85		μA
V_{IMP}	Voltage of IMP Open		3.4	3.9	4.4	V

PFC Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_Z	Output Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
V_{OL-PFC}	Output Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
t_{PFC}	Interval OPFC Lags Behind OPWM at Start-up		9.0	11.5	14.0	ms
V_{OH-PFC}	Output Voltage High	V_{DD}=13V; I_O=100mA	8			V
t_{R-PFC}	Rising Time	V_{DD}=15V; C_L=5nF; O/P=2V to 9V	40	70	120	ns
t_{F-PFC}	Falling Time	V_{DD}=15V; C_L=5nF; O/P=9V to 2V	40	60	110	ns
DCY_{MAX}	Maximum Duty Cycle		93		98	%

PWM Stage

FBPWM

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
A_{v-PWM}	FB to Current Comparator Attenuation		2.5	3.1	3.5	V/V
Z_{FB}	Input Impedance		4	5	7	KΩ
I_{FB}	Maximum Source Current		0.8	1.2	1.5	mA
$FB_{OPEN-LOOP}$	PWM Open-Loop Protection voltage		4.2	4.5	4.8	V
$t_{OPEN-PWM}$	PWM Open-Loop Protection Delay Time		45	56	70	ms
$t_{OPEN-PWM-Hiccup}$	Interval of PWM Open-Loop Protection Reset		450	600	750	ms

PWM-Current Sense

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PD-PWM}	Propagation Delay to Output	VDD=15V,OPWM<=9V	60		120	ns
$V_{LIMIT-1}$	Peak Current Limit Threshold Voltage1	RANGE=Open	0.65	0.70	0.75	V
$V_{LIMIT-2}$	Peak Current Limit Threshold Voltage2	RANGE=Ground	0.60	0.65	0.70	V
$t_{LEB-PWM}$	Leading-Edge Blanking Time		270	350	450	ns
$\triangle V_{SLOPE}$	Slope Compensation	$\triangle V_S = \triangle V_{SLOPE} \times (T_{on}/T)$ $\triangle V_S$: Compensation Voltage Added to Current Sense	0.45	0.50	0.55	V

PWM Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Z-PWM}	Output Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
V_{OL-PWM}	Output Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
V_{OH-PWM}	Output Voltage High	V_{DD}=13V; I_O=100mA	8			V
t_{R-PWM}	Rising Time	V_{DD}=15V; C_L=5nF; O/P=2V to 9V	30	60	120	ns
t_{F-PWM}	Falling Time	V_{DD}=15V; C_L=5nF; O/P=9V to 2V	30	50	110	ns
DCY_{MAXPWM}	Maximum Duty Cycle		73	78	83	%

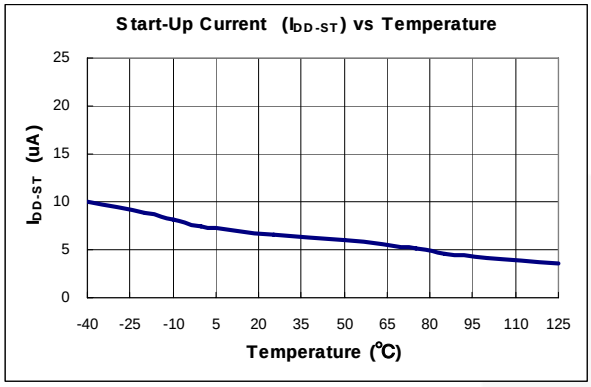
OTP Section

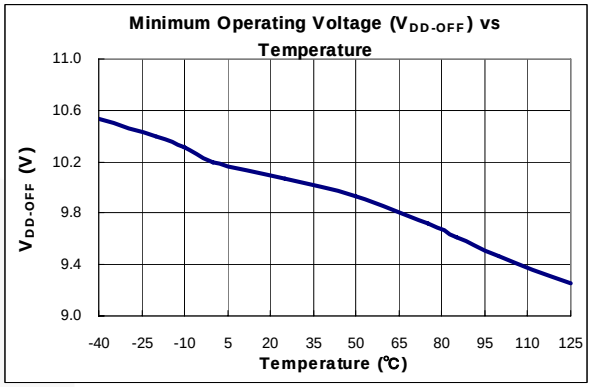
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{OTP}	OTP Pin Output Current	R_I=24KΩ	90	100	110	μA
V_{OTP-ON}	Recovery Level on OTP		1.35	1.40	1.45	V
$V_{OTP-OFF}$	OTP Threshold Voltage		1.15	1.20	1.25	V
t_{OTP}	OTP Debounce Time		8		25	μs

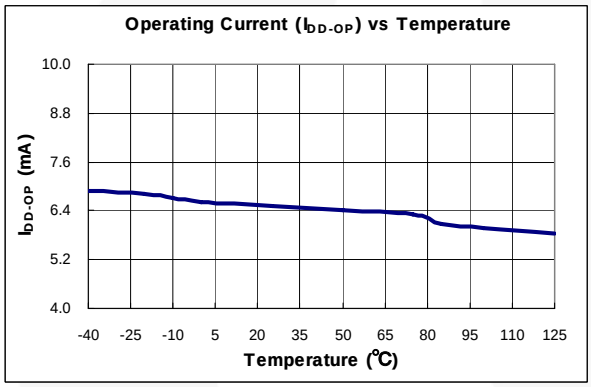
Soft-Start Section

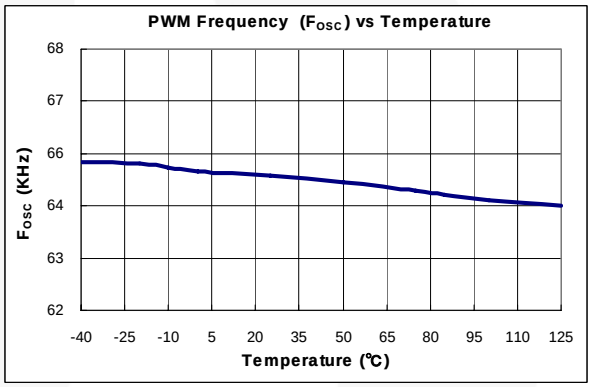
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SS}	Constant Current Output for Soft-Start	R_T=24KΩ	44	50	56	μA
R_D	Discharge R_{DSON}			470		Ω

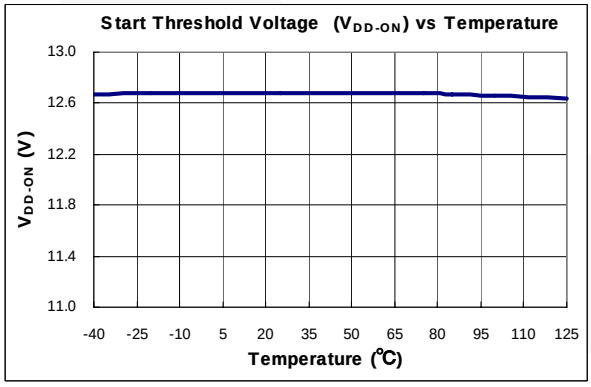
TYPICAL CHARACTERISTICS

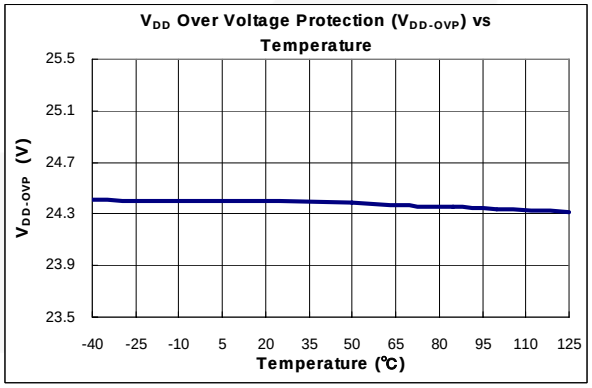


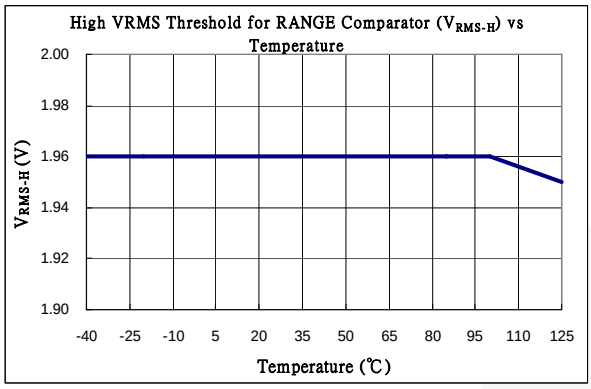


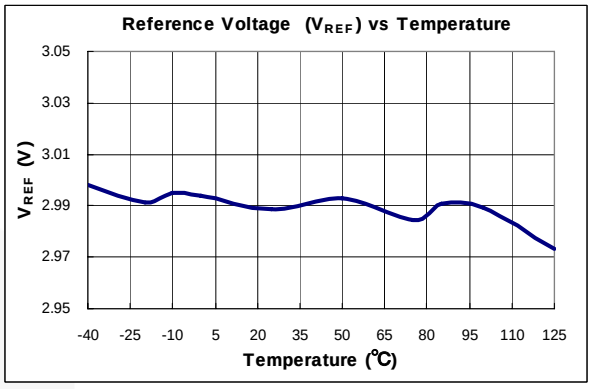


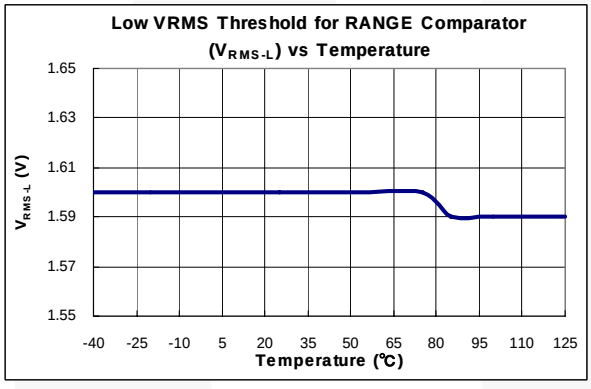


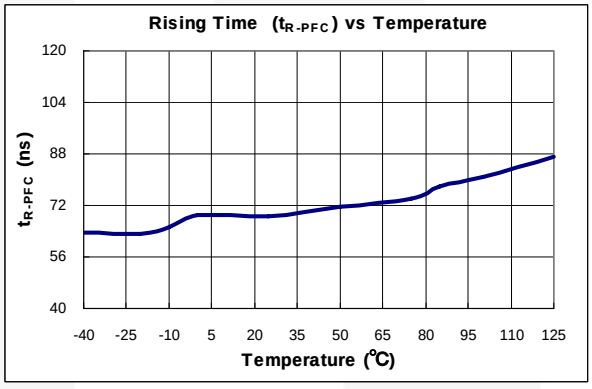


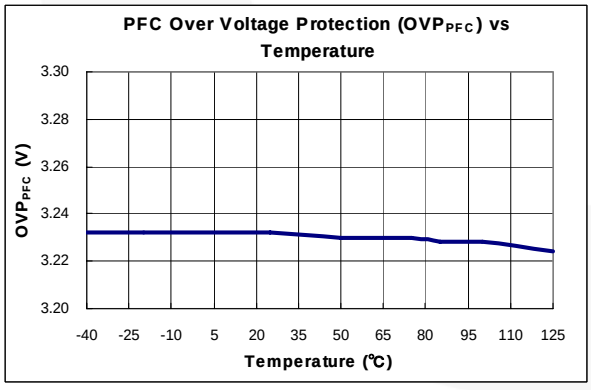


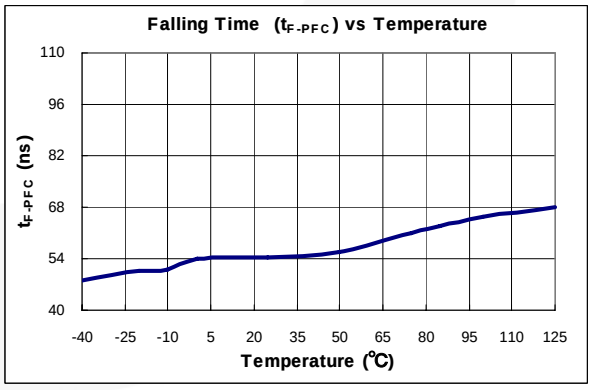

High VRMS Threshold for RANGE Comparator (V_{RMS-H}) vs Temperature
V_{RMS-H} (V)
2.00
1.98
1.96
1.94
1.92
1.90
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

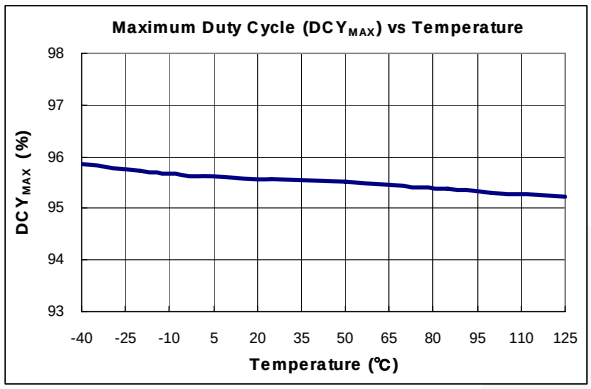

Reference Voltage (V_{REF}) vs Temperature
V_{REF} (V)
3.05
3.03
3.01
2.99
2.97
2.95
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

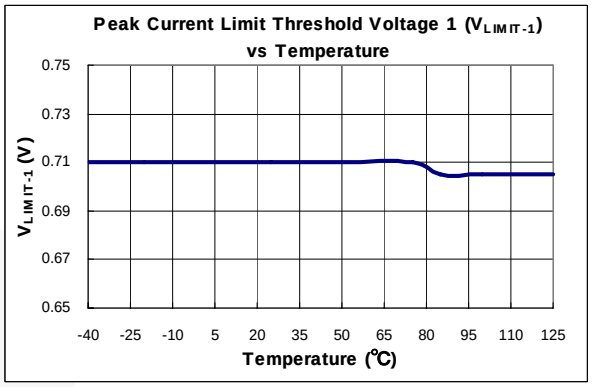

Low VRMS Threshold for RANGE Comparator (V_{RMS-L}) vs Temperature
V_{RMS-L} (V)
1.65
1.63
1.61
1.59
1.57
1.55
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

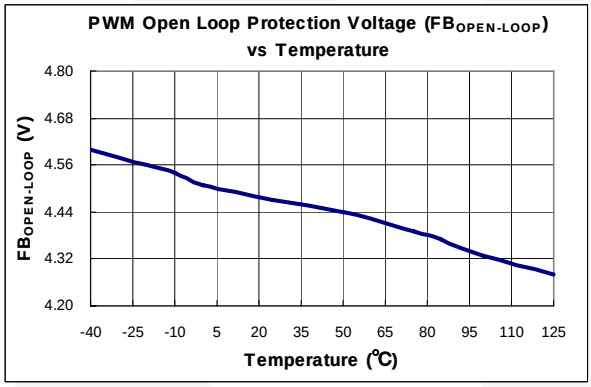

Rising Time (t_{R-PFC}) vs Temperature
t_{R-PFC} (ns)
120
104
88
72
56
40
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

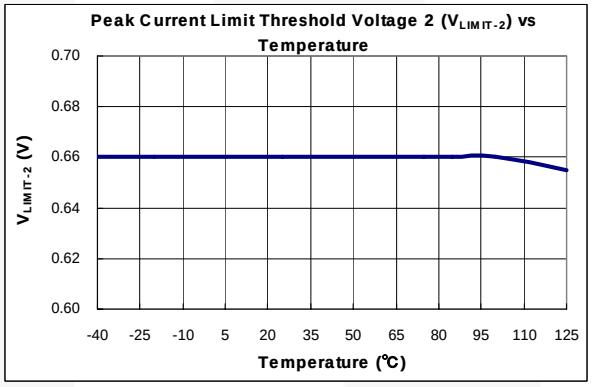

PFC Over Voltage Protection (OVP_{PFC}) vs Temperature
OVP_{PFC} (V)
3.30
3.28
3.26
3.24
3.22
3.20
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

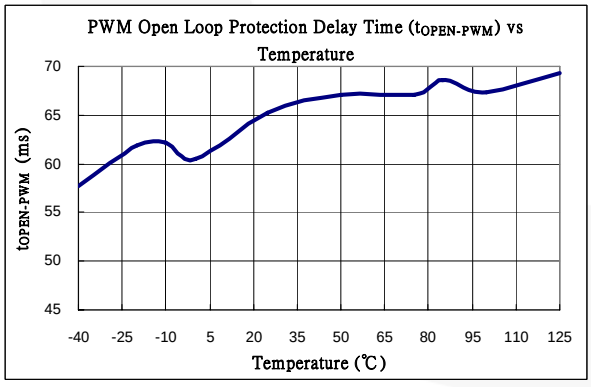

Falling Time (t_{F-PFC}) vs Temperature
t_{F-PFC} (ns)
110
96
82
68
54
40
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

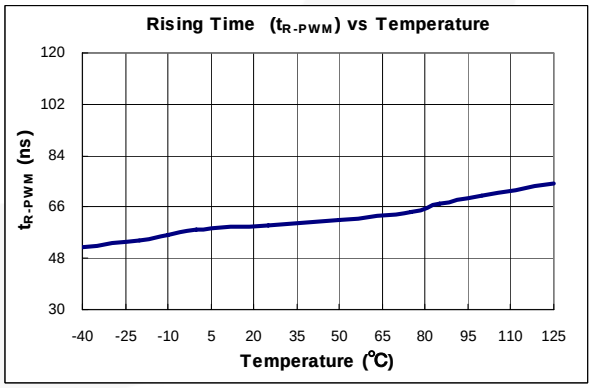

Maximum Duty Cycle (DCY$_{MAX}$) vs Temperature
DCY$_{MAX}$ (%)
98
97
96
95
94
93
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

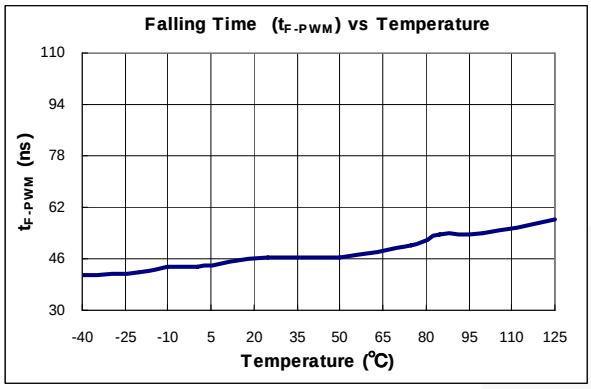

Peak Current Limit Threshold Voltage 1 (V$_{LIMIT-1}$) vs Temperature
V$_{LIMIT-1}$ (V)
0.75
0.73
0.71
0.69
0.67
0.65
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

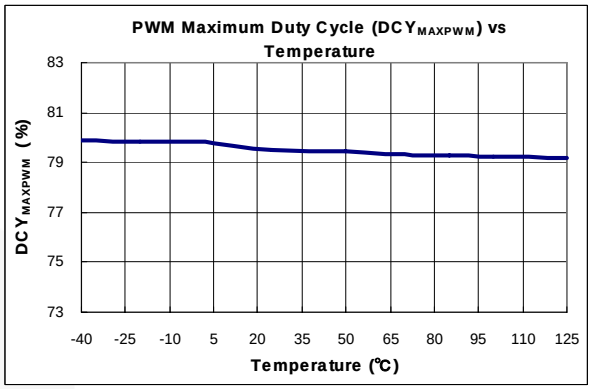

PWM Open Loop Protection Voltage (FB$_{OPEN-LOOP}$) vs Temperature
FB$_{OPEN-LOOP}$ (V)
4.80
4.68
4.56
4.44
4.32
4.20
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

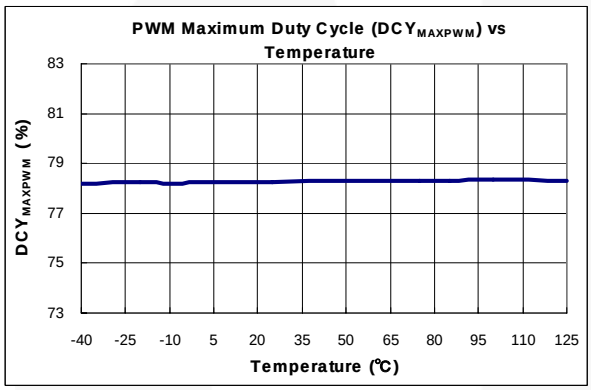

Peak Current Limit Threshold Voltage 2 (V$_{LIMIT-2}$) vs Temperature
V$_{LIMIT-2}$ (V)
0.70
0.68
0.66
0.64
0.62
0.60
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

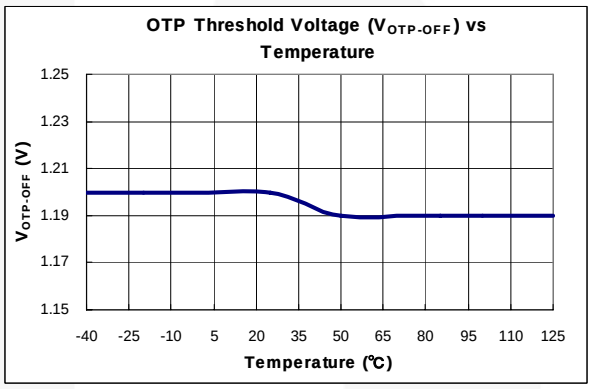

PWM Open Loop Protection Delay Time (t$_{OPEN-PWM}$) vs Temperature
t$_{OPEN-PWM}$ (ms)
70
65
60
55
50
45
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Rising Time (t$_{R-PWM}$) vs Temperature
t$_{R-PWM}$ (ns)
120
102
84
66
48
30
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Falling Time (t_{F-PWM}) vs Temperature
110
94
78
62
46
30
t_{F-PWM} (ns)
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


PWM Maximum Duty Cycle (DCY_{MAXPWM}) vs Temperature
83
81
79
77
75
73
DCY_{MAXPWM} (%)
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


PWM Maximum Duty Cycle (DCY_{MAXPWM}) vs Temperature
83
81
79
77
75
73
DCY_{MAXPWM} (%)
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


OTP Threshold Voltage ($V_{OTP-OFF}$) vs Temperature
1.25
1.23
1.21
1.19
1.17
1.15
$V_{OTP-OFF}$ (V)
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

OPERATION DESCRIPTION

SG6901A is a highly integrated PFC/PWM combination controller. Many functions and protections are built in to provide a compact design. The following sections describe the operation and function.

Switching Frequency and Current Sources

The switching frequency of SG6901A can be programmed by the resistor R_I connected between RI pin and GND. The relationship is:

$$F_{OSC} = \frac{1560}{R_I\ (k\Omega)}(kHz) \text{ ----------} \quad (1)$$

For example, a 24KΩ resistor R_I results in a 65KHz switching frequency. Accordingly, a constant current, I_T, flows through R_I:

$$I_T = \frac{1.2V}{R_I\ (k\Omega)}(mA) \text{ ----------} \quad (2)$$

I_T is used to generate internal current reference.

Line Voltage Detection (VRMS)

Figure 1 shows a resistive divider with low-pass filtering for line-voltage detection on the VRMS pin. The V_{RMS} voltage is used for the PFC multiplier, brownout protection, and range control.

For brownout protection, the SG6901A is disabled with 195ms delay time if the voltage V_{RMS} drops below 0.8V.

For PFC multiplier and range control, refer to section below for more details.

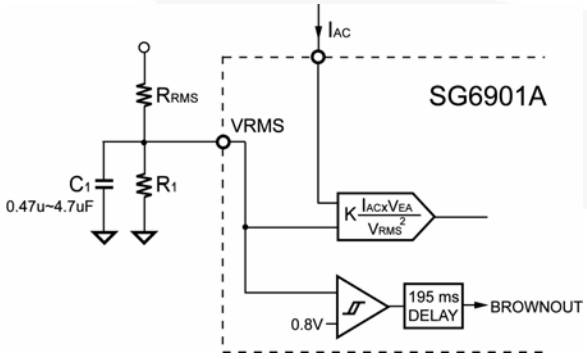


FIG.1 Line Voltage Detection Circuit

PFC Output Voltage Control (RANGE)

For an universal input (90 ~ 264V_{AC}) power supply applying active boost PFC and flyback as a second stage, the output voltage of PFC is usually designed around 250V at low line and 390V at high line. This can improve the efficiency at low-line input. The RANGE pin (open-drain structure) is used for the two-level output voltage setting.

Figure 2 shows the RANGE output that programs the PFC output voltage. The RANGE output is shorted to ground when the V_{RMS} voltage exceeds V_{RMS-H} (1.95V) while it is of high impedance (open) whenever the V_{RMS} voltage drops below V_{RMS-L} (1.6V). The output voltages can be designed using equations:

$$\text{Range} = \text{Open} \Rightarrow V_O = \frac{R_A + R_B}{R_B} \times 3V \quad \text{----} \quad (3)$$

$$\text{Range} = \text{Ground} \Rightarrow V_O = \frac{R_A + (R_B // R_C)}{(R_B // R_C)} \times 3V$$

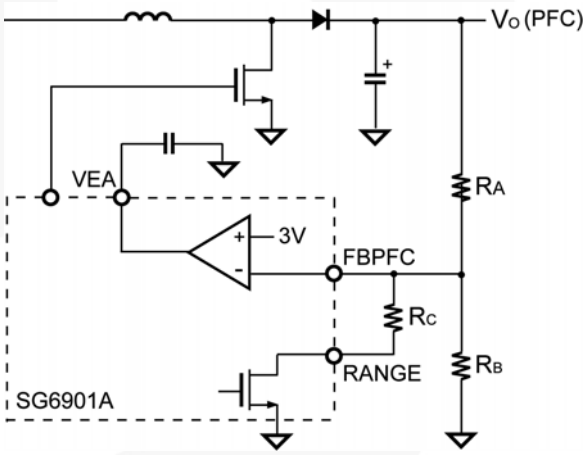


FIG.2 Range Control Two-Level Output Voltage

Interleave Switching

The SG6901A uses interleaved switching to synchronize the PFC and flyback stages, which reduces switching noise and spreads the EMI emissions. Figure 3 shows off-time, T_{OFF}, inserted between the turn-off of the PFC gate drive and the turn-on of the PWM.

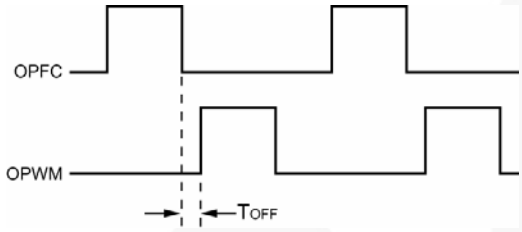


FIG.3 Interleaved Switching Pattern

PFC Operation

The purpose of a boost active power factor corrector (PFC) is to shape the input current of a power supply. The input current waveform and phase follow that of the input voltage. Average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and switching charge multiplier-divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 4 shows the total control loop for the average-current-mode control circuit of SG6901A.

The current source output from the switching charge multiplier-divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} (\mu A) \quad \text{----------} \quad (4)$$

As shown in Figure 4, the current output from IMP pin, I_{MP}, is the summation of I_{MO} and I_{MR1}. I_{MR1} and I_{MR2} are identical fixed-current sources used to pull high the operating point of the IMP and IPFC pins since the voltage across R_S goes negative with respect to ground. Constant current sources I_{MR1} and I_{MR2} are typically 60μA.

Through the differential amplification of the signal across R_S, better noise immunity is achieved. The output of $_{IEA}$ is compared with an internal sawtooth and the pulse width for PFC is determined. Through the average current-mode control loop, the input current I_S is proportional to I_{MO}:

$$I_{MO} \times R_2 = I_S \times R_S \quad \text{----------} \quad (5)$$

According to Equation 5, the minimum value of R_2 and maximum of R_S can be determined since I_{MO} should not exceed the specified maximum value.

There are different concerns in determining the value of the sense resistor R_S. The value of R_S should be small enough to reduce power consumption, but large enough to maintain the resolution. A current transformer (CT) may be used to improve efficiency of high-power converters.

To achieve good power factor, the voltage for V_{RMS} and V_{EA} should be kept as constant as possible, according to Equation 4. Good RC filtering for V_{RMS} and narrow bandwidth (lower than the line frequency) for voltage loop are suggested for better input current shaping. The transconductance error amplifier has output impedance Z_O and a capacitor C_{EA} (1μF ~ 10μF) should be connected to ground. This establishes a dominant pole f1 for the voltage loop:

$$f_1 = \frac{1}{2\pi \times Z_O \times C_{EA}} \quad \text{----------} \quad (6)$$

The average total input power can be expressed as:

$$\begin{aligned} Pin &= V_{IN(rms)} \times I_{IN(rms)} \\ &\propto V_{RMS} \times I_{MO} \\ &\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} \\ &\propto V_{RMS} \times \frac{\frac{Vin}{R_{AC}} \times V_{EA}}{V_{RMS}^2} \\ &= \sqrt{2} \times \frac{V_{EA}}{R_{AC}} \end{aligned} \quad \text{----------} \quad (7)$$

From Equation 7, V_{EA}, the output of the voltage error amplifier, controls the total input power and the power delivered to the load.

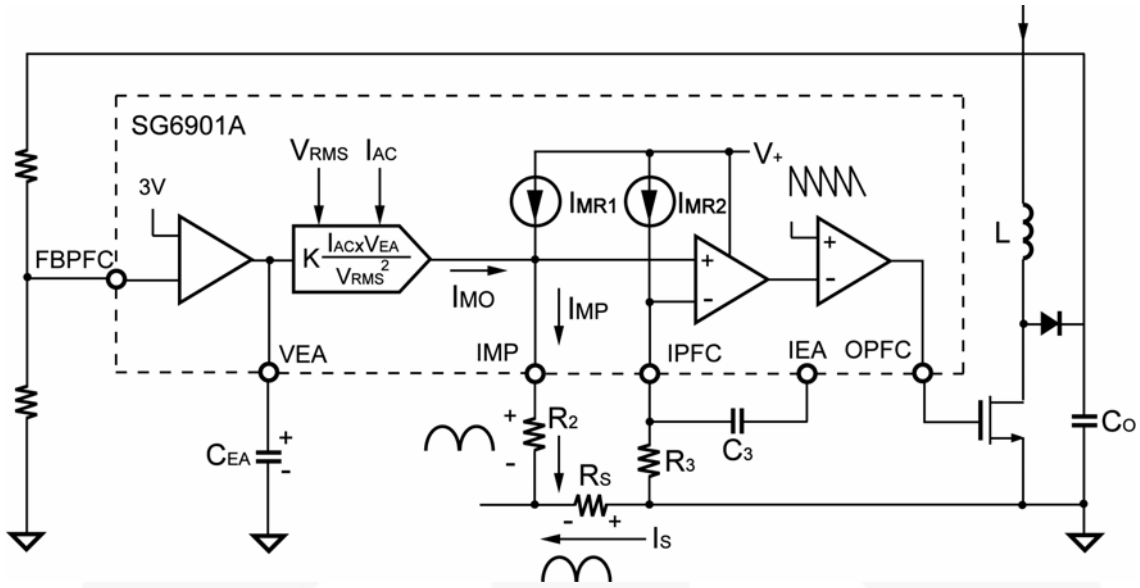


FIG.4 Average-Current-Mode Control Loop

Multi-Vector Error Amplifier

Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative multi-vector error amplifier provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

Figure 5 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds ±5% of the reference voltage, the transconductance error amplifier adjusts its output impedance to increase the loop response.

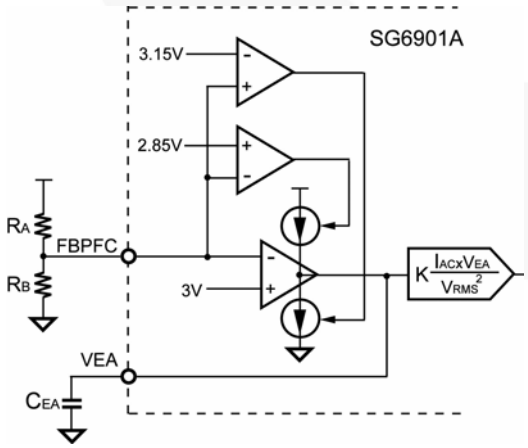


FIG. 5 Multi-Vector Error Amplifier

PFC Over-Voltage Protection

Using a voltage divider from the output of PFC to the OVP pin, the PFC output voltage can be safely protected.

Once the voltage on the OVP pin is over OVP_{PFC}, the OPFC is disabled. THE OPFC is not enabled again until the OVP voltage falls below OVP_{PFC}.

Cycle-by-Cycle Current Limiting

SG6901A provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 6 shows the peak current limit for the PFC stage. The PFC gate drive is terminated once the voltage on the ISENSE pin goes below V_{PK}.

The voltage of V_{RMS} determines the voltage of V_{PK}. The relationship between V_{PK} and V_{RMS} is shown in Figure 6.

The amplitude of the constant current, I_P, is determined by the internal current reference according to the equation:

$$I_P = 2 \times \frac{1.2V}{R_I} \quad \text{----------} \quad (8)$$

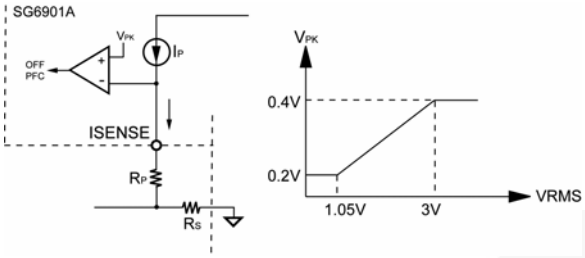


FIG. 6 V_{RMS} Controlled Current Limiting

The peak current of the I_{SENSE} is given by (V_{RMS}<1.05V):

$$I_{SENSE\_peak} = \frac{(I_P \times R_P) - 0.2V}{R_S} \quad \text{----------} \quad (9)$$

Flyback PWM and Slope Compensation

As shown in Figure 7, peak-current-mode control is utilized for flyback PWM. The SG6901A inserts a synchronized 0.5V ramp at the beginning of each switching cycle. This built-in slope compensation ensures stable operation for continuous current-mode operation.

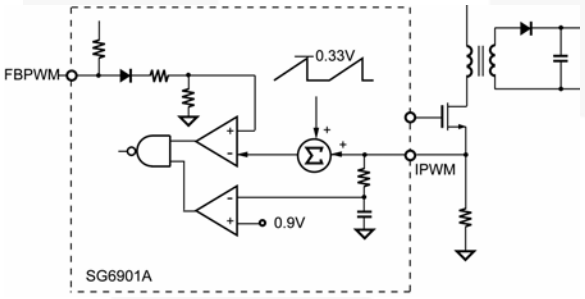


FIG. 7 Peak Current Control Loop

When the IPWM voltage, across the sense resistor, reaches the threshold voltage (0.9V), the OPWM is turned off after a small propagation delay t_{PD-PWM}.

To improve stability or prevent sub-harmonic oscillation, a synchronized positive-going ramp is inserted at every switching cycle.

Limited Power Control

Every time the output of power supply is shorted or overloaded, the FBPWM voltage increases. If the FBPWM voltage is higher than a designed threshold, $FB_{OPEN-LOOP}$ (4.5V) for longer than $t_{OPEN-PWM}$ (56ms), the OPWM is turned off.

As long as the voltage on the VDD pin is larger than V_{DD-OFF} (minimum operating voltage), the OPWM is not enabled. This protection is reset every $t_{OPEN-PWM-Hiccup}$ interval. A low-frequency hiccup mode protection prevents the power supply from being overheated under overloading conditions.

Over-Temperature Protection

SG6901A provides an OTP pin for over-temperature protection. A constant current is output from this pin. If R_I is equal to 24KΩ, the magnitude of the constant current is 100μA. An external NTC thermistor must be connected from this pin to ground, as shown as Figure 8. When the OTP voltage drops below $V_{OTP-OFF}$ (1.2V), SG6901A is disabled and does not recover until OTP voltage exceeds V_{OTP-ON} (1.4V).

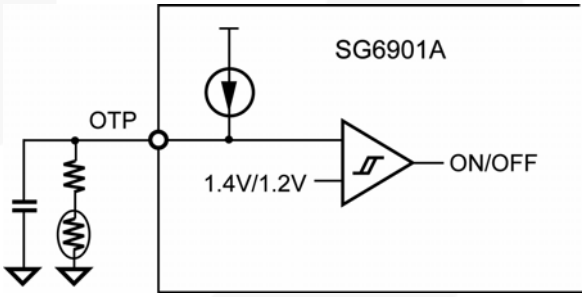


FIG. 8 OTP Function

Soft-Start

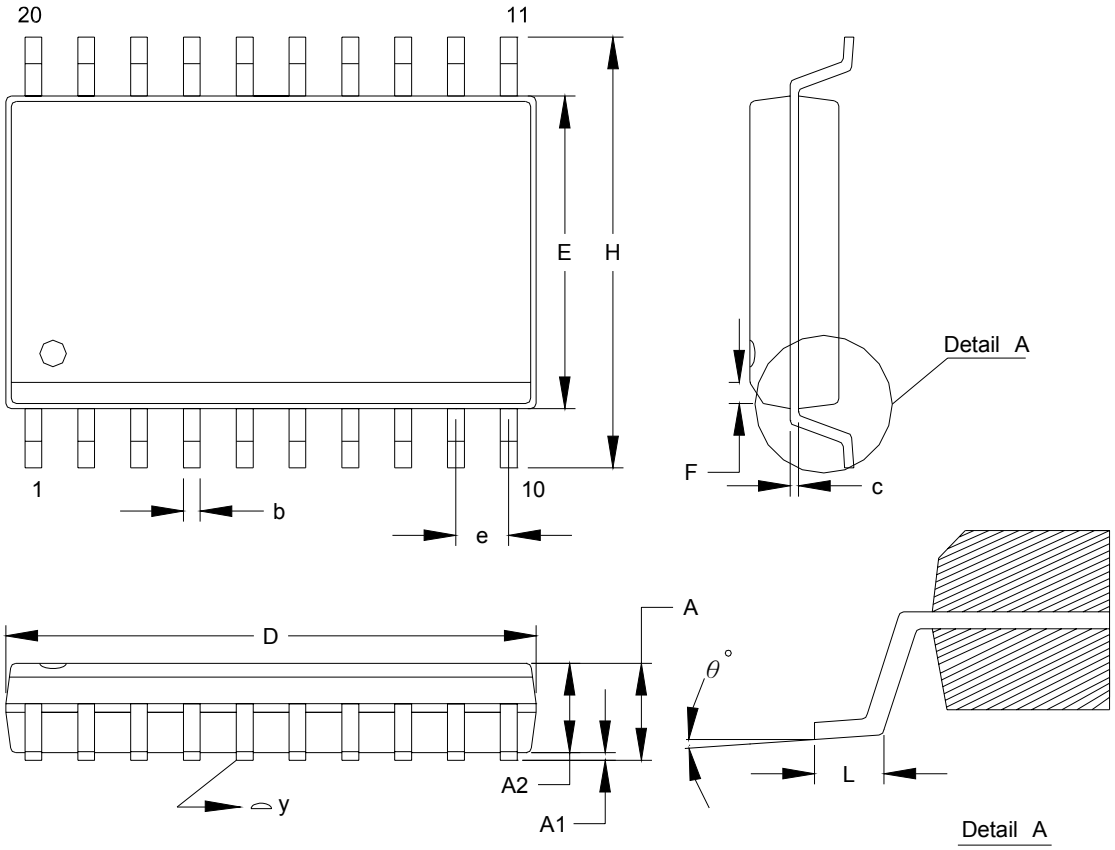
During start-up of PWM stage, the SS pin charges an external capacitor with a constant current source. The voltage on FBPWM is clamped by the SS voltage during start-up. In the event of a protected condition and/or PWM disabled, the SS pin quickly discharges.

Gate Drivers

SG6901A output stage is a fast totem-pole gate driver. The output driver is clamped by an internal 18V Zener diode to protect the external power MOSFET.

PACKAGE INFORMATION

20 PINS – PLASTIC SOP (S)



Dimensions:

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.362		2.642	0.093		0.104
A1	0.101		0.305	0.004		0.012
A2	2.260		2.337	0.089		0.092
b		0.406			0.016	
c		0.203			0.008	
D	12.598		12.903	0.496		0.508
E	7.391		7.595	0.291		0.299
e		1.270			0.050	
H	10.007		10.643	0.394		0.419
L	0.406		1.270	0.016		0.050
F		0.508X45°			0.020X45°	
y			0.101			0.004
θ°	0°		8°	0°		8°

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QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
The Power Franchise®
the power franchise
TinyBoost™
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TINYOPTO™
TinyPower™
TinyPWM™
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