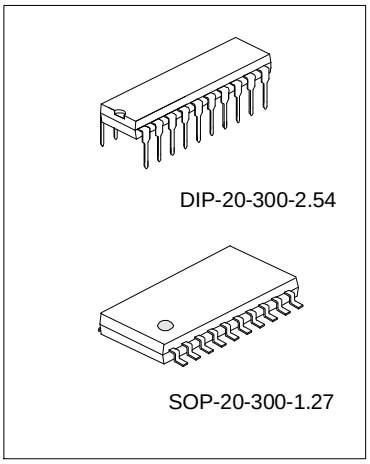
PLL FOR DIGITAL TUNING SYSTEM

DESCRIPTION

The SC9257 is phase-locked loop (PLL) LSIs for digital tuning systems (DTS) with built in 2 modulus prescalers.

The LSIs are used to configure high-performance digital tuning systems, such as radio/cassette players. They allow high-performance AM/FM tuners to be implemented easily



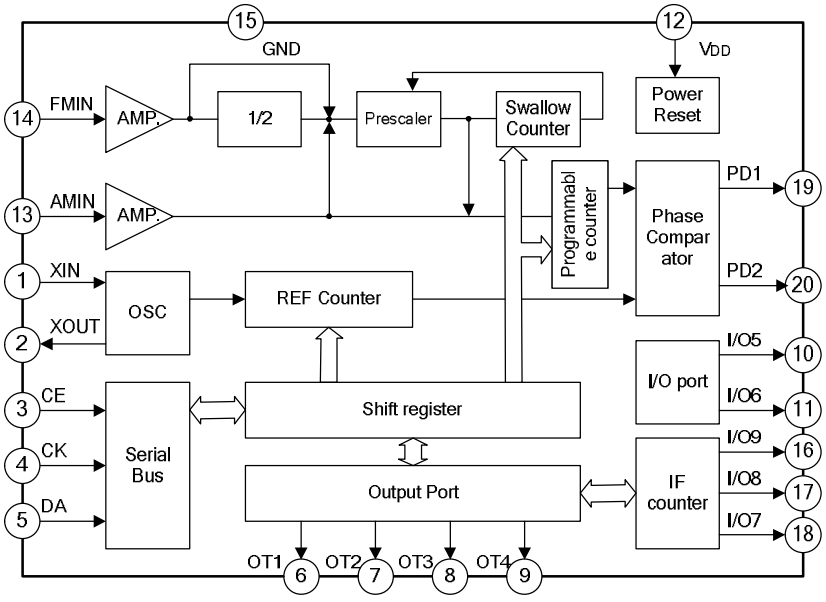
FEATURES

* Available in DIP20, SOP20 packages.
* High speed programmable dividers.
  — FMIN: 30 to 150 MHz .....(with 2 modulus prescaler)
  — AMIN: 0.5 to 40 MHz .....(with 2 modulus prescaler or direct dividing)
* 16-bit programmable counter, dual parallel output phase comparator, crystal oscillator and reference counter.
* Uses 3.6MHz, 4.5MHz, 7.2MHz or 10.8MHz crystal oscillators
* Has 15 reference FM and AM frequencies : 0.5K, 1K, 2.5K, 3K, 3.125K, 3.90625K, 5K, 6.25K, 7.8125K, 9K, 10K, 12.5K, 25K, 50K, 100K (When using 4.5MHz crystal)
* Has an intermediate frequency (IF) measurement counter.
* Numerous general-purpose I/O pins for such uses as peripheral circuit control.
* Has 4 output ports that are open drain.
* Turns off FM, AM and IF amps when Standby mode function
* Serial data input and interface (CE,CK,DA).
* Supply voltage : 4.5 to 5.5 V

ORDERING INFORMATION

Device	Package
SC9257	DIP-20-300-2.54
SC9257S	SOP-20-300-1.27

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_{amb}=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.3~6.0	V
Input Voltage	V_{IN}	-0.3~V_{DD}+0.3	V
N-ch Open-Drain Off withstanding Voltage	V_{OFF}	13	V
Power Dissipation	P_D	300(200)	mW
Operating Temperature	T_{OPR}	-40~85	°C
Storage Temperature	T_{STG}	-65~150	°C

ELECTRICAL CHARACTERISTICS (unless otherwise specified, T_{amb}= -40~85°C, V_{DD}=4.5~5.58V.)

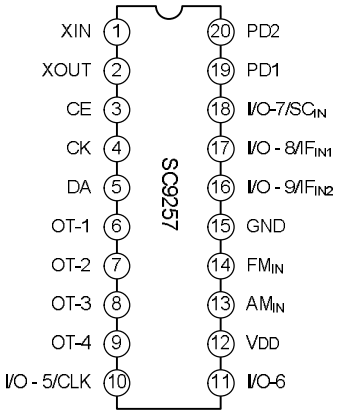
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Power Supply Voltage	V_{DD1}	PLL operation (normal operating)	3.5	4.2	5.5	V
Operating Power Supply Current	I_{DD1}	V_{DD}=5.0V, X_{IN}=10.8MHz, F_{MIN}=150MHz	--	8	15	mA
Stand-by mode						
Crystal Oscillation Frequency Supply Voltage	V_{DD2}	PLL OFF (Operating crystal oscillation)	4.0	5.0	5.5	V
Operating Power Supply Current	I_{DD2}	V_{DD}=5.0V, X_{IN} =7.2MHz PLL OFF	--	0.81	1.50	mA
Operating Power Supply Current	I_{DD3}	V_{DD}=5.0V, X_{IN} stop, PLL OFF	--	140	280	μA
Operating frequency range						
Crystal Oscillation Frequency	f_{XIN}	Connect crystal resonator to X_{IN}-X_{OUT} terminal	3.6	~	10.8	MHz
FMIN (FMH, FML)	f_{FM}	FMH, FML mode, V_{IN}=0.2Vp-p	30	~	150	MHz
FMIN (FML)	f_{FML}	FML mode, V_{IN}=0.3Vp-p	30	~	150	MHz
AMIN (HF)	f_{HF}	HF mode, V_{IN}=0.2Vp-p	1	~	50	MHz
AMIN (LF)	f_{LF}	LF mode, V_{IN}=0.2Vp-p	0.8	~	50	MHz
IFIN1, IFIN2	f_{IF}	V_{IN}=0.2Vp-p	1.0	~	30	MHz
SCIN	f_{SC}	V_{IH}=0.7V_{DD}, V_{IL}=0.3V_{DD}, square wave input.	--	~	100	kHz
Operating input amplitude range						
FMIN (FMH, FML)	V_{FM}	FMH, FML mode, f_{IN}=30~130MHz	0.2	~	V_{DD}-0.5	Vp-p
FMIN (FML)	V_{FML}	FML mode, f_{IN}=30~150MHz	0.3	~	V_{DD}-0.5	Vp-p
AMIN (HF)	V_{HF}	HF mode, f_{IN}=1~40MHz	0.2	~	V_{DD}-0.5	Vp-p
AMIN (LF)	V_{LF}	LF mode, f_{IN}=0.5~20MHz	0.2	~	V_{DD}-0.5	Vp-p
IFIN1, IFIN2	VIF	F_{IN}=0.1~15MHz	0.2	~	V_{DD}-0.5	Vp-p

(To be continued)

(Continued)

Parameter		Symbol	Test Condition	Min.	Typ.	Max.	Unit
OT1~OT4 N-ch open drain							
Output Current	"L" level	I_{OL1}	V_{OL}=5.0V	30.0	60.0	--	mA
OFF-leak Current		I_{OEF}	V_{IN}=5V	--	---	1.0	μA
I/O-5~I/O-9, SCIN							
Input Voltage	"H" level	V_{IH1}		0.7V_{DD}	~	V_{DD}	V
	"L" level	V_{IL1}		0	~	0.3V_{DD}	
Input Current	"H" level	I_{IH}	V_{IH}=5V	--	--	1.0	μA
	"L" level	I_{IL}	V_{IL}=0V	--	--	-1.0	
Output Current	"H" level	I_{OH4}	V_{OH}=4.0V (expect SCIN)	-10.0	-24.0	--	mA
	"L" level	I_{OL4}	V_{OL}=1.0V (expect SCIN)	5.0	13.0	--	
CE, CK, DA							
Input Voltage	"H" level	V_{IH2}		0.7V_{DD}	~	V_{DD}	V
	"L" level	V_{IL2}		0	~	0.4V_{DD}	
Input Current	"H" level	I_{IH}	V_{IH}=5V	--	--	1.0	μA
	"L" level	I_{IL}	V_{IL}=0V	--	--	-1.0	
Output Current	"H" level	I_{OH5}	V_{OH}=4.0V (DA)	-1.0	-3.0	--	mA
	"L" level	I_{OL5}	V_{OL}=1.0V (DA)	1.0	3.0	--	
PD1, PD2							
Input Current	"H" level	I_{OH3}	V_{OH}=4.0V	-2.0	-10.0	--	mA
	"L" level	I_{OL3}	V_{OL}=1.0V	2.0	5.0	--	
Tri-State Lead Current		I_{TL}	V_{TLH}=5V, V_{TLL}=0V	--	--	±1.0	μA
XOUT							
Output Current	"H" level	I_{OH2}	V_{OH}=4.0V	-0.1	-1.1	--	mA
	"L" level	I_{OL2}	V_{OL}=1.0V	0.1	1.1	--	
Input feedback resistance							
Input Feedback Resistance	"H" level	Rf1	FMIN, AMIN, IFIN (T_{amb}=25°C)	350	700	1400	kΩ
	"L" level	Rf2	X_{IN}-X_{OUT} (T_{amb}=25°C)	500	1900	4000	

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin name	Description
1	XIN	For reference frequency and internal clock generation. Connects 3.6MHz, 4.5MHz, 7.2MHz or 10.8MHz crystal oscillator
2	XOUT	
3	CE	Serial I/O ports. These pins transfer data to and from the controller
4	CK	
5	DA	
6	OT-1	N channel open drain port pins. The output states are determined by O1 to O4 bits in the serial data. All output ports are set to the OFF state when the power is turned on
7	OT-2	
8	OT-3	
9	OT-4	
10	I/O-5/CLK	CMOS structure allows free use of these ports for input or output. Ports are set for input when the power is turned on, I/O-5 can be switched for use as a system clock output pin.
11	I/O-6	
13	AMIN	Oscillator input for AM .
14	FMIN	Oscillator input for AM .
16	I/O-9/IFIN2	I/O port input/output pins. Can be switched for use as IF counter input pins. Pins are set for input when power is turned on.
17	I/O-8/IFIN1	
18	I/O-7/SCIN	I/O port. It can be switched for use as signal input pin to measure low-frequency signal cycles. (note) This pin is set for input when power on.
19	PD1	These pins are for PLL charge pump output. PD1 and PD2 are output in parallel.
20	PD2/OT-4	
15	GND	Power supply pins (V_{DD} = 4.5 to 5.5 V)
12	V_{DD}	

FUNCTION DESCRIPTION

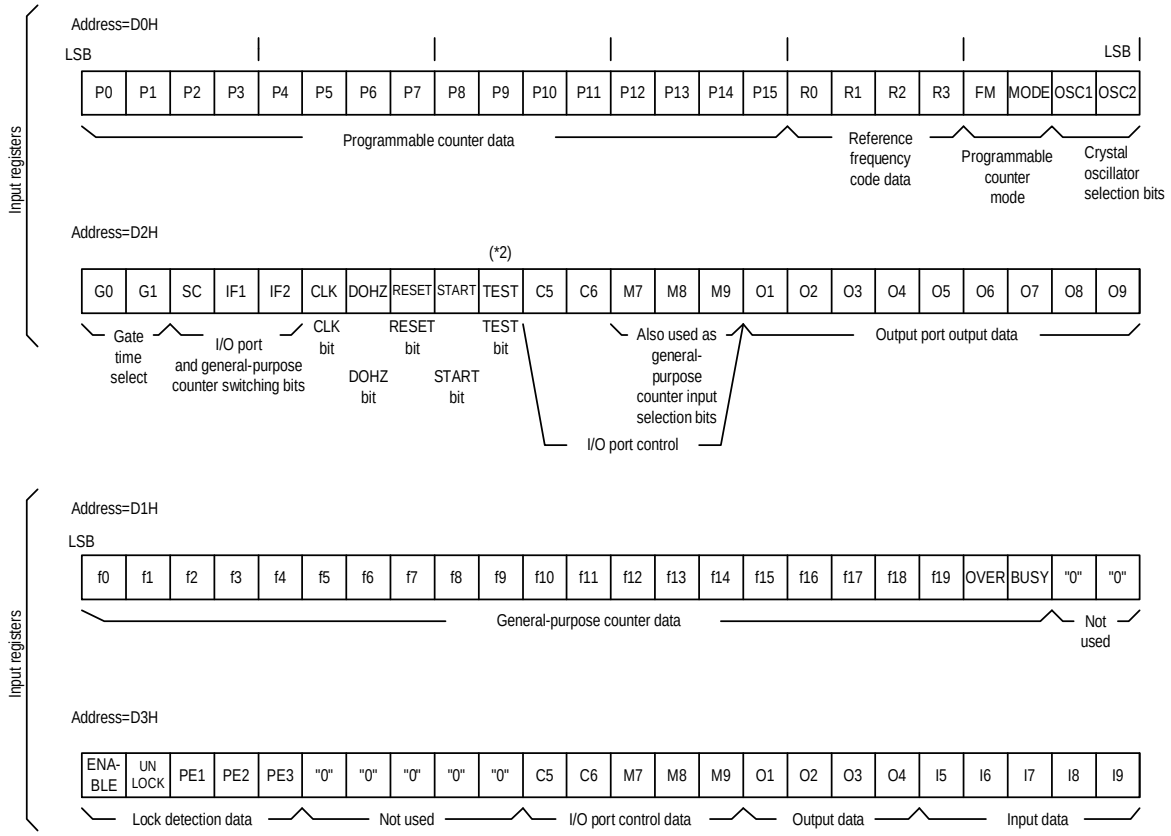
Serial I/O ports

SC9257 has set two 24 bits input registers and two 24 bits output registers. These registers are transferred through the serial ports (DA, CK, CE). Each serial transfer consists of a total of 32 bits, with 8 address bits and 24 data bits.

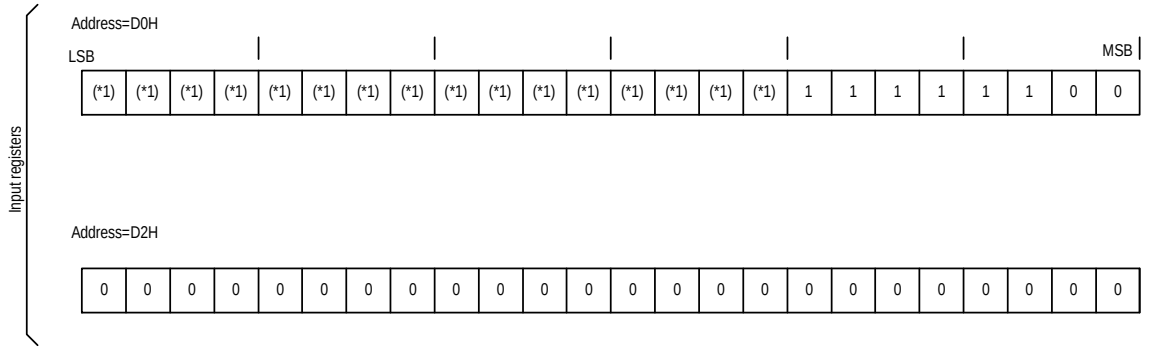
Each register has the only 8 bits address, we can select the register by the 8 bits address, the following table is the address assignment for each register:

Register	Address	Contents of 24 bits	No. of bit
Input register 1	D0H	Control the data input (serial input)	24
Input register 2	D2H	Control the data input (serial input)	24
Output register 1	D1H	Data output (serial output)	24
Output register 2	D3H	Data output (serial output)	24

Register assignments



When power is turned on, the input registers are set as shown below.



Note: 1. Data are undefined.

2. Set data to “0” for test bit.

Serial transfer format

The serial transfer format consists of 32 bits: 8 bits address and 24 bits data, the four registers address are D0H~D3H .

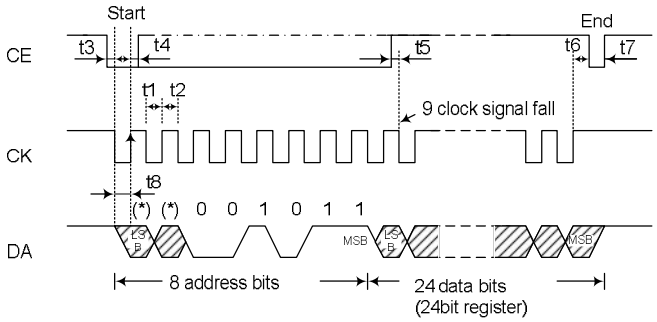


Fig.1

- Serial data transfer

When the serial transfer interface in the idle state, the CE, CK, DA pin lines are set to high level. The CE is used for control the transfer start and end; DA is the transfer data consisted of 8 bits address and 2 bits data; the CK is the sync clock signal. When the CE signal is at low level, the falling edge of the CK initiates serial data, and then begin the transform; when CE signal is at low level and the CK is at high level, the transfer ends. During the transferring, when the CE signal is at low level, the CK signal is no more than 8 falls.

After begin to transfer, it is effective for the sending side to produce output in sync with the CK signal fall , and the receiving side receives the serial data as valid data when the CK signal rises.

When output the serial data, set the serial data output to high impedance after 8 bits address register output, so that it can receive serial data from the output registers.

Data reception subsequently continues until the period signal becomes “L” level; data transfer ends just before the period signal rises. Therefore, the data pin must have an open-drain or tristate interface.

Note: 1. when power is turned on, some bits of the register have undefined states. To set internal circuit states, execute a dummy data transfer before performing regular data transfer.

2. times t1~t8 have the following value:

t1≥1.0μs
t2≥1.0μs
t3≥0.3μs
t4≥0.3μs
t5≥0.3μs
t6≥1.0μs
t7≥1.0μs
t8≥0.3μs

3. Asterisks represent numbers taken from addresses, as in D*H.

Crystal oscillator pins (XIN, XOUT)

As fig.2 shows, connect two capacitors at the XIN, XOUT pin, and connect a crystal oscillator between two capacitors to generate the clock necessary for internal operation. The oscillate frequency of 3.6MHz, 4.5MHz, 7.2MHz or 10.8MHz can be selected through the OSC1 and OSC2 bit.

OSC1	OSC2	OSCILLATOR FREQUENCY
0	0	3.6MHz
1	0	4.5MHz
0	1	7.2MHz
1	1	10.8MHz

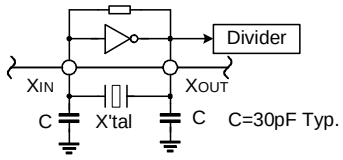


Fig.2

Note: set to 3.6MHz (OSC1="0" and OSC2="0") when power is turned on. The crystal is not oscillating at this time because the system is in standby mode.

Reference frequency generator

The reference frequency generator consists of crystal oscillator and counter. Where the crystal oscillator frequency of 3.6MHZ, 7.2MHZ or 10.8MHZ can be selected, and can generate 15 reference frequencies at most.

Set the reference frequency through the internal registers R0~R3.

R0	R1	R2	R3	REFERENCE FREQUENCY	R0	R1	R2	R3	REFERENCE FREQUENCY
0	0	0	0	0.5 KHz	0	0	0	1	*7.8125 KHz
1	0	0	0	1 KHz	1	0	0	1	9 KHz
0	1	0	0	2.5 KHz	0	1	0	1	10 KHz
1	1	0	0	3 KHz	1	1	0	1	12.5 KHz
0	0	1	0	3.125 KHz	0	0	1	1	25 KHz
1	0	1	0	*3.90654 KHz	1	0	1	1	50 KHz
0	1	1	0	5 KHz	0	1	1	1	100 KHz
1	1	1	0	6.25 KHz	1	1	1	1	Standby mode (*1)

Note:

1. At the 15 reference frequencies marked with an asterisk "*"can only be generated with a 4.5MHZ crystal oscillator, other crystal oscillator only can generate 13 reference frequencies.
2. Standby mode

   Standby mode occurs when bits R0,R1,R2,and R3 are all set to "1".In standby mode, the programmable counter stops, and FM, AM and IFIN are set to "amp off" state, and the PD pin output high impedance, This saves current consumption when the radio is turned off.

   During standby mode, the I/O ports (I/O-5~I/O-9) and output ports (OT1~OT4) can be controlled and the crystal oscillator can be turned on and off.
3. The system is set to standby mode when power is turned on. At this time, the crystal oscillator is not oscillating and the I/O ports are set to input mode.

Programmable counter

The programmable counter section consists of a 1/2 prescaler, a 2 modulus prescalers and a 4bit +12bit programmable binary counter.

1. Setting programmable counter

   The programmable counter consists of 16 bits of divisor data and 2 bits select data(FM, MODE).

(1) Setting dividing mode

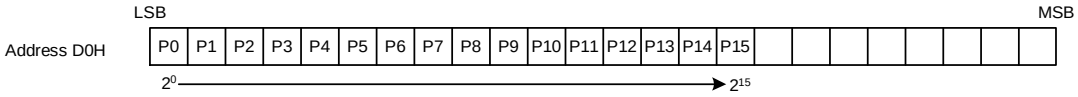
the dividing mode have 4 mode can be selected, the FM and MODE bits are used to set the divide mode:.

MODE	FM	MODE	DIVIDING MODE	TYPICAL RECEIVING BAND	INPUT FREQUENCY RANGE	INPUT PIN	FREQUENCY
LF	0	0	Direct dividing mode	LW,MW,SWL	0.5 ~ 20MHz	AM_{IN}	n
HF	0	1	Pulse swallow mode	SWH	1 ~ 40MHz		
FM_L	1	0		FM	30 ~ 130MHz 30 ~ 150MHz	FM_{IN}	
FM_H	1	1	1/2 + pulse swallow mode	FM	30 ~ 130MHz		2n

(2) Setting divisor

The divisor for the programmable counter is set as binary data in bits P0~P15.

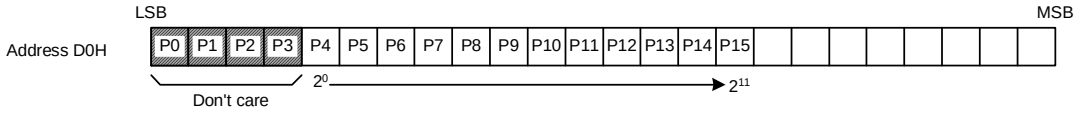
- Pulse swallow mode (16 bits)



Divisor setting range (pulse swallow mode):n=210H~FFFH (528~65535)

(Note) In the 1/2+pulse swallow mode, the actual divisor is 2*n.

- Direct dividing mode (12 bits)



In this dividing mode, P4~P15 are available, p4 is the LSB, and data P0~P3 don't care.

Divisor setting range (direct dividing mode):n=10H~FFFH(16~4095)

2. Prescaler and programmable counter circuit configuration

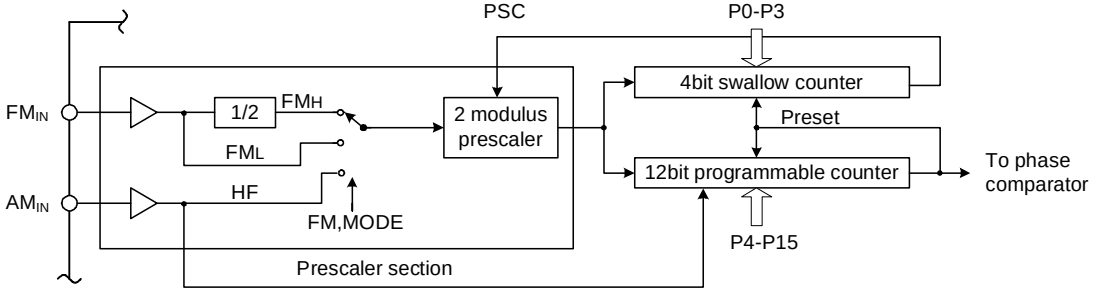


Fig.3

In the above figure: in FMH mode, the FM signal goes through high speed 1/2 divider, then enters the 2 modulus prescaler, 4 bits swallow counter and 12 bits programmable counter; in the FML and HF mode, FM and Am signal enter the 2 modulus prescaler, 4 bits swallow counter and 12 bits programmable counter directly; in the HL mode, AM signal enter the 12 bits programmable counter. Whatever selecting which mode, after divided, all the signal enter phase comparator.

FM and AM signal is coupling through the external capacitor, and amplify it by internal amplifier, so FM and AM only need low amplitude input.

IF counter

SC9257 built-in 20 bits IF counter. It is used for counting AM/FM IF frequency and measure cycle for some low frequency signal.

1. IF counter control bits

(1) *Bits G0 and G1 … Used for selecting the IF counter gate time.*

G0	G1	GATE TIME	CYCLE MEASUREMENT PULSE
0	0	1ms	50 KHz
1	0	4ms	150 KHz
0	1	16ms	900 KHz
1	1	64ms	Crystal oscillator frequency

(2) Bits SC,IF1 and IF2 …I/O port and IF counter switching bits.

(*) The functions of the following pins are switched by data.

SC	I/O-7/SC_{IN}
1	SC_{IN}
0	I/O-7

IF1	I/O-8/IF_{IN1}
1	SC_{IN}
0	I/O-8

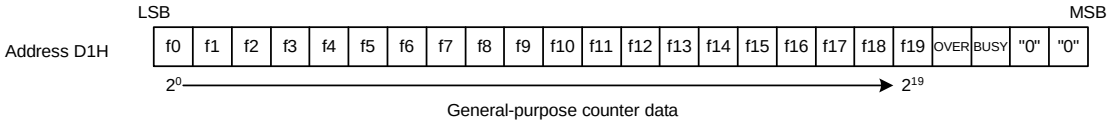
IF2	I/O-9/IF_{IN2}
1	IF_{IN2}
0	I/O-9

(3) when the bits SC, IF1 and IF2 are all set to 1, bit M7, M8 and M9 … M7 sets the state for pin I/O-7/SCIN, M8 sets the state for pin I/O-8/IFIN1; M9, for pin I/O-9/IFIN2.

M7	M8	M9	PIN STATES (When bits sc, IF1 and IF2 are all set to "1")		
			SC_{IN}	IF_{IN1}	IF_{IN2}
0	0	0	INPUT disabled	INPUT pulled down	INPUT pulled down
(*)	(*)	1			INPUT enabled
(*)	1	0		INPUT enabled	INPUT pulled down
1	0	0	INPUT enabled	INPUT pulled down	

Note: Bits marked with an asterisk "(*)" are don't care

(4) *Bits f0~f19…The IF counter results can be read in binary from bits f0~f9 of the output register (D1H).*



(5) *OVER and BUSY bits…Detect the operating state of the IF counter.*

	BIT DATA = "1"	BIT DATA = "0"
Busy	IF counter busy	IF counter ended counting
Over	Counted value in IF counter= 2^{20} (Overflow state)	Counted value in IF counter= 2^{20} -1

Note: When using the IF counter, before referring to the contents of the IF counter result bit (f0~f9), confirm that the busy bit is "0" and the OVER bit is "0".

(6) *START bit…used for reset the IF counter*

START = 0: reset unavailable

START = 1: reset available, IF counter begin to counting.

2. IF counter circuit configuration

The general-purpose counter section consists of input amps, a gate time controls circuit and a 20 bit binary counter.

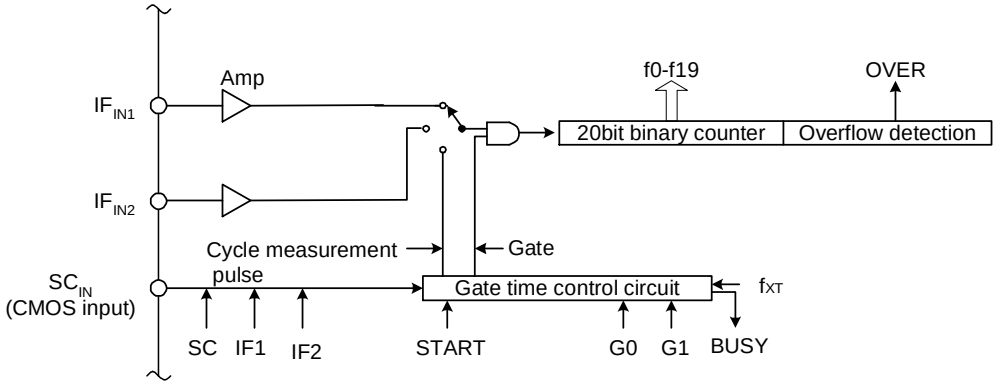
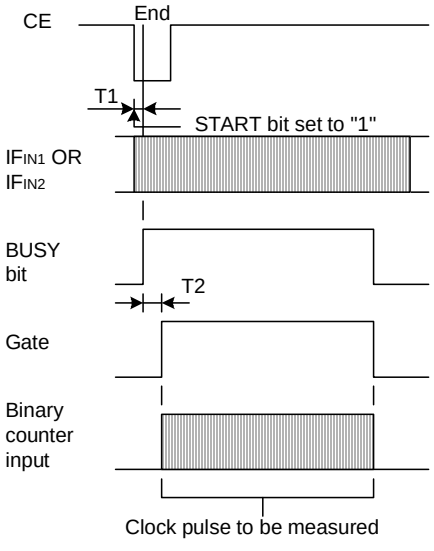


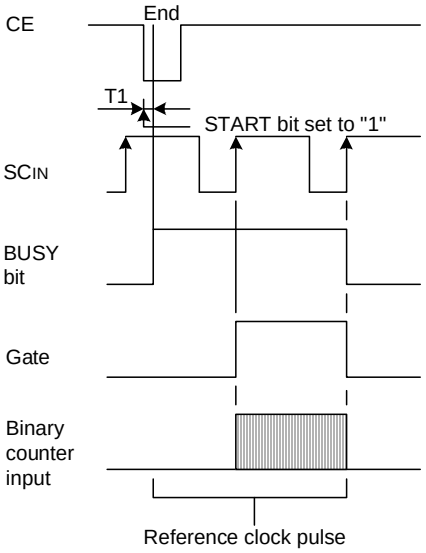
Fig.4

3. General-purpose counter measurement timing



Frequency measurement timing chart

0<T1≤0.25(μs), 0<T2 ≤1 (ms)



Cycle measurement timing chart

Note: 1. IFIN1 and IFIN2 input have built-in amps. Data are input by capacitor coupling. FMIN and AMIN operate at low amplitude.

2. SCIN is configured for CMOS input, so input signals should be logic level.

General-purpose I/O ports

The output port and I/O port are controlled and set by the input register.

Input/output form	port	Input/output configuration
Output port	Dedicated: 4 ports	N channel open-drain output
I/O ports	Dedicated: 1 port, Maximum: 5 ports	CMOS input/output

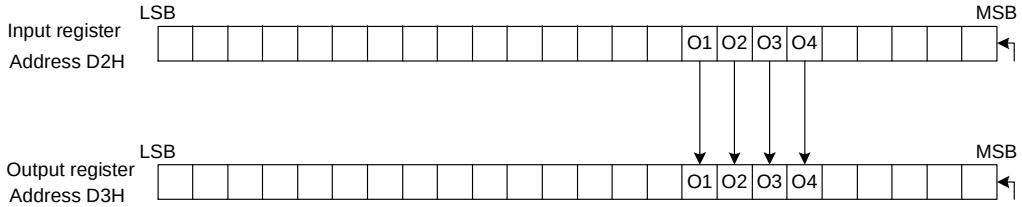
1. General-purpose output ports (OT-1~OT-4)

Pins OT-1~OT-4 are N-channel open-drain output ports, used to control signal output. They have an off withstanding voltage of 12V. The output data of OT1~OT4 depend on the corresponding registers O1~O4 (see table 1). The data in bits O1~O4 also can be read from the DA pin as output register serial data O1~O4.

(1) *O1~O4 control the output state of OT1~OT4 pins*

O1~O4	PIN OUTPUT STATE
	OT-1~OT-4
0	High impedance (N channel open drain output =off)
1	"L" level (N channel open drain output =on)

(2) The data set in bits O1~O4 of the input register can read as serial data O1~O4 from the output register.



2. General-purpose I/O ports (I/O-5~I/O-9)

Pins I/O-5~ I/O-9 are general-purpose I/O ports used for control signal input and output. They are configured for CMOS input and output.

I/O5~ I/O9 are set by C5, C6 and M7~M9 of the input register:

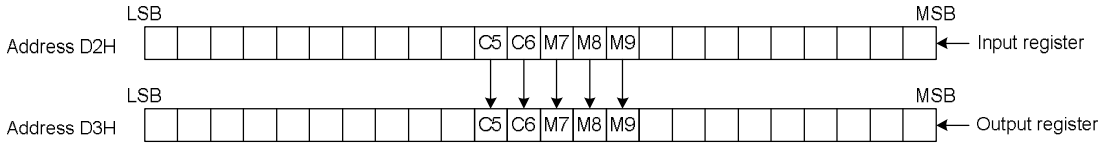
When the bits C5, C6 and M7~M9 are “0”, set these ports for input; the data in these port can latch at the output register, and as serial data read I5~I9 from DA pin.

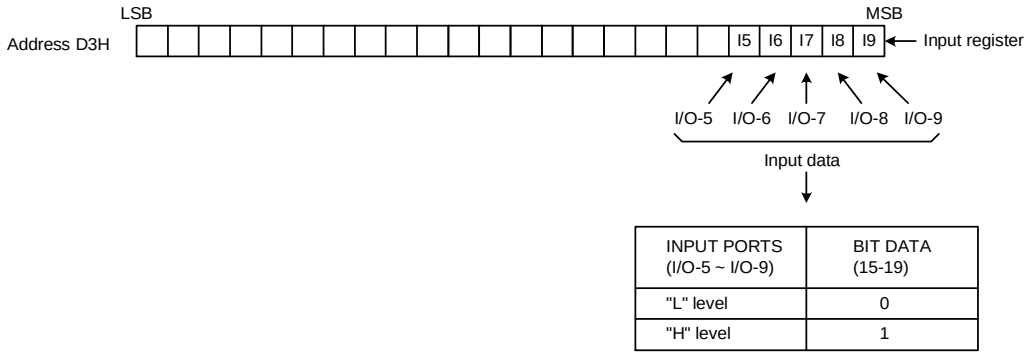
When the bits C5, C6 and M7~M9 are “1”, set these ports for output; the data at input register O5~O9 through pin I/O-5~I/O9 output in parallel. If O5~O9 is “0”, the I/O5~I/O9 output low level in parallel; if O5~O9 is “1”, the I/O5~I/O9 output high level in parallel.

In the SC9257, pin I/O7~I/O9 also as IF counter input pins, pin I/O5 as CLK pin, so when bits SC, IF1, IF2 and CLK are all set to “0”, above operation are valid.

Besides, bits C5, C6 and M7~M9 of the input register can be read as serial data C5, C6 and M7~M9 from the output register.

Data which are input in parallel from pins I/O –5~I/O-9 can be read as serial data I5~I9 from the output register (D3H)





INPUT PORTS (I/O-5 ~ I/O-9)	BIT DATA (15-19)
"L" level	0
"H" level	1

Note: 1. When pins I/O-5~I/O-9 are used for output, the data in I5~I9 of the output register(D3H) are undefined..

2.When power is turned on, input register (D2H) I/O port controls bits C5, C6 and M7~M9 and output data bits O5~O9 are set to “0”. General-purpose I/O ports are set as input ports. Pins which are used both as general-purpose I/O ports and for general-purpose counter input set for I/O port input. The output state of general-purpose output ports is set to high impedance (N channel open drain output =off).

Phase comparator

The phase comparator is used for comparing the phase difference of the reference frequency signal and dividing output signal. The frequencies and phase differences of these two signals are then equalized by passing them through low-pass filters. The filter constants can be customized for FM and AM bands since the signals are output in parallel from the phase comparator then pass through the two tristate buffer pins, PD1 and PD2.

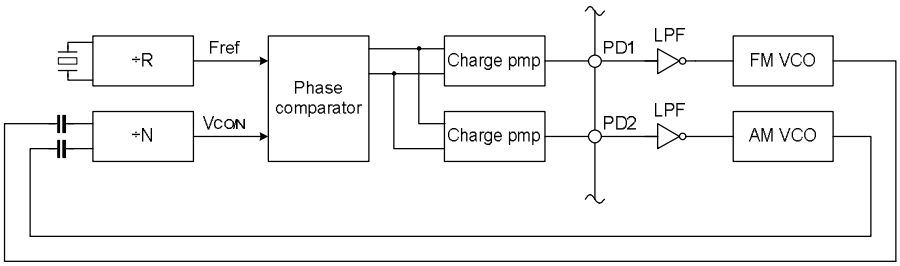
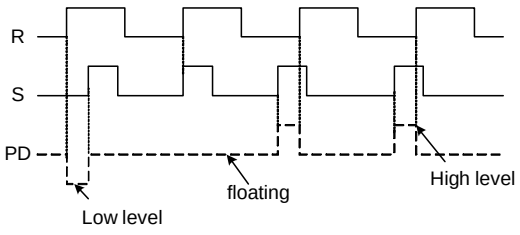
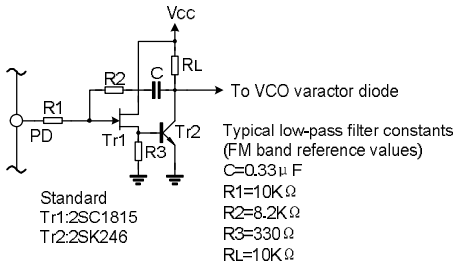


Fig.5



PD Output Timing Chart

Fig.6



Typical Active Low-Pass Filter Circuit

Fig.7

The figures above show the PD output timing chart and a typical active low-pass filter circuit featuring a Darlington connection between the FET and transistor.

The filter circuit shown above is just one example. Actual circuits should be designed based on the band composition and the properties desired from the system.

Lock detection bits

The lock detection bits detect locked states in the PLL system. These systems also have phase error detection bits (bits PE1~PE3), which are capable of more precise detection (±0.55μs~±7.15μs).

1. Unlock detection bit (UNLOCK)

This bit detects, using the reference frequency cycle, the phase difference between the reference frequency and the divided output of the programmable counter. When there is no lock, that is, when the reference frequency and the divided output of the programmable counter are not the same, unlock F/F is set.

Unlock F/F is reset every time the input register (D2H) unlock reset bit (RESET) is set to “1”. After unlock F/F has been reset in this way, locked state can detected by checking the unlock detection bit (UNLOCK) of the output register (D3H). After unlock F/F has been reset, the unlock detection bit must be checked after a time interval exceeding that of the reference frequency cycle has elapsed. This is because the reference frequency cycle inputs the lock detection strobe to unlock F/F. If the time interval is short, the correct locked state cannot be detected. Therefore, the output register (D3H) has a lock enable bit (ENABLE). This bit is reset every time the input register (D2H) reset bit is set to “1”, and set to “1” through the lock detection timing. That is, the locked state is correctly detected when the lock enable bit (ENABLE) is “1”.

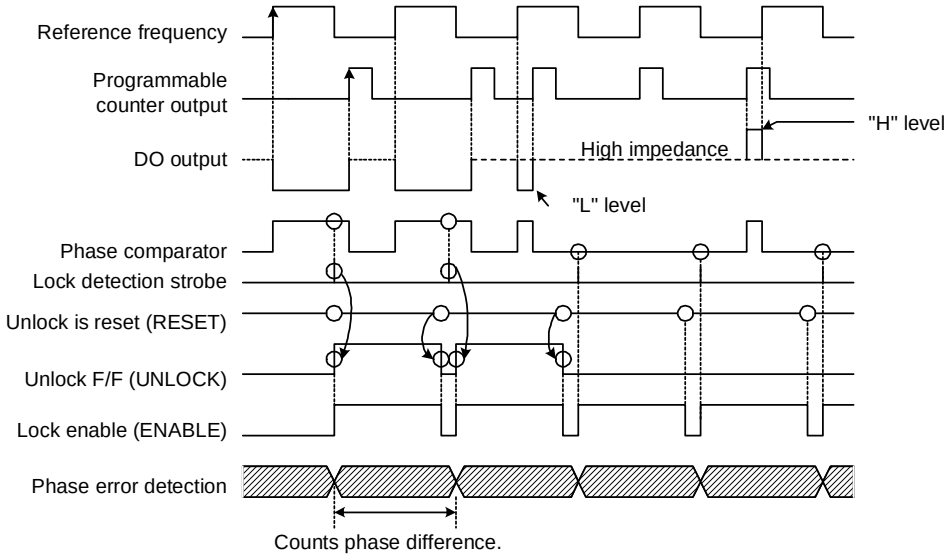
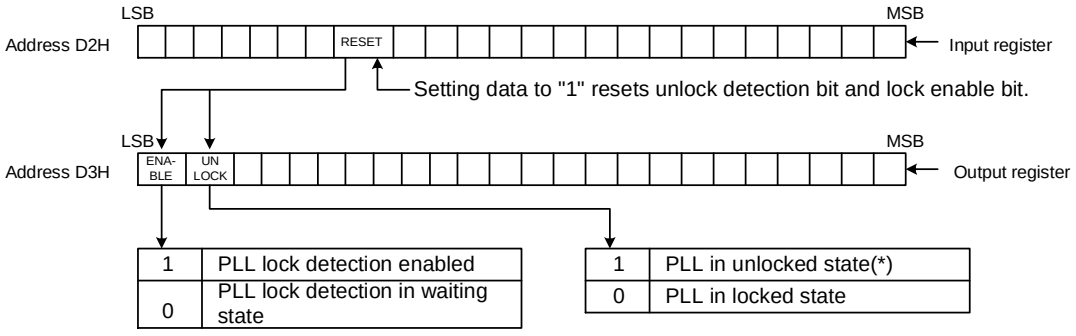


Fig.8



Note: The asterisk (*) indicates an error state of over 180° phase difference relative to the reference frequency

2. Phase error detection bits (PE1~PE3)

Phase error detection bits are the phase difference between the reference frequency and the divided output of the programmable counter. When the UNLOCK bit is set to"0", the phase error detection bits (bits PE1~PE3) are capable of precise phase error detection of ±0.55μs~±7.15μs; when the UNLOCK bit is set to"0", the phase difference relative to the reference frequency is over 180°, bits PE1~PE3 cannot correctly detect the phase error.

Phase detection bits are output through register PE1~PE3. See the following table:

PE1	PE2	PE3	PHASE ERROR (PE)
0	0	0	PE< ± 0.55μ s
0	0	1	± 0.55μ s = PE< ± 1.65μ s
0	1	0	± 1.65μ s = PE< ± 2.75μ s
0	1	1	± 2.75μ s = PE< ± 3.85μ s
1	0	0	± 3.85μ s = PE< ± 4.95μ s
1	0	1	± 4.95μ s = PE< ± 6.05μ s
1	1	0	± 6.05μ s = PE< ± 7.15μ s
1	1	1	± 7.15μ s = PE

Following is a typical lock detection operation. It shows the operation flow from locked state to frequency change with a phase error greater than ±6.05μs.

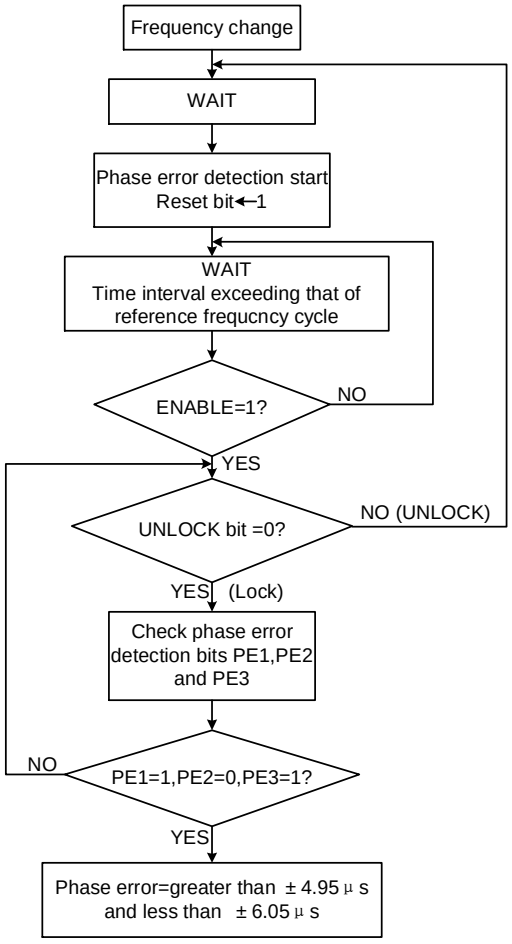


Fig.9

Other control bits

1. CLK and C5 bits which switch the function for the I/O-5/CLK pin.

(1) The CLK bit controls switching of the I/O-5/CLK pin and CLK pin.

R0~R3 Select	CLK	C5	I/O-5/ CLK PIN STATE		CRYSTAL OSCILLATOR CIRCUIT STATE
R0~R3=0	0	0	I/O port	Input port	Oscillator circuit off
	0	1		Output port	
	1	0	CLK output	System clock off (CLK at "L" level)	Oscillator circuit on
	1	1		System clock output(*)	
R0~R3?0	0	0	I/O port	Input port	Oscillator circuit on
	0	1		Output port	
	1	0	CLK output	System clock output(*)	
	1	1			

Note: The system clock output marked with an asterisk "(*)" refers to output of the crystal oscillator frequencies listed below.

Crystal oscillator (MHz)	System clock (kHz)	Duty (%)
10.8	600	50
7.2		
3.6		
4.5	750	

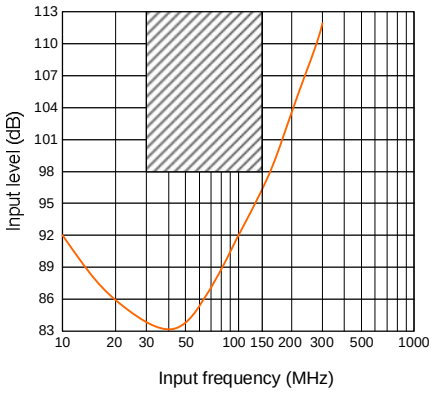
2. DOHZ bit used for control the PD2 pin output state.

0	PD2 output in normal operation (phase comparison error output)
1	PD2 output fixed at high impedance

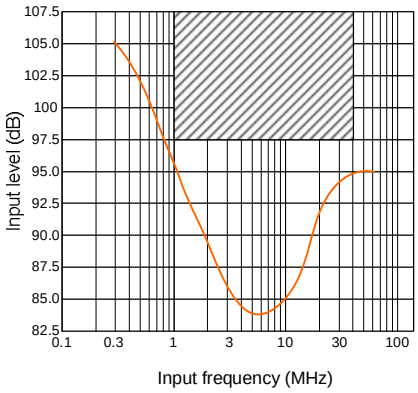
3. TEST bit… Data should normally be set to "0".

ELECTRICAL CHARACTERISTICS CURVE

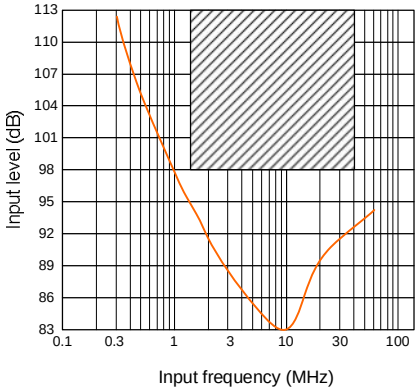
FMIN (HF) Frequency characteristics



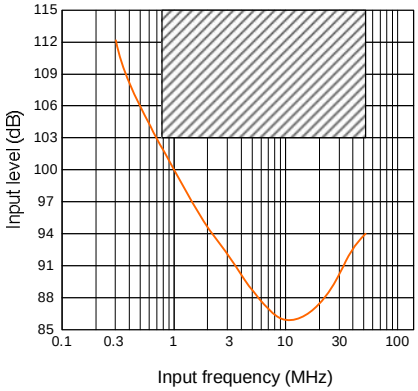
AMIN (HF) Frequency characteristics



AMIN (LF) Frequency characteristics



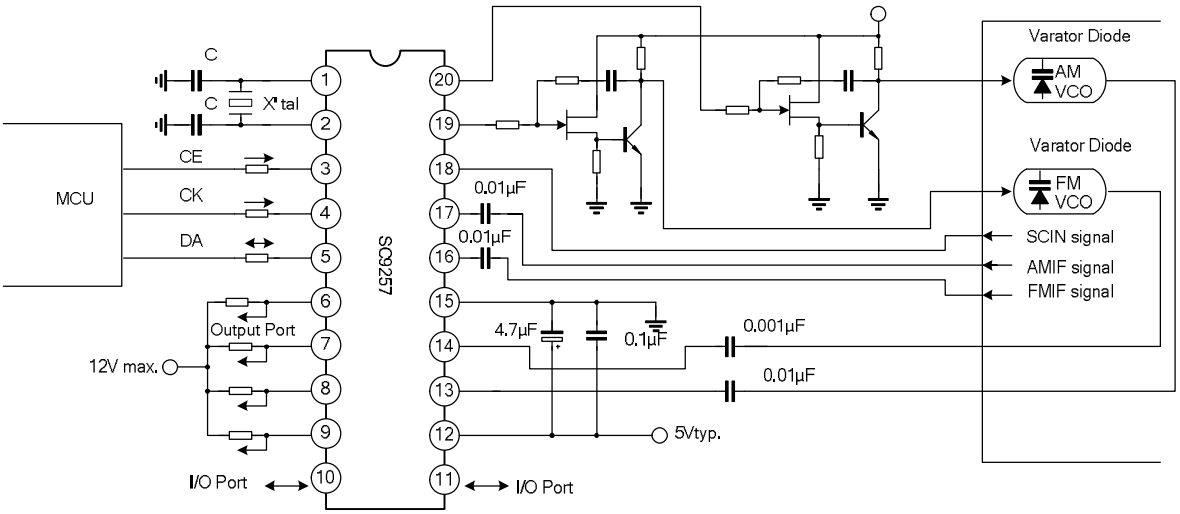
IFIN Frequency characteristics



Note: Denote the normal working area

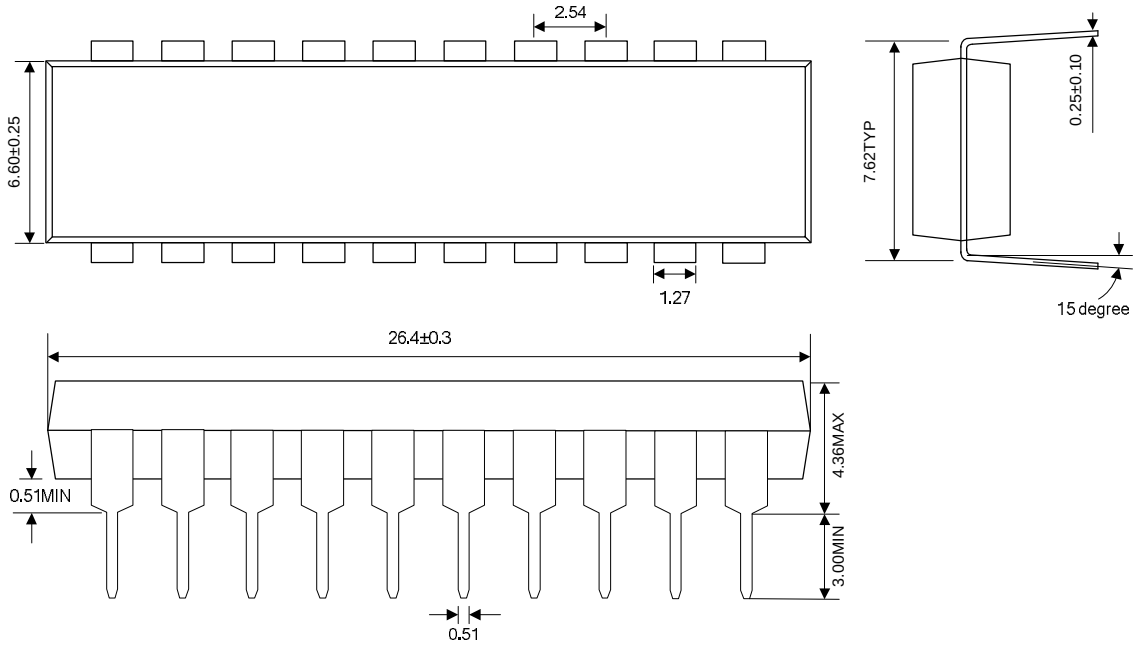
Condition: VDD=5V,Tamb=25℃

TYPICAL APPLICATION CIRCUIT

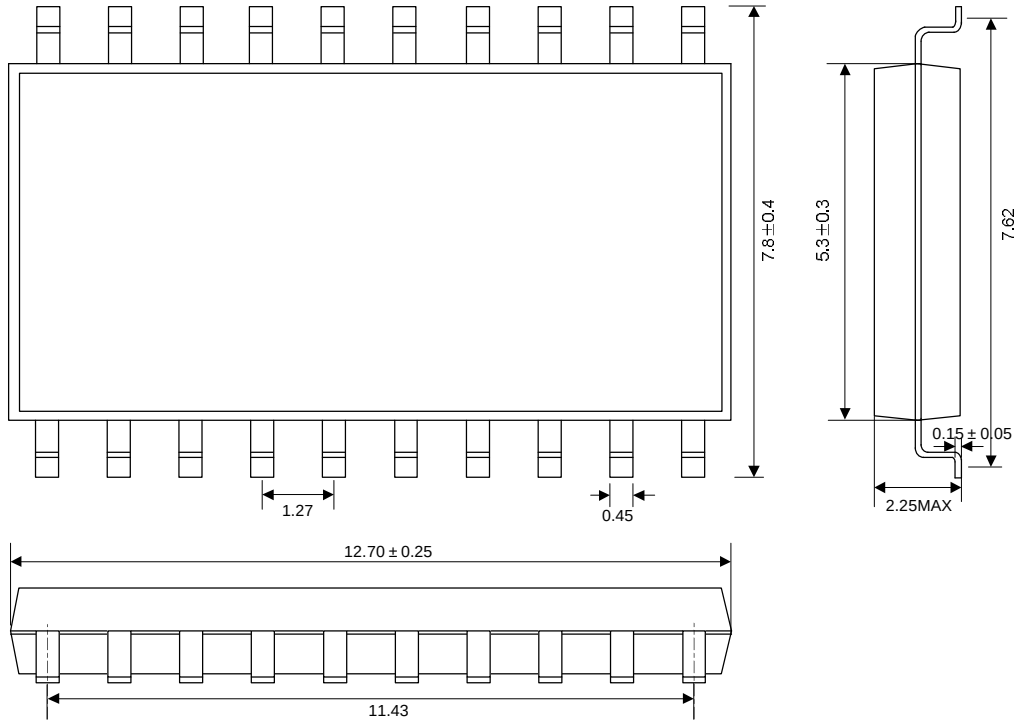


PACKAGE OUTLINE

DIP-20-300-2.54 UNIT: mm



SOP-20-300-1.27 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.

ATTACHMENT

Revision History

Data	REV	Description	Page
2004.08.03	1.0	Original	
2005.03.28	1.1	Modify the “ELECTRICAL CHARACTERISTICS”	3