

Two-Phase DC/DC Controller for CPU Core Power Supply

General Description

The RT9241A/B is a two-phase buck DC/DC controller integrated with all control functions for high performance processor VRM. The RT9241A/B drives 2 buck switching stages operating in 180 degree phase shift. The two-phase architecture provides high output current while maintaining low power dissipation on power devices and low stress on input and output capacitors. The high equivalent operating frequency also reduces the component dimension and the output voltage ripple in load transient.

RT9241A/B regulates both easily set voltage and current loops. Precise current sharing for power stage is achieved by differential input current sense and processing circuit. The settings of current sense, droop tuning and over current protection are independent to compensation circuit of voltage loop. The feature greatly facilitates the flexibility of CPU power supply design and tuning.

The RT9241A/B uses a 5-bit DAC of 1.1V to 1.85V (25mV/step) output with load current droop compensation to meet the strict VRM transient requirement. The IC monitors the V_{CORE} voltage for PGOOD and over voltage protection. Soft start, over current protection and programmable under voltage lockout are also provided to assure the safety of microprocessor and power system.

Ordering Information

RT9241A/B	□	□
	—	Package type
	S	: SOP-20
	—	Operating temperature range
	C	: Commercial standard
	—	Operating frequency version
	A	: 200KHz
	B	: 100KHz

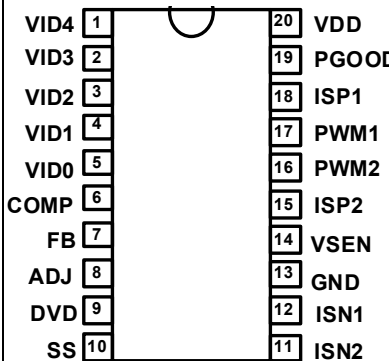
Features

- Two-Phase Power Conversion
- VRM 9.0 DAC Output with Active Droop Compensation for Fast Load Transient
- Precise Channel Current Sharing with Differential Sense Input
- Hiccup Mode Over Current Protection
- Programmable Under Voltage Lockout and Soft Start
- High Ripple Frequency, (Channel Frequency Times Channel Number)
- 100KHz Version (RT9241B) for Lower Switching Loss

Applications

- Power Supply for Server and Workstation
- Power Supply for High Current Microprocessor

Pin Configurations

Part Number	Pin Configurations
RT9241A/B CS (Plastic SOP-20)	<p style="text-align: center;">TOP VIEW</p> 

RT9241A/B

Absolute Maximum Ratings

- Supply Voltage 7V
- Input, Output or I/O Voltage GND-0.3V ~ V_{DD}+0.3V
- Power Dissipation, P_D @ T_A = 25°C
SOP-20 0.625W
- Package Thermal Resistance
SOP-20, θ_{JA} 110°C /W
- Ambient Temperature Range 0°C ~ 70°C
- Junction Temperature Range 0°C ~ 125°C
- Storage Temperature Range -40°C ~ 150°C
- Lead Temperature (Soldering, 10 sec.) 260°C

Electrical Characteristics

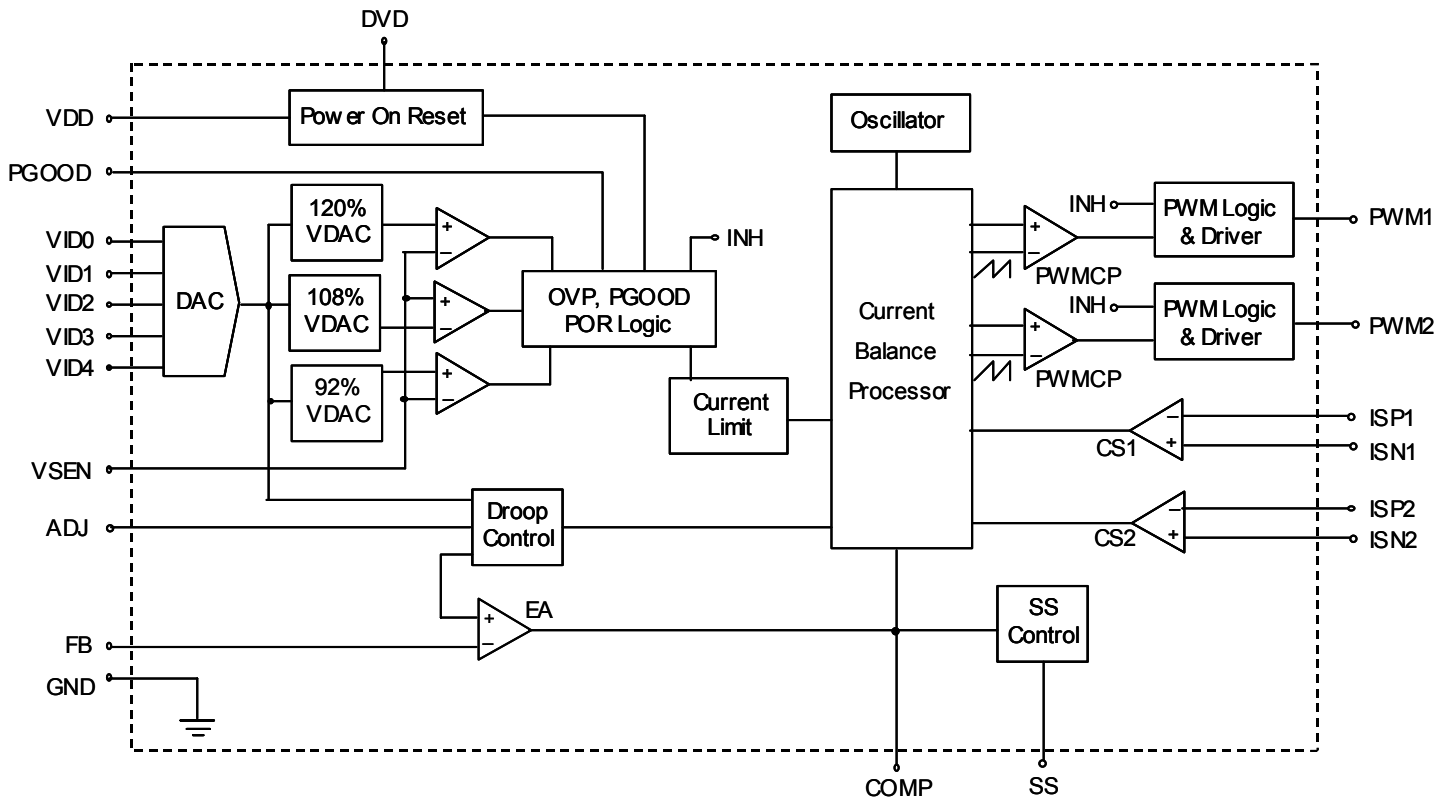
(V_{DD} = 5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
V_{DD} Supply Current						
Nominal Supply Current	I _{DD}	PWM 1,2 Open	--	4	10	mA
Power-On Reset						
V _{DD} Rising Threshold			4.2	4.35	4.6	V
V _{DD} Falling Threshold			--	3.85	--	V
Hysteresis			0.2	0.6	--	V
V _{DVD} Rising Trip Threshold			1.19	1.25	1.31	V
Oscillator						
Frequency	RT9241A	For each phase	170	200	230	kHz
	RT9241B		85	100	115	
Ramp Amplitude			--	1.7	--	V
Ramp Valley			1.0	1.3	--	V
Maximum On Time of Each Channel			70	75	80	%
Reference and DAC						
DACOUT Voltage Accuracy			-1.0	--	+1.0	%
DAC (VID0-VID4) Input Low Voltage			--	--	0.8	V
DAC (VID0-VID4) Input High Voltage			2.0	--	--	V
DAC (VID0-VID4) Bias Current			20	28	36	μA
PWM Controller Error Amplifier						
DC Gain			--	85	--	dB
Bandwidth			--	10	--	MHz
Slew Rate		C _L = 10pF	--	5	--	V/μS

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Current Sense GM Amplifier						
ISP 1,2 Full Scale Source Current			50	--	--	μA
ISP 1,2 Current for OCP			70	75	--	μA
Protection						
SS Current		$V_{SS} = 1\text{V}$	8	13	18	μA
Over-Voltage Trip (VSEN/DACOUT)			118	122	126	%
Power Good						
Upper Threshold (VSEN/DACOUT)		VSEN Rising	106	110	114	%
Lower Threshold (VSEN/DACOUT)		VSEN Rising	86	90	94	%

Function Block Diagram



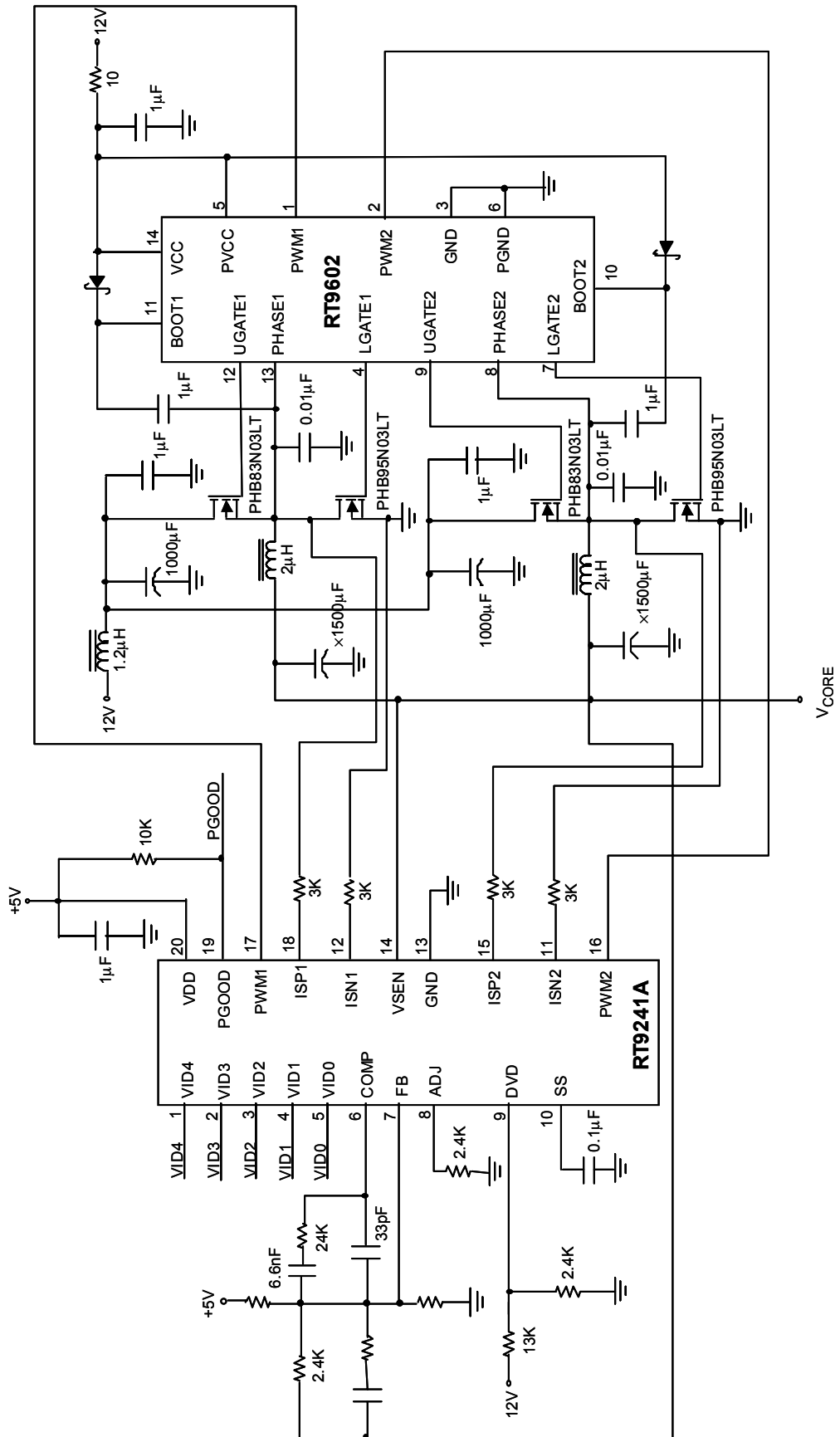
RT9241A/B

Table 1 Output Voltage Program

Pin Name					Nominal Output Voltage DACOUT
VID4	VID3	VID2	VID1	VID0	
1	1	1	1	1	Off
1	1	1	1	0	1.100V
1	1	1	0	1	1.125V
1	1	1	0	0	1.150V
1	1	0	1	1	1.175V
1	1	0	1	0	1.200V
1	1	0	0	1	1.225V
1	1	0	0	0	1.250V
1	0	1	1	1	1.275V
1	0	1	1	0	1.300V
1	0	1	0	1	1.325V
1	0	1	0	0	1.350V
1	0	0	1	1	1.375V
1	0	0	1	0	1.400V
1	0	0	0	1	1.425V
1	0	0	0	0	1.450V
0	1	1	1	1	1.475V
0	1	1	1	0	1.500V
0	1	1	0	1	1.525V
0	1	1	0	0	1.550V
0	1	0	1	1	1.575V
0	1	0	1	0	1.600V
0	1	0	0	1	1.625V
0	1	0	0	0	1.650V
0	0	1	1	1	1.675V
0	0	1	1	0	1.700V
0	0	1	0	1	1.725V
0	0	1	0	0	1.750V
0	0	0	1	1	1.775V
0	0	0	1	0	1.800V
0	0	0	0	1	1.825V
0	0	0	0	0	1.850V

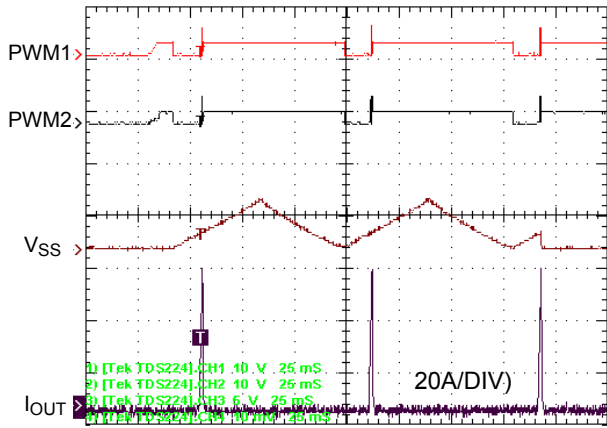
Note: (1) 0:Connected to GND (2) 1:Open

RT9241A/B



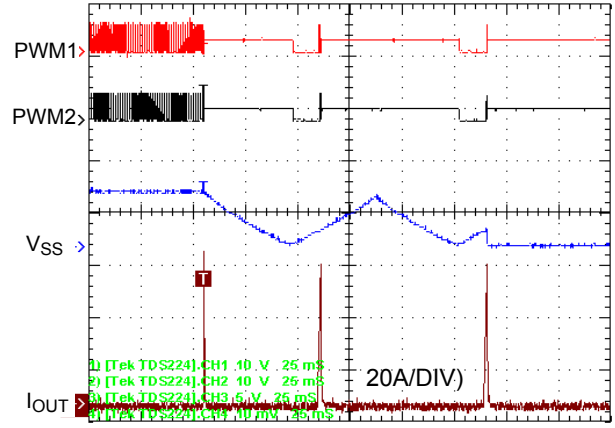
Typical Operating Characteristics

Over Current Protection at Power-Up



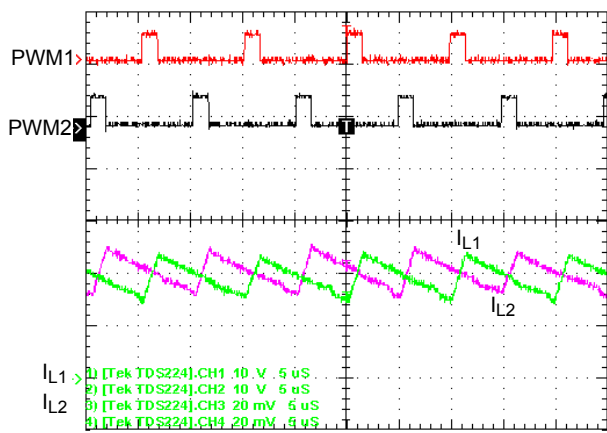
Time (25mS/DIV)

Over Current Protection at Steady State



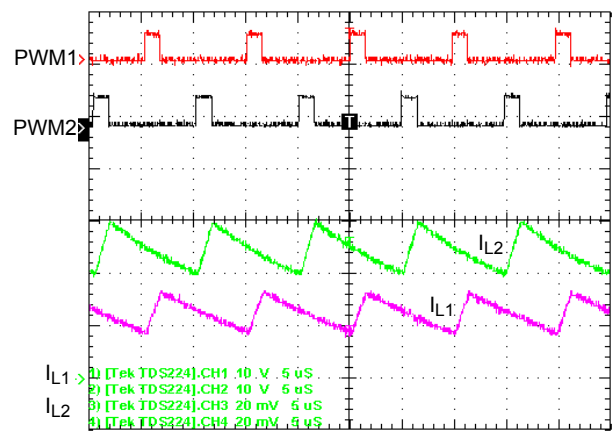
Time (25mS/DIV)

Current Sharing between Two Phases



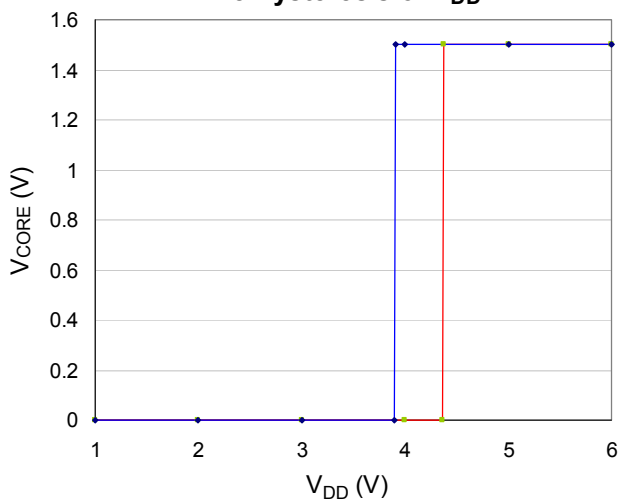
Time (5 μS/DIV)

Two-Phase Converter without Current Sharing

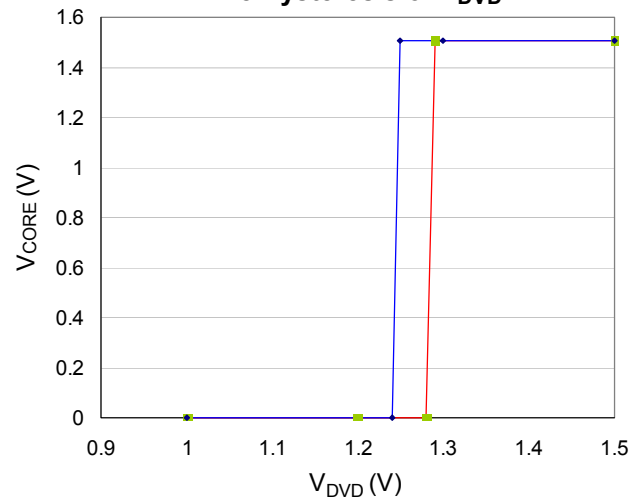


Time (5 μS/DIV)

The Hysteresis of V_{DD}



The Hysteresis of V_{DVD}



RT9241A/B

Functional Pin Description

VID4, VID3, VID2, VID1 and VID0 (Pin1,2,3,4,5)

DAC voltage identification inputs for VRM9.0. These pins are TTL-compatible and internally pulled to VDD if left open.

COMP (Pin 6)

Output of the error amplifier and input of the PWM comparator.

FB (Pin 7)

Inverting input of the internal error amplifier.

ADJ (Pin 8)

Current sense output for active droop adjust. Connect a resistor from this pin to GND to set the amount of load droop. This pin should not be opened.

DVD (Pin 9)

Programmable power UVLO detection input. Trip threshold = 1.25V at V_{DVD} rising

SS (Pin 10)

Connect this SS pin to GND with a capacitor to set the start time interval. Pull this pin below 1V(ramp valley of saw-tooth wave in pulse width modulator) to shutdown the converter output.

ISN1 (Pin 12), ISN2 (Pin 11)

Current sense inputs from the individual converter channel's sense component GND nodes.

GND (Pin 13)

Ground for the IC.

VSEN (Pin 14)

Power good and over voltage monitor input. Connect to the microprocessor-CORE voltage.

ISP1 (Pin 18), ISP2 (Pin 15)

Current sense inputs for individual converter channels. Tie this pin to the component sense node.

PWM1 (Pin 17), PWM2 (Pin 16)

PWM outputs for each driven channel. Connect these pins to the PWM input of the MOSFET driver.

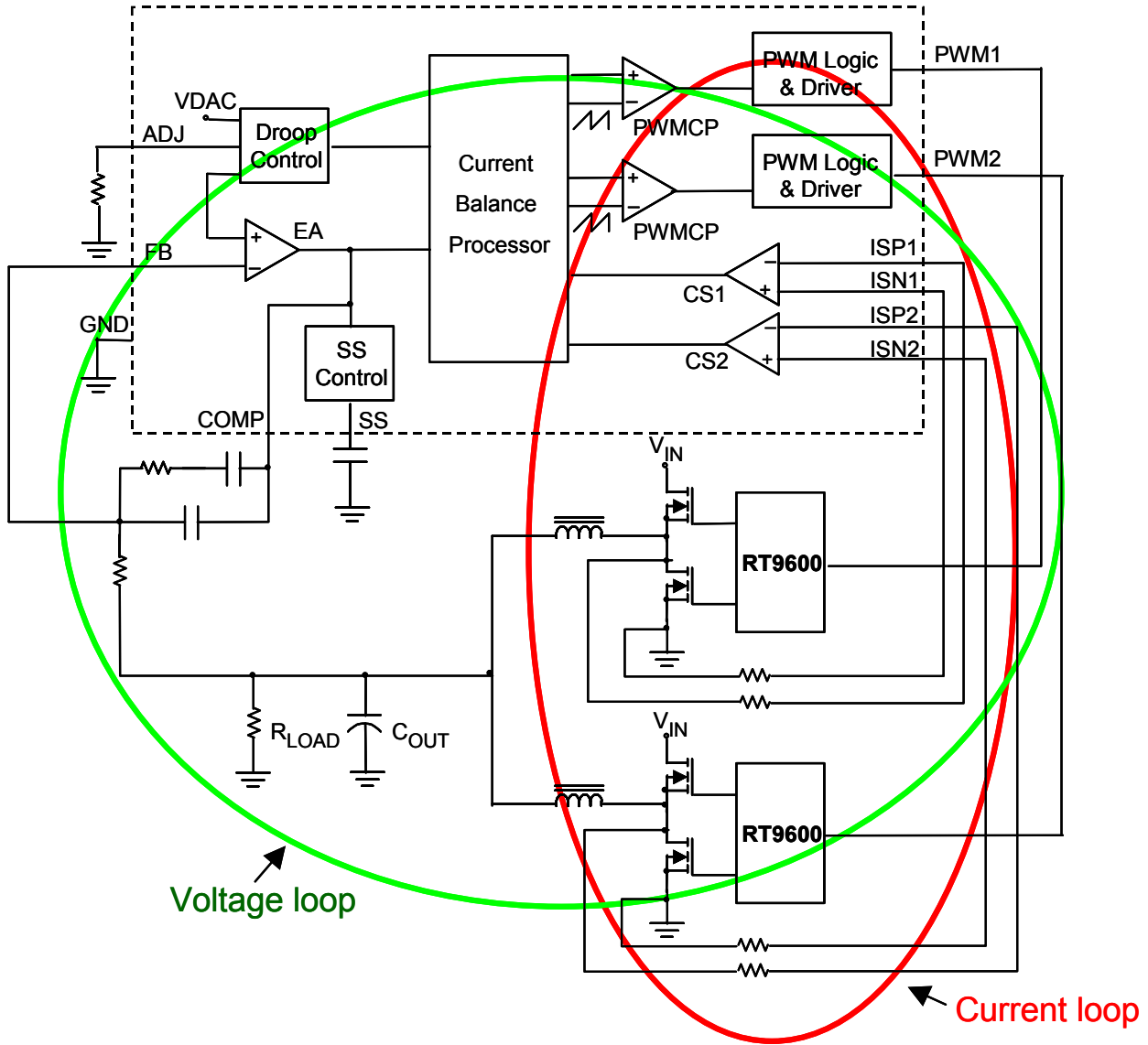
PGOOD (Pin 19)

Power good open-drain output.

VDD (Pin 20)

IC power supply. Connect this pin to a 5V supply.

Simplified Block Diagram Control Loops for a Two Phase Converter



The sensing circuit gets $I_X \frac{I_L \times R_S}{R_{SP}}$ by local feedback. $R_{SP} = R_{SN}$ to cancel the voltage drop caused by GM amplifier input bias current. I_X is sampled and held just before low side MOSFET turns off (See Fig.2). Therefore,

$$I_{X(S/H)} = \frac{I_{L(S/H)} \times R_S}{R_{SP}} \quad I_{L(S/H)} = I_{L(AVG)} + \frac{V_O}{L} \times \frac{T_{OFF}}{2}$$

$$T_{OFF} = \left(\frac{V_{IN} - V_O}{V_{IN}} \right) \times T_S, \text{ for switching period} = T_S$$

$$I_{X(S/H)} = \left[I_{L(AVG)} - \frac{V_O - \left(\frac{V_{IN} - V_O}{V_{IN}} \right) \times T_S}{2L} \right] \times \frac{R_S}{R_{SP}}$$

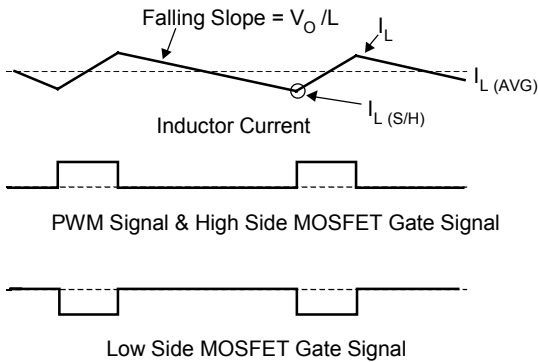


Fig. 2 Inductor Current and PWM Signal

Droop tuning

The S/H current signals from power channels are injected to ADJ pin to create droop voltage.

$$V_{ADJ} = R_{ADJ} \times \frac{2}{3} \sum I_X$$

The DAC output voltage decreases by V_{ADJ} to form the V_{CORE} load droop(see Fig.3).

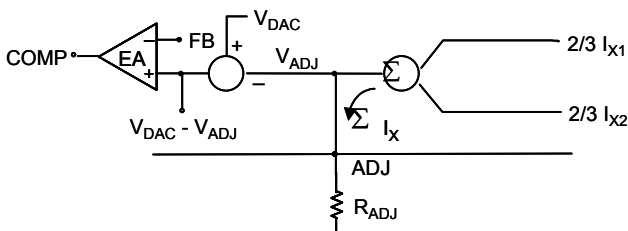


Fig. 3 Droop Tune Circuit

Protection and SS function

For OVP, the RT9241A/B detects the V_{CORE} by V_{SEN} pin. Eliminate the parasitic delay and noise influence on the PCB path for fast and accurate detection. The trip point of OVP is 120% of normal output level. The PWM outputs are pulled low to turn on the low side MOSFET and turn off the high side MOSFET of the synchronous rectifier at OVP. The OVP latch can only be reset by V_{DD} or V_{DVD} restart power on reset sequence. The PGOOD detection trip point of V_{CORE} is $\pm 8\%$ out of the normal level. The PGOOD open drain output pulls low when V_{OCRE} exceeds the range.

Soft start circuit generates a ramp voltage by charging external capacitor with 10uA current after IC POR acts. The PWM pulse width and V_{CORE} are clamped by the rising ramp to reduce the in-rush current and protect the power components.

OCP is triggered if one channel S/H current signal $I_X > 75\mu A$. Controller forces PWM output latched at high impedance to turn off both high and low side MOSFET in the power stage and initial the hiccup mode protection. The SS pin voltage is pulled low with a 10uA current after it is less than 90% V_{DD} . The converter restarts after SS pin voltage $< 0.2V$. Three times of OCP disable the converter and only release the latch by POR acts (see Fig.4).

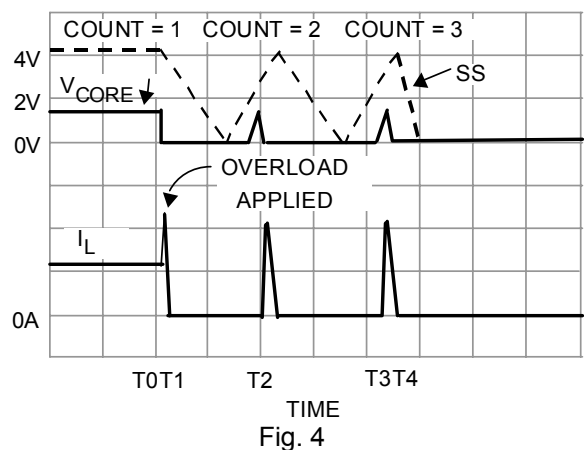
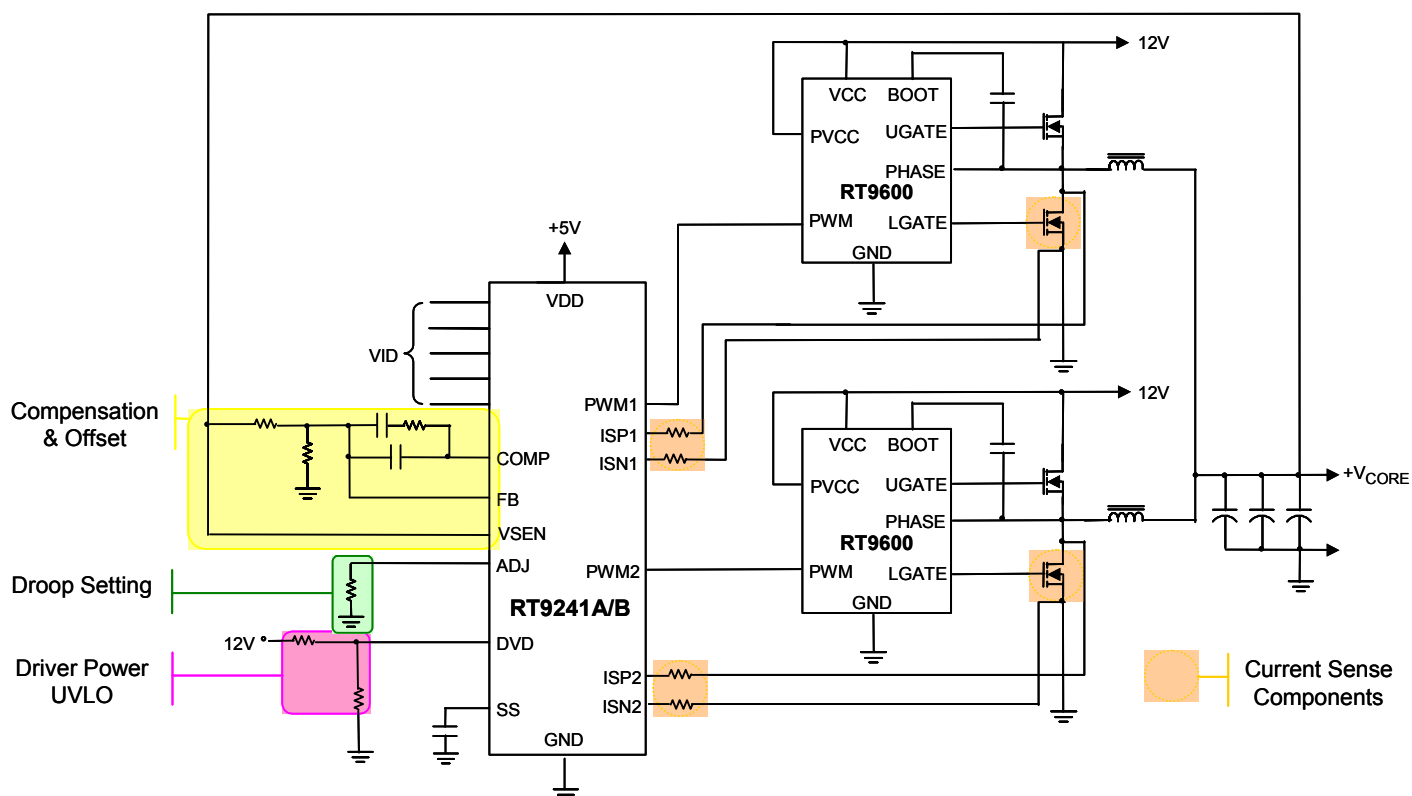


Fig. 4

RT9241A/B

Two-Phase Converter and Components Function Grouping



Design Procedure Suggestion

Voltage loop setting

- Output filter pole and zero (Inductor, output capacitor value & ESR)
- Error amplifier compensation network

Current loop setting

- Over current protection trip point setting by GM amplifier S/H current(current sense component R_{on} , ISP_x & ISN_x pin external resistor value, keep ISP_x current = $75\mu A$ at OCP condition)

VRM load line setting

- Droop amplitude (ADJ pin resistor)
- No load offset (additional resistor in compensation network)

Power sequence & SS

DVD pin external resistor and SS pin capacitor
PCB layout

- Kelvin sense for current sense GM amplifier input**
- Refer to layout guide for other item

Design Example for RT9241A

Two phase converter $V_{CORE} = 1.5V$, $V_{IN} = 12V$, full load current = 40Amp, droop voltage at full load = 120mV, OCP trip point for each power stage = 30Amp (at Sample/Hold), low side MOSFET $R_{DS(ON)} = 6m\Omega$ at room temperature, $L = 2\mu H$, $C_{OUT} = 9000\mu F$, capacitor ESR = 2m Ω .

1. Compensation setting

a. Modulator Gain, Pole and Zero

$$\text{Modulator Gain} = \frac{V_{IN}}{V_{RAMP}}$$

saw-tooth wave amplitude $V_{RAMP} = 1.7V$,

modulator Gain = 8.6 = 18.7dB

$$\text{LC filter pole} = \frac{1}{2\pi\sqrt{LC}} = 1.2\text{kHz}$$

$$\text{ESR zero} = \frac{1}{2}\pi C R_{ESR} = 8.8\text{kHz}$$

b. EA compensation network

Use type 2 compensation scheme (see Fig. 5),

$$f_Z = \frac{1}{2\pi R_2 C_1} \quad f_P = \frac{1}{2\pi R_2 \left(\frac{C_1 \times C_2}{C_1 + C_2} \right)}$$

mid-band gain = $\frac{R_2}{R_1}$. Choose $R_1 = 2.4K\Omega$,

$R_2 = 24K\Omega$, $C_1 = 6.6nF$, $C_2 = 33pF$, get $f_Z = 1KHz$,

$f_P = 200KHz$, mid-band Gain=10=20dB,

modulator asymptotic Bode plot of EA

compensation and PWM loop Gain Bode shown

as Fig. 6.

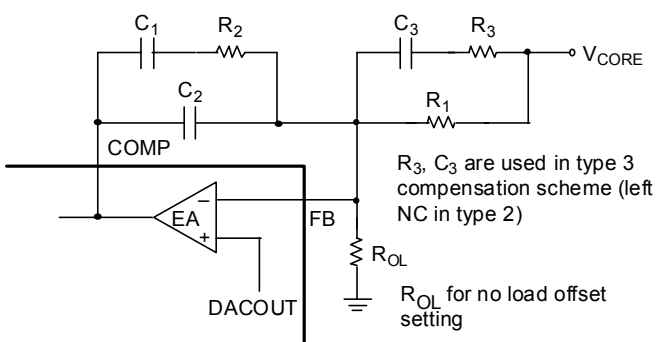


Fig. 5 EA Compensation Network

Asymptotic Bode Plot of PWM Loop Gain

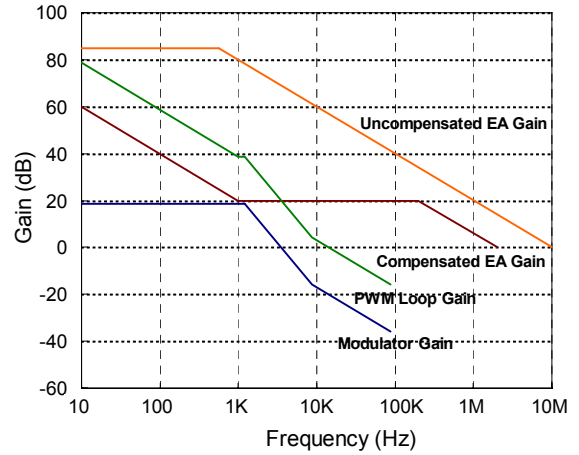


Fig. 6 Asymptotic Bode Plot of PWM Loop Gain

2. Over Current Protection setting

OCP trip point current = 30A (at Sample/Hold) ,

$$I_X = \frac{R_{DS(ON)} \times 30A}{R_{SP}} = 75\mu A \quad R_{ISP} = 2.4K\Omega$$

Take the temperature rising for consideration, if MOSFET working temperature=70°C and the temperature coefficient =5000ppm/°C, $R_{ISP}(70^\circ C) = R_{ISP}(27^\circ C) \times \{R_{DS(ON)}(70^\circ C)/R_{DS(ON)}(27^\circ C)\} = 1.75K\Omega$

3. Droop setting

Full load current of each power channel = 40A/2 = 20Amp, the ripple current = $\Delta I_L =$

$$5\mu S \times \frac{1.5V}{2\mu H} \times \left(1 - \frac{1.5V}{12V} \right) = 3.28A$$

, load current at S/H $20A - \frac{\Delta I_L}{2} = 18.36A$

$$= I_{X(MAX)} = \frac{R_{DS(ON)} \times 18.36A}{R_{ISP}}, \text{ GM Amp}$$

S/H

$R_{ISP} = R_{ISN} = 2.4K\Omega$, $I_{X(MAX)} = 46\mu A$, required Droop = 120mV = $46\mu A \times 2 \times 2/3 \times R_{ADJ}$, $R_{ADJ} = 1.97K\Omega$.

Take the temperature rising for consideration, we just modify R_{ISP} like OCP setting.

4. SS capacitor

$C_{SS} = 0.1\mu F$ is the suitable value for most application.

RT9241A/B

Layout Guide

Layout Guide

Place the high-power switching components first, and separate them from sensitive nodes.

1. Most critical path: the current sense circuit is the most sensitive part of the converter. The current sense resistors tied to ISP1,2 and ISN1,2, should be located not more than 0.5 inch from the IC and away from the noise switching nodes. The PCB trace of sense nodes should be parallel and as short as possible. Kelvin connection of the sense component (additional sense resistor or MOSFET $R_{DS(ON)}$) ensures the accurate stable current sensing.

No Kelvin sense, no guarantee for stable operation!

Switching ripple current path:

- a. Input capacitor to high side MOSFET
 - b. Low side MOSFET to output capacitor
 - c. The return path of input and output capacitor
 - d. Separate the power and signal GND
 - e. The switching nodes(the connection node of high/low side MOSFET and inductor) is the most noisy points. Keep them away from sensitive small-signal node.
 - f. Reduce parasitic R, L by minimum length, enough copper thickness and avoiding of via.
2. MOSFET driver should be close to MOSFET
- 4.The compensation, bypass and other function setting components should be near the IC and away from the noisy power path.

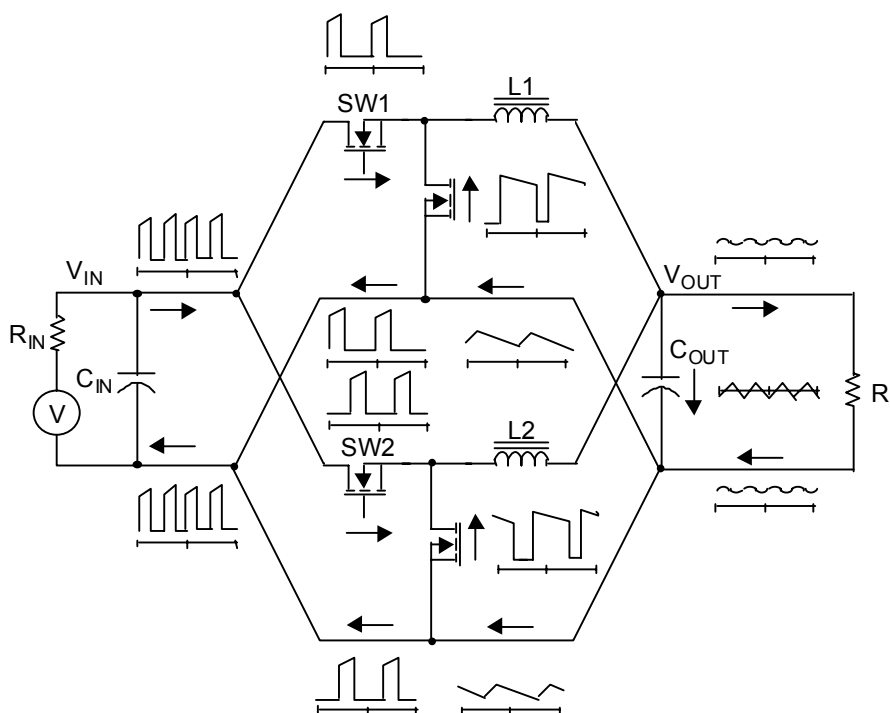


Fig.7 Power Stage Ripple Current Path

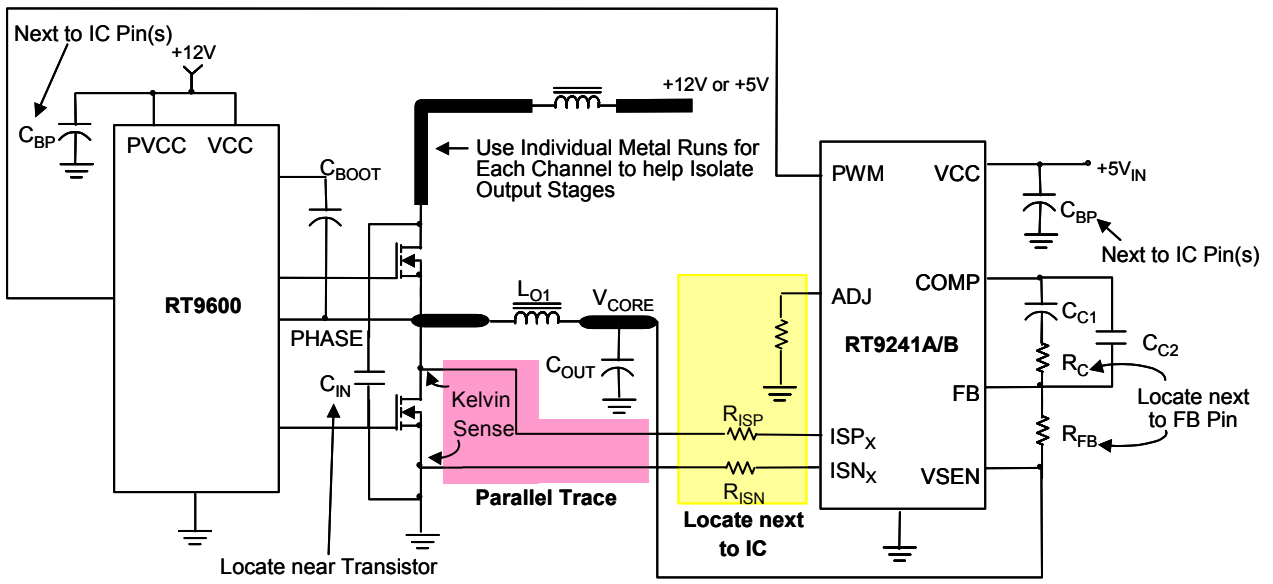
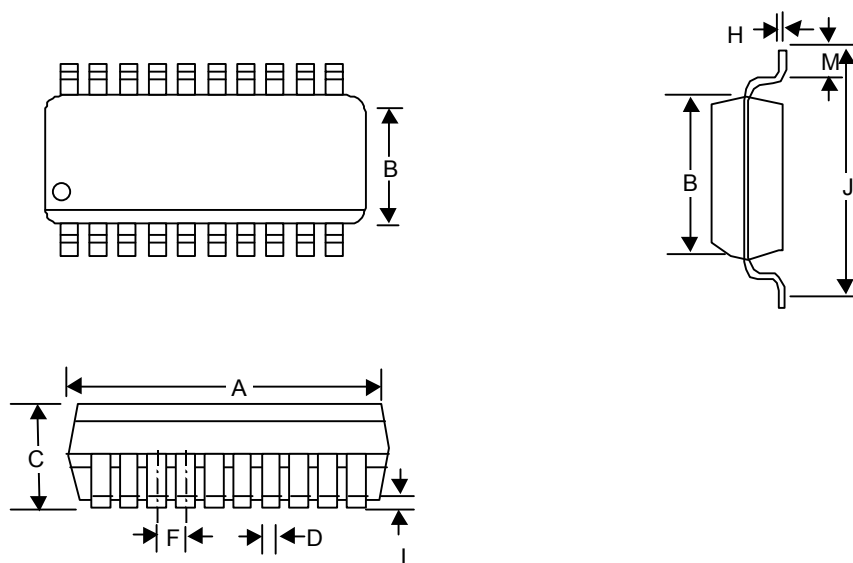


Fig.8 Layout Consideration

RT9241A/B

Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	12.598	13.005	0.496	0.512
B	7.391	7.595	0.291	0.299
C	2.362	2.642	0.093	0.104
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.229	0.330	0.009	0.013
I	0.102	0.305	0.004	0.012
J	10.008	10.643	0.394	0.419
M	0.381	1.270	0.015	0.050

20-Lead SOP Plastic Package

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