

SANYO	No.3245A	LA5317M
		Monolithic Linear IC Variable Divided Voltage Generator for LCD Use

Overview

The LA5317M is a variable divided voltage generator IC for multiple drive of LCD matrix.

Features

- Power supply for variable bias LCD drive (1/5 to 1/20 bias available by on-chip resistances)
- 5 OP amps to deliver 5 voltage outputs
- Low current dissipation (1.6mA typ)
- Miniflat package

Maximum Ratings at Ta = 25°C

			unit
Maximum Supply Voltage	$V_{EE\ max}$	$V_{CC-V_{EE}}$	-38 to 0 V
Maximum Output Current	$I_{OUT\ max}$	$V_1\ to\ V_5$	*±25 mA
Allowable Power Dissipation	$P_d\ max$		800 mW
Operating Temperature	T_{opr}		-20 to +75 °C
Storage Temperature	T_{stg}		-30 to +125 °C

Note 1) Continuous operation (nonbreakdown) is guaranteed when operated at the maximum ratings shown above.

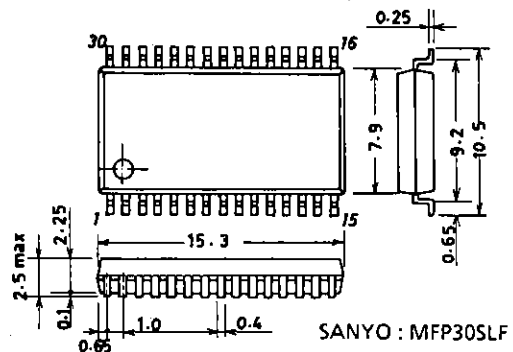
Note 2)* The maximum output current is a value specified under the conditions otherwise specified separately.

Operating Conditions at Ta = 25°C

			unit
Supply Voltage	V_{EE}	$V_{CC-V_{EE}}$	-35 to -10 V
Output Current	I_{OUT1}	V_1	-0.5 to +10 mA
	$I_{OUT2,3}$	V_2, V_3	-10 to +10 mA
	$I_{OUT4,5}$	V_4, V_5	-15 to +0.5 mA

Note 3) Set V_{CC}, V_{EE} so that $|V_1|, |V_5-V_4|$ become 1V or greater.

Package Dimensions 3073A-M30IC
(unit: mm)

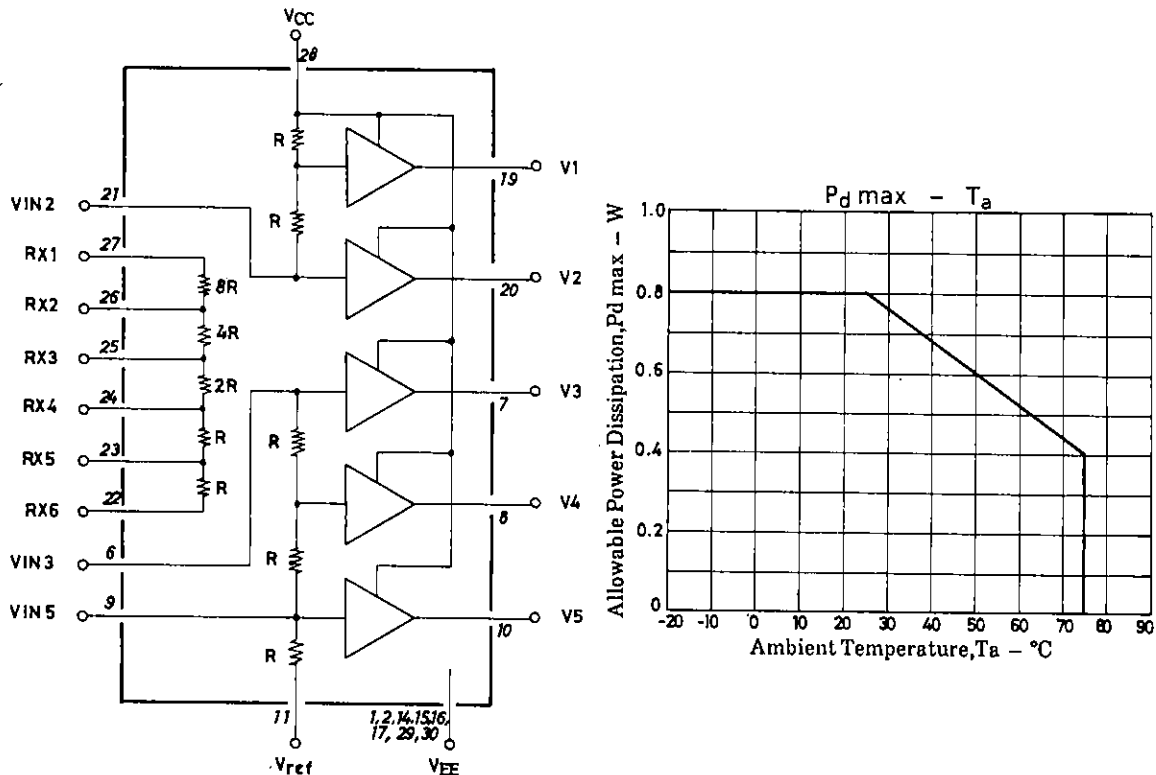


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Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} - V_{EE} = 20\text{V}$, $V_{REF} = V_{EE}$, $R_X = 8R$

			min	typ	max	unit
Current Dissipation	I_{CC}, I_{EE}	$V_{CC}, V_{EE} : V_{CC} - V_{EE} = 20\text{V}$, $R_X = 8R$		1.6	3	mA
Output Voltage Ratio	1	Ra1	V_2/V_1	1.96	2.00	2.04
	2	Ra2	$(V_5 - V_3)/(V_5 - V_4)$	1.96	2.00	2.04
	3	Rb1	V_5/V_1	11.64	12.00	12.36
	4	Rb2	V_5/V_2	5.82	6.00	6.18
	5	Rb3	$V_5/(V_5 - V_3)$	5.82	6.00	6.18
	6	Rb4	$V_5/(V_5 - V_4)$	11.64	12.00	12.36
Internal Resistance Ratio	1	8R	$R_{X1} - R_{X2}$		8	
	2	12R	$R_{X1} - R_{X3}$	Resistance ratio referenced to R across R_{X5} and R_{X6}	12	
	3	14R	$R_{X1} - R_{X4}$		14	
	4	15R	$R_{X1} - R_{X5}$		15	
	5	16R	$R_{X1} - R_{X6}$		16	
Resistance	R	R value when 0.5V is applied across R_{X5} and R_{X6} .			20	
Load Regulation	1	ΔV_1	$V_1 : -0.2\text{mA} < I_{OUT1} < +10.0\text{mA}$		± 20	mV
	2	ΔV_2	$V_2 : -0.2\text{mA} < I_{OUT2} < +10.0\text{mA}$		± 20	mV
	3	ΔV_3	$V_3 : -0.2\text{mA} < I_{OUT3} < +10.0\text{mA}$		± 20	mV
	-2	$-\Delta V_2$	$V_2 : -10.0\text{mA} < I_{OUT2} < +0.2\text{mA}$		± 20	mV
	-3	$-\Delta V_3$	$V_3 : -10.0\text{mA} < I_{OUT3} < +0.2\text{mA}$		± 20	mV
	-4	$-\Delta V_4$	$V_4 : -10.0\text{mA} < I_{OUT4} < +0.2\text{mA}$		± 20	mV
	-5	$-\Delta V_5$	$V_5 : -10.0\text{mA} < I_{OUT5} < +0.2\text{mA}$		± 20	mV

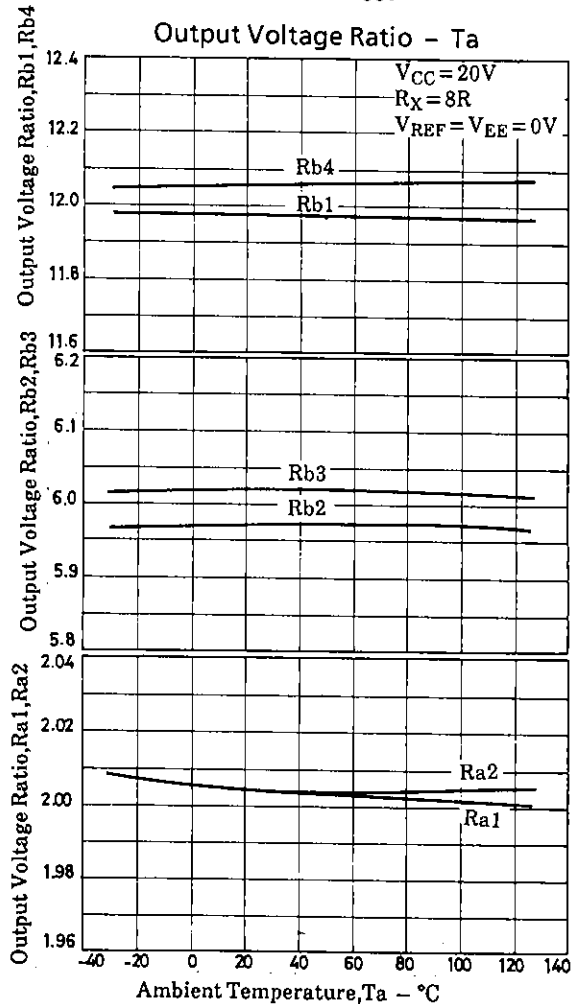
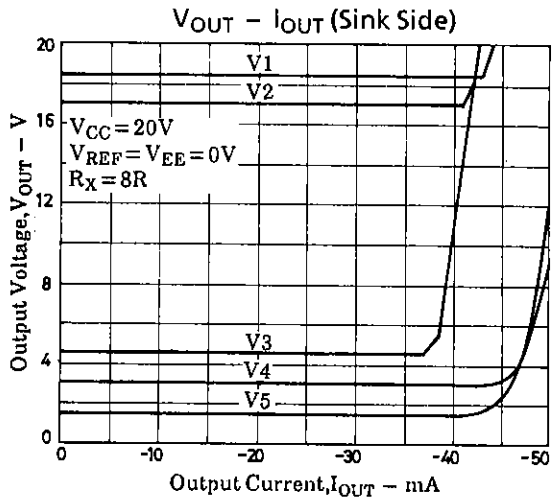
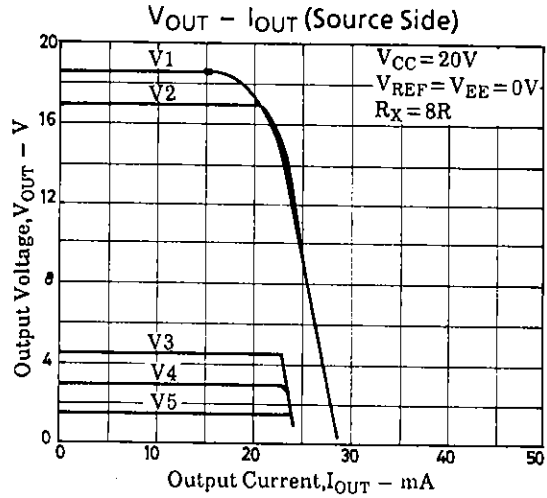
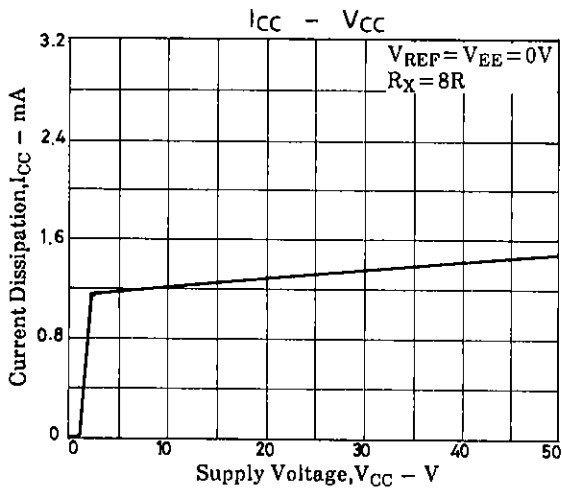
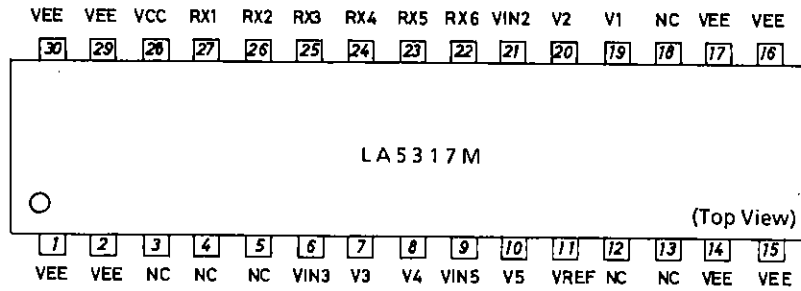
Equivalent Circuit Block Diagram



Note : Use the IC so that $V_{RX1} \geq V_{RX2} \geq V_{RX3} \geq V_{RX4} \geq V_{RX5} \geq V_{RX6}$ is obtained.

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Pin Assignment



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