

SNx4HC595 8-Bit Shift Registers With 3-State Output Registers

1 Features

- 8-Bit Serial-In, Parallel-Out Shift
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads
- Low Power Consumption: 80- μ A (Maximum) I_{CC}
- $t_{pd} = 13$ ns (Typical)
- ± 6 -mA Output Drive at 5 V
- Low Input Current: 1 μ A (Maximum)
- Shift Register Has Direct Clear
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Network Switches
- Power Infrastructure
- LED Displays
- Servers

3 Description

The SNx4HC595 devices contain an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial outputs for cascading. When the output-enable (\overline{OE}) input is high, the outputs are in the high-impedance state.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|--------------------|
| SN54HC595 | LCCC (20) | 8.89 mm x 8.89 mm |
| | CDIP (16) | 21.34 mm x 6.92 mm |
| SN74HC595 | PDIP (16) | 19.31 mm x 6.35 mm |
| | SOIC (16) | 9.90 mm x 3.90 mm |
| | SOIC (16) | 10.30 mm x 7.50 mm |
| | SSOP (16) | 6.20 mm x 5.30 mm |
| | TSSOP (16) | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

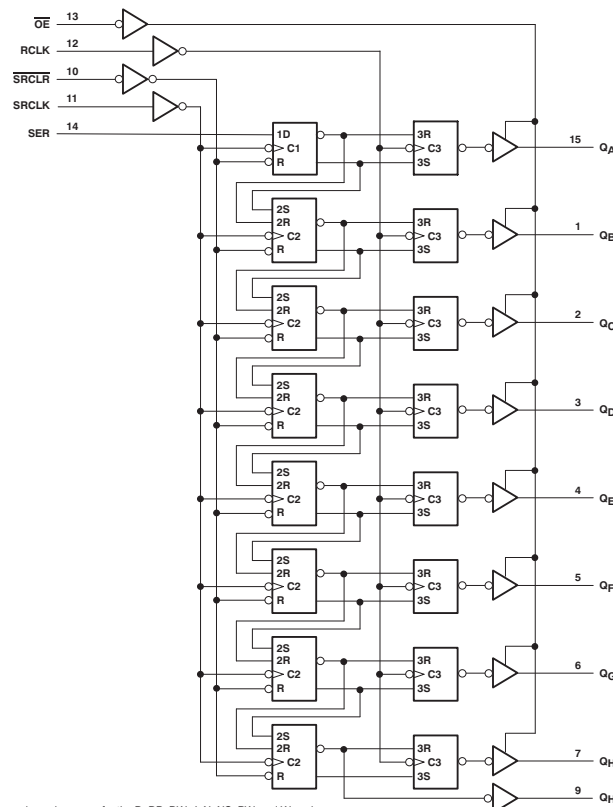


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

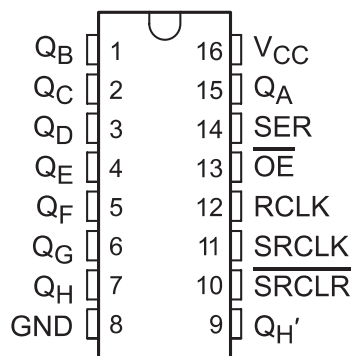
| Changes from Revision H (November 2009) to Revision I | Page |
|--|----------|
| • Added <i>Applications</i> section, <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted <i>Ordering Information</i> table. | 1 |
| • Added Military Disclaimer to <i>Features</i> list. | 1 |

5 Device Comparison Table

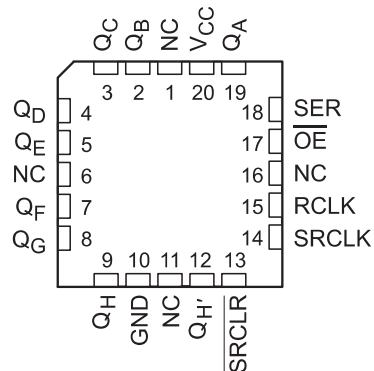
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|--------------------|
| SN54HC595FK | LCCC (20) | 8.89 mm x 8.89 mm |
| SN54HC595J | CDIP (16) | 21.34 mm x 6.92 mm |
| SN74HC595N | PDIP (16) | 19.31 mm x 6.35 mm |
| SN74HC595D | SOIC (16) | 9.90 mm x 3.90 mm |
| SN74HC595DW | SOIC (16) | 10.30 mm x 7.50 mm |
| SN74HC595DB | SSOP (16) | 6.20 mm x 5.30 mm |
| SN74HC595PW | TSSOP (16) | 5.00 mm x 4.40 mm |

6 Pin Configuration and Functions

D, N, NS, J, DB, or PW Package
16-Pin SOIC, PDIP, SO, CDIP, SSOP, or TSSOP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

| NAME | PIN | | I/O | DESCRIPTION |
|--------------------|--------------------------------------|------|-----|--------------------------|
| | SOIC, PDIP, SO, CDIP, SSOP, or TSSOP | LCCC | | |
| GND | 8 | 10 | — | Ground Pin |
| \overline{OE} | 13 | 17 | I | Output Enable |
| Q_A | 15 | 19 | O | Q_A Output |
| Q_B | 1 | 2 | O | Q_B Output |
| Q_C | 2 | 3 | O | Q_C Output |
| Q_D | 3 | 4 | O | Q_D Output |
| Q_E | 4 | 5 | O | Q_E Output |
| Q_F | 5 | 7 | O | Q_F Output |
| Q_G | 6 | 8 | O | Q_G Output |
| Q_H | 7 | 9 | O | Q_H Output |
| $Q_{H'}$ | 9 | 12 | O | $Q_{H'}$ Output |
| RCLK | 12 | 14 | I | RCLK Input |
| SER | 14 | 18 | I | SER Input |
| SRCLK | 11 | 14 | I | SRCLK Input |
| \overline{SRCLR} | 10 | 13 | I | \overline{SRCLR} Input |
| NC | — | 1 | — | No Connection |
| | | 16 | | |
| | | 11 | | |
| | | 16 | | |
| V_{CC} | — | 20 | — | Power Pin |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------------|---|--|------|-----|------|
| V _{CC} | Supply voltage | | -0.5 | 7 | V |
| I _{IK} | Input clamp current ⁽²⁾ | V _I < 0 or V _I > V _{CC} | | ±20 | mA |
| I _{OK} | Output clamp current ⁽²⁾ | V _O < 0 or V _O > V _{CC} | | ±20 | mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | | ±35 | mA |
| | Continuous current through V _{CC} or GND | | | ±70 | mA |
| T _J | Junction temperature | | | 150 | °C |
| T _{stg} | Storage temperature | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | SN54HC595 | | | SN74HC595 | | | UNIT |
|-----------------|---|-------------------------|-----------------|-----|-----------|-----------------|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | | 1.5 | | | V |
| | | V _{CC} = 4.5 V | 3.15 | | 3.15 | | | |
| | | V _{CC} = 6 V | 4.2 | | 4.2 | | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | | 0.5 | | | V |
| | | V _{CC} = 4.5 V | | | 1.35 | | | |
| | | V _{CC} = 6 V | | | 1.8 | | | |
| V _I | Input voltage | 0 | V _{CC} | | 0 | V _{CC} | | V |
| V _O | Output voltage | 0 | V _{CC} | | 0 | V _{CC} | | V |
| Δt/Δv | Input transition rise or fall time ⁽²⁾ | V _{CC} = 2 V | 1000 | | 1000 | | | ns |
| | | V _{CC} = 4.5 V | 500 | | 500 | | | |
| | | V _{CC} = 6 V | 400 | | 400 | | | |
| T _A | Operating free-air temperature | -55 | 125 | | -40 | 85 | | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).
- (2) If this device is used in the threshold region (from V_{IL,max} = 0.5 V to V_{IH,min} = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_i = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74AHCT595 | | | | | | UNIT |
|---|-------------|-----------|-----------|----------|---------|------------|------|
| | D (SOIC) | DB (SSOP) | DW (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | |
| | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance | 73 | 82 | 57 | 67 | 64 | 108 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

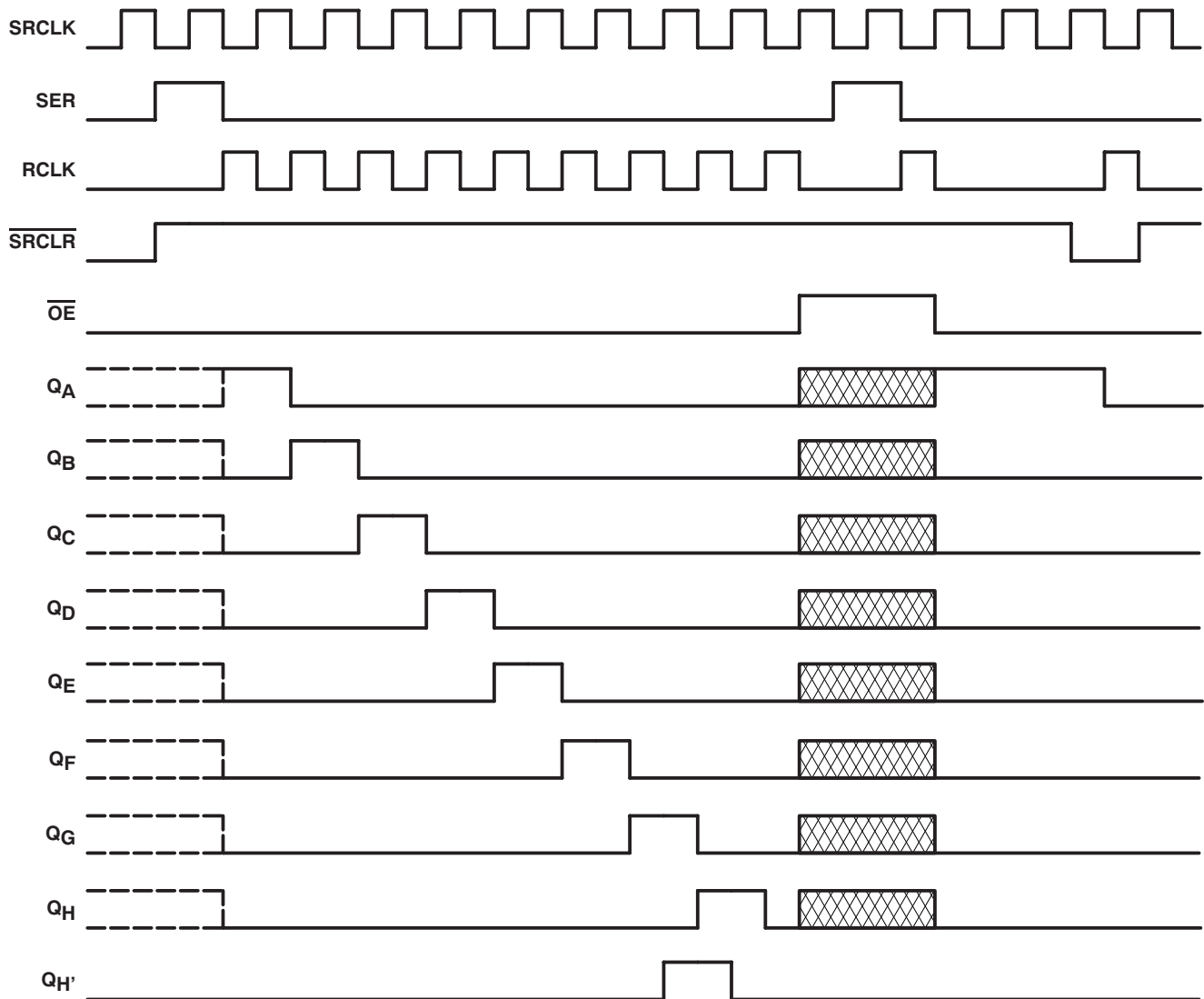
| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54HC595 | | SN74HC595 | | UNIT | |
|-----------------|--|--------------------------|---|-------|-------|-----------|-------|-----------|-------|------|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | 4.5 V | Q _H , I _{OH} = -4 mA | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | | Q _A - Q _H , I _{OH} = -6 mA | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | | Q _H , I _{OH} = -5.2 mA | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| 6 V | Q _A - Q _H , I _{OH} = -7.8 mA | 5.48 | 5.8 | | 5.2 | | 5.34 | | | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | Q _H , I _{OL} = 4 mA | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | | Q _A - Q _H , I _{OL} = 6 mA | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | | Q _H , I _{OL} = 5.2 mA | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| 6 V | Q _A - Q _H , I _{OL} = 7.8 mA | | 0.15 | 0.26 | | 0.4 | | 0.33 | | | |
| I _I | V _I = V _{CC} or 0 | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA | |
| I _{OZ} | V _O = V _{CC} or 0, Q _A - Q _H | 6 V | | ±0.01 | ±0.5 | | ±10 | | ±5 | μA | |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | 6 V | | | 8 | | 160 | | 80 | μA | |
| C _i | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF | |

7.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC595 | | SN74HC595 | | UNIT |
|--------------------|---|-----------------|-----------------------|-----|-----------|-----|-----------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | 2 V | 6 | | 4.2 | | 5 | | MHz |
| | | 4.5 V | 31 | | 21 | | 25 | | |
| | | 6 V | 36 | | 25 | | 29 | | |
| t _w | SRCLK or RCLK high or low | 2 V | 80 | | 120 | | 100 | | ns |
| | | 4.5 V | 16 | | 24 | | 20 | | |
| | | 6 V | 14 | | 20 | | 17 | | |
| | $\overline{\text{SRCLR}}$ low | 2 V | 80 | | 120 | | 100 | | |
| | | 4.5 V | 16 | | 24 | | 20 | | |
| | | 6 V | 14 | | 20 | | 17 | | |
| t _{su} | SER before SRCLK↑ | 2 V | 100 | | 150 | | 125 | | ns |
| | | 4.5 V | 20 | | 30 | | 25 | | |
| | | 6 V | 17 | | 25 | | 21 | | |
| | SRCLK↑ before RCLK↑ ⁽¹⁾ | 2 V | 75 | | 113 | | 94 | | |
| | | 4.5 V | 15 | | 23 | | 19 | | |
| | | 6 V | 13 | | 19 | | 16 | | |
| | $\overline{\text{SRCLR}}$ low before RCLK↑ | 2 V | 50 | | 75 | | 65 | | |
| | | 4.5 V | 10 | | 15 | | 13 | | |
| | | 6 V | 9 | | 13 | | 11 | | |
| | $\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑ | 2 V | 50 | | 75 | | 60 | | |
| | | 4.5 V | 10 | | 15 | | 12 | | |
| | | 6 V | 9 | | 13 | | 11 | | |
| t _h | Hold time, SER after SRCLK↑ | 2 V | 0 | | 0 | | 0 | | ns |
| | | 4.5 V | 0 | | 0 | | 0 | | |
| | | 6 V | 0 | | 0 | | 0 | | |

(1) This set-up time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.




NOTE:  implies that the output is in 3-State mode.

Figure 1. Timing Diagram

7.7 Switching Characteristics

Over recommended operating free-air temperature range.

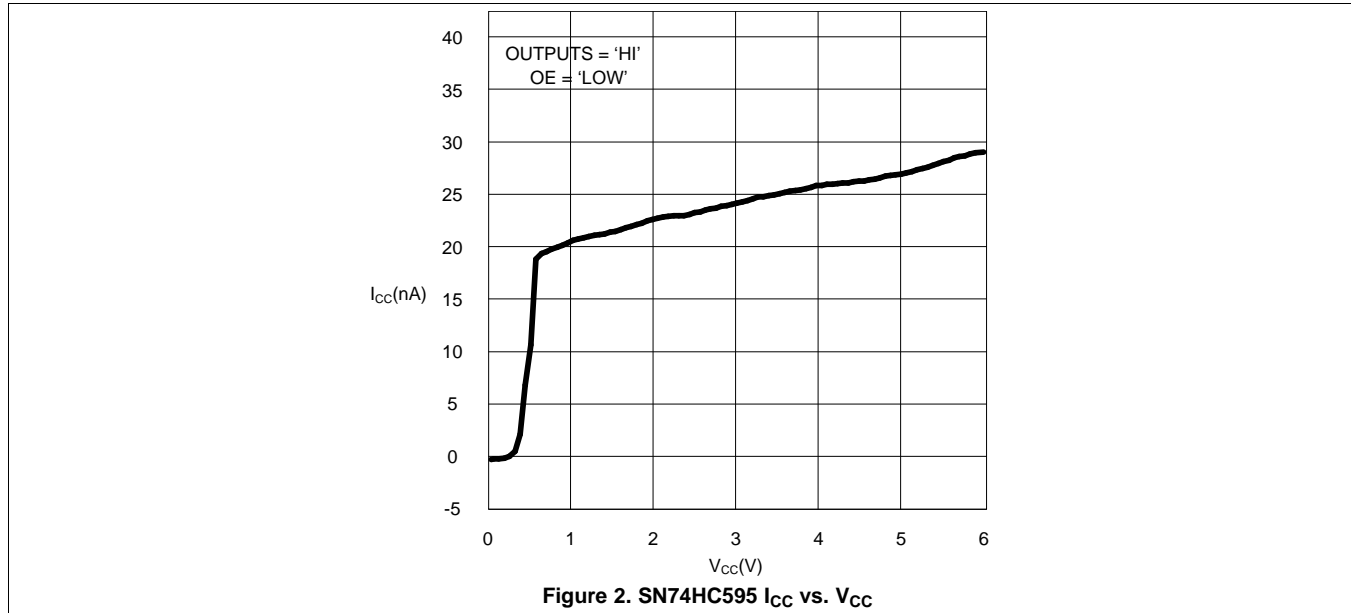
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | V _{CC} | T _A = 25°C | | | SN54HC595 | | SN74HC595 | | UNIT |
|------------------|---------------------------|---------------------------------|------------------|-----------------|-----------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f _{max} | | | 50 pF | 2 V | 6 | 26 | | 4.2 | | 5 | MHz | |
| | | | | 4.5 V | 31 | 38 | | 21 | | 25 | | |
| | | | | 6 V | 36 | 42 | | 25 | | 29 | | |
| t _{pd} | SRCLK | Q _{H'} | 50 pF | 2 V | | 50 | 160 | | 240 | | 200 | ns |
| | | | | 4.5 V | | 17 | 32 | | 48 | | 40 | |
| | | | | 6 V | | 14 | 27 | | 41 | | 34 | |
| | RCLK | Q _A – Q _H | 50 pF | 2 V | | 50 | 150 | | 225 | | 187 | |
| | | | | 4.5 V | | 17 | 30 | | 45 | | 37 | |
| | | | | 6 V | | 14 | 26 | | 38 | | 32 | |
| t _{PHL} | $\overline{\text{SRCLR}}$ | Q _{H'} | 50 pF | 2 V | | 51 | 175 | | 261 | | 219 | ns |
| | | | | 4.5 V | | 18 | 35 | | 52 | | 44 | |
| | | | | 6 V | | 15 | 30 | | 44 | | 37 | |
| t _{en} | $\overline{\text{OE}}$ | Q _A – Q _H | 50 pF | 2 V | | 40 | 150 | | 255 | | 187 | ns |
| | | | | 4.5 V | | 15 | 30 | | 45 | | 37 | |
| | | | | 6 V | | 13 | 26 | | 38 | | 32 | |
| t _{dis} | $\overline{\text{OE}}$ | Q _A – Q _H | 50 pF | 2 V | | 42 | 200 | | 300 | | 250 | ns |
| | | | | 4.5 V | | 23 | 40 | | 60 | | 50 | |
| | | | | 6 V | | 20 | 34 | | 51 | | 43 | |
| t _t | | Q _A – Q _H | 50 pF | 2 V | | 28 | 60 | | 90 | | 75 | ns |
| | | | | 4.5 V | | 8 | 12 | | 18 | | 15 | |
| | | | | 6 V | | 6 | 10 | | 15 | | 13 | |
| | | Q _{H'} | 50 pF | 2 V | | 28 | 75 | | 110 | | 95 | |
| | | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | | 6 V | | 6 | 13 | | 19 | | 16 | |
| t _{pd} | RCLK | Q _A – Q _H | 150 pf | 2 V | | 60 | 200 | | 300 | | 250 | ns |
| | | | | 4.5 V | | 22 | 40 | | 60 | | 50 | |
| | | | | 6 V | | 19 | 34 | | 51 | | 43 | |
| t _{en} | $\overline{\text{OE}}$ | Q _A – Q _H | 150 pf | 2 V | | 70 | 200 | | 298 | | 250 | ns |
| | | | | 4.5 V | | 23 | 40 | | 60 | | 50 | |
| | | | | 6 V | | 19 | 34 | | 51 | | 43 | |
| t _t | | Q _A – Q _H | 150 pf | 2 V | | 45 | 210 | | 315 | | 265 | ns |
| | | | | 4.5 V | | 17 | 42 | | 63 | | 53 | |
| | | | | 6 V | | 13 | 36 | | 53 | | 45 | |

7.8 Operating Characteristics

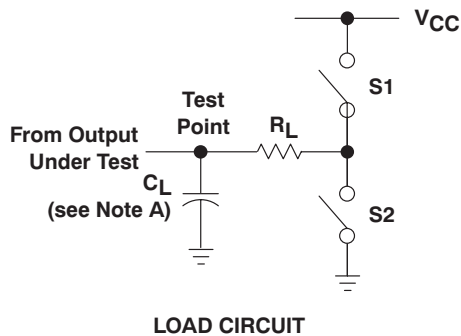
T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|-----------------|-----|------|
| C _{pd} Power dissipation capacitance | No load | 400 | pF |

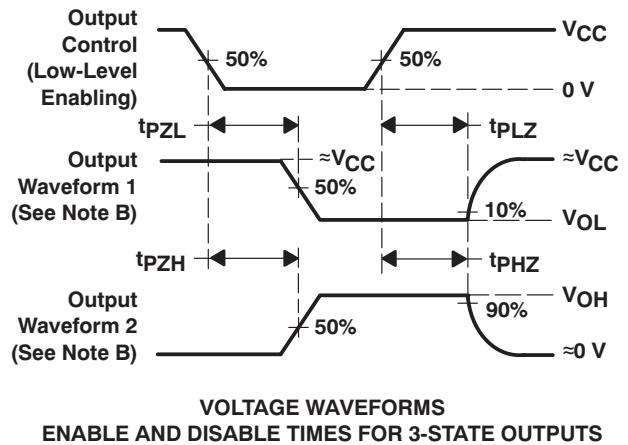
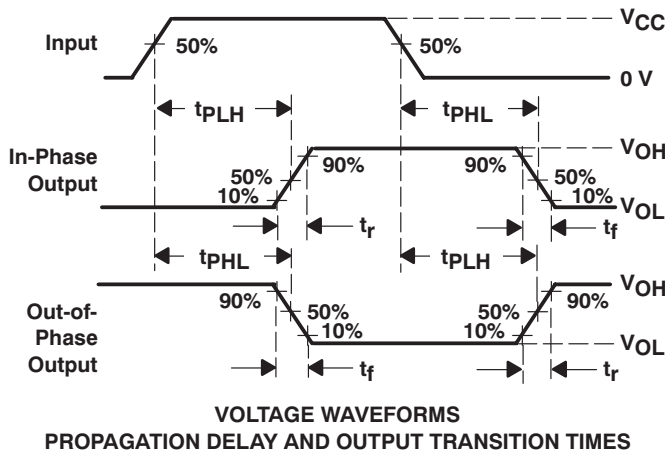
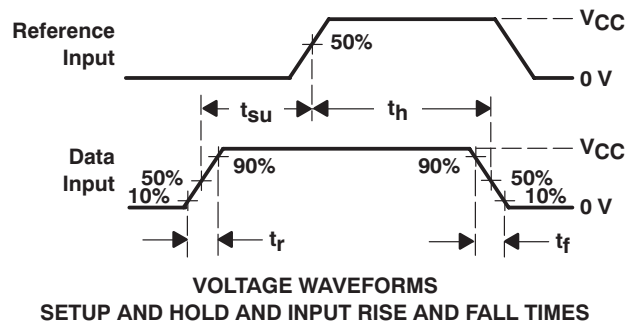
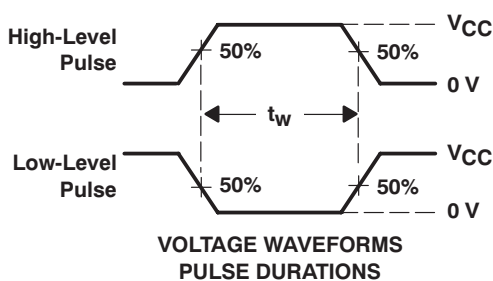
7.9 Typical Characteristics



8 Parameter Measurement Information



| PARAMETER | R_L | C_L | S1 | S2 |
|-------------------|--------------|-----------------|--------|--------|
| t_{en} | 1 k Ω | 50 pF or 150 pF | Open | Closed |
| | | | Closed | Open |
| t_{dis} | 1 k Ω | 50 pF | Open | Closed |
| | | | Closed | Open |
| t_{pd} or t_t | | 50 pF or 150 pF | Open | Open |



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - The outputs are measured one at a time, with one input transition per measurement.
 - t_{pLZ} and t_{pHZ} are the same as t_{dis} .
 - t_{pZL} and t_{pZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SNx4HC595 is part of the HC family of logic devices intended for CMOS applications. The SNx4HC595 is an 8-bit shift register that feeds an 8-bit D-type storage register.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

9.2 Functional Block Diagram

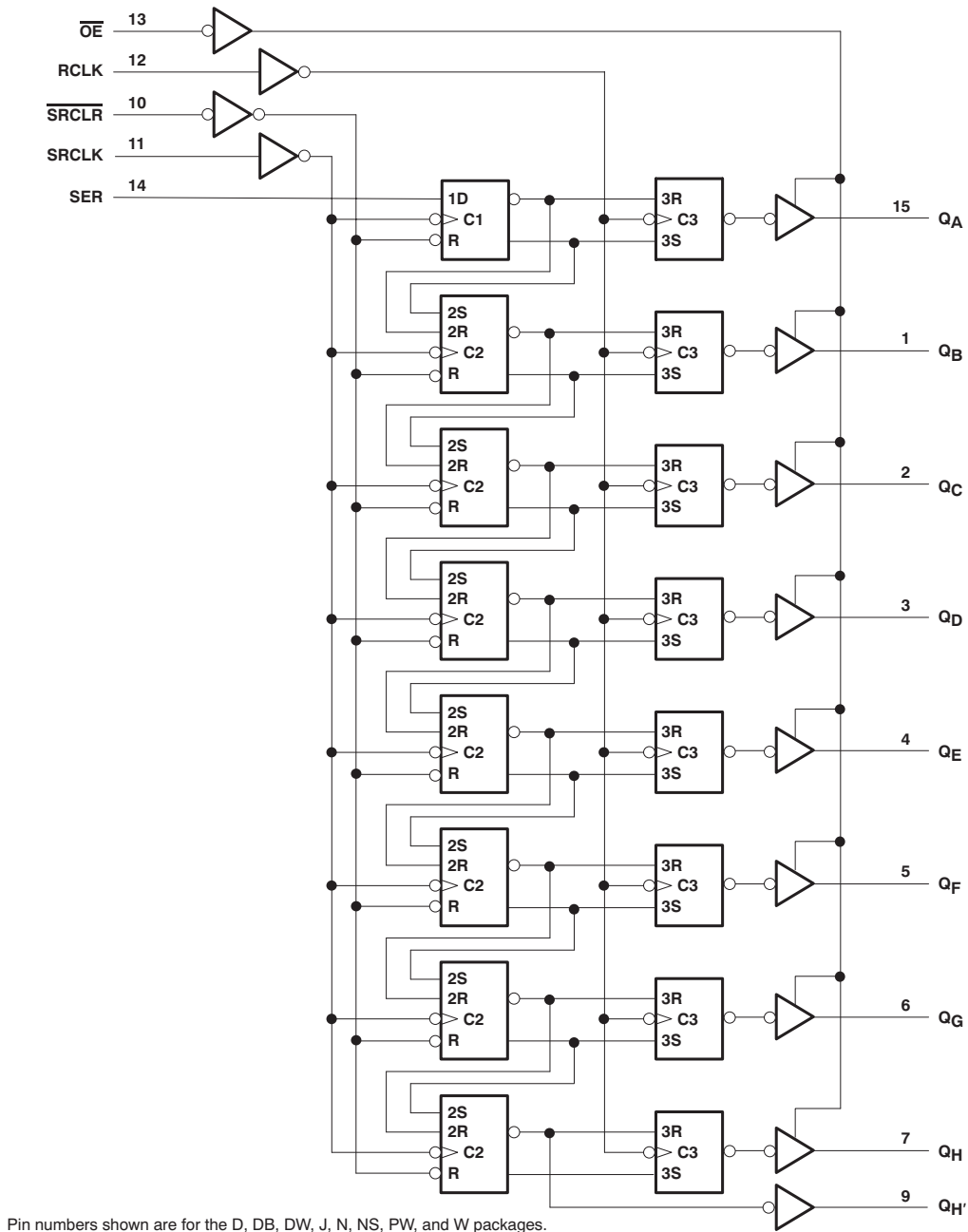


Figure 4. Logic Diagram (Positive Logic)

9.3 Feature Description

The SNx4HC595 devices are 8-bit Serial-In, Parallel-Out Shift Registers. They have a wide operating current of 2 V to 6 V, and the high-current 3-state outputs can drive up to 15 LSTTL Loads. The devices have a low power consumption of 80- μ A (Maximum) I_{CC} . Additionally, the devices have a low input current of 1 μ A (Maximum) and a ± 6 -mA Output Drive at 5 V.

9.4 Device Functional Modes

Table 1 lists the functional modes of the SNx4HC595 devices.

Table 1. Function Table

| INPUTS | | | | | FUNCTION |
|--------|------------|-------|------------|-----------------|--|
| SER | SRCLK | SRCLR | RCLK | \overline{OE} | |
| X | X | X | X | H | Outputs $Q_A - Q_H$ are disabled. |
| X | X | X | X | L | Outputs $Q_A - Q_H$ are enabled. |
| X | X | L | X | X | Shift register is cleared. |
| L | \uparrow | H | X | X | First stage of the shift register goes low. Other stages store the data of previous stage, respectively. |
| H | \uparrow | H | X | X | First stage of the shift register goes high. Other stages store the data of previous stage, respectively. |
| X | X | X | \uparrow | X | Shift-register data is stored in the storage register. |

10 Application and Implementation

10.1 Application Information

The SNx4HC595 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

10.2 Typical Application

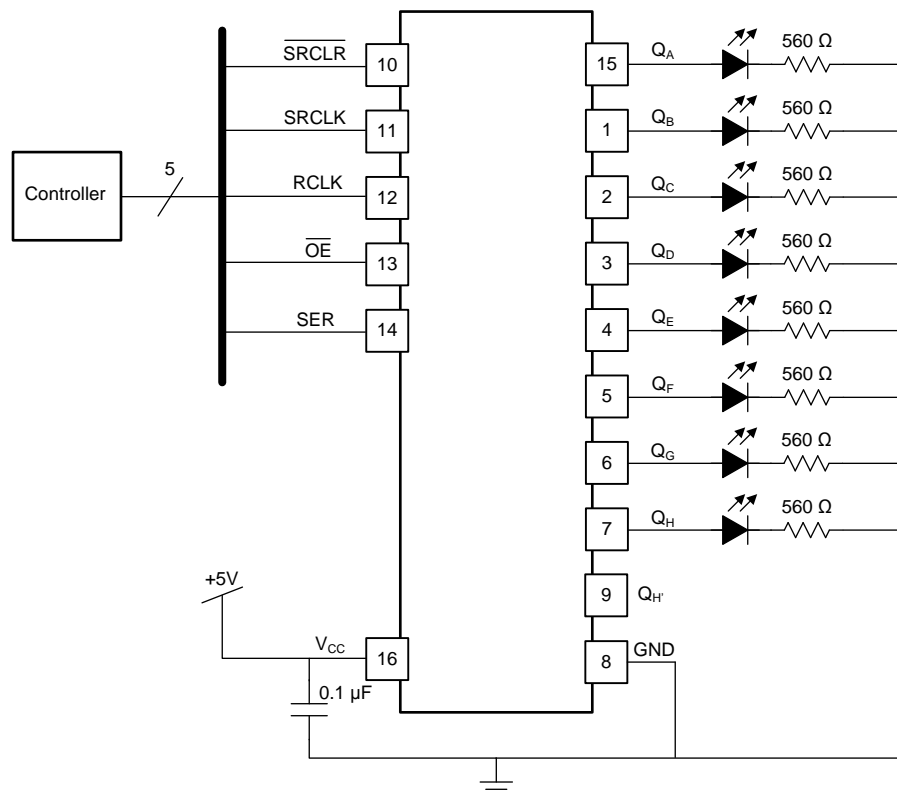


Figure 5. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

- Recommended input conditions
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
- Recommend output conditions
 - Load currents should not exceed 35 mA per output and 70 mA total for the part
 - Outputs should not be pulled above V_{CC}

Typical Application (continued)

10.2.3 Application Curves

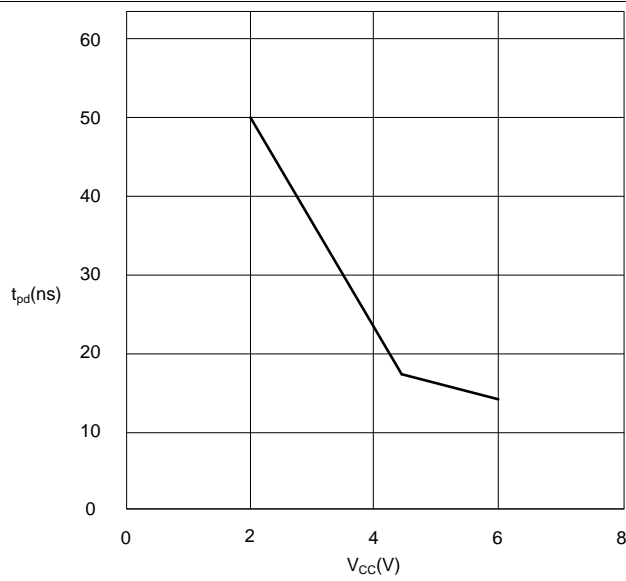


Figure 6. SN75HC595 t_{pd} vs. V_{CC}

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μf is recommended; if there are multiple V_{CC} pins, then 0.01 μf or 0.022 μf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μf and a 1 μf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 7](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

12.2 Layout Example

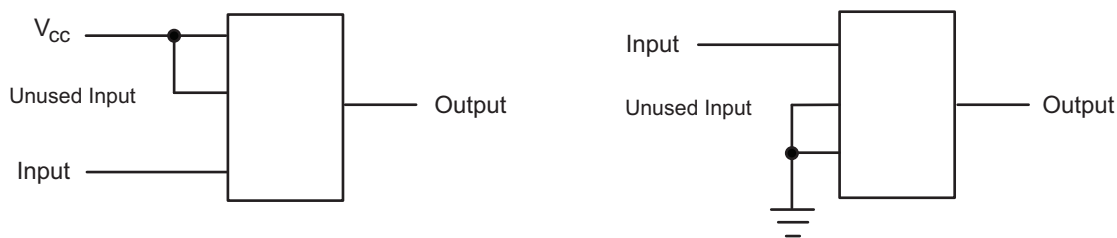


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, [SCBA004](#)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54HC595 | Click here | Click here | Click here | Click here | Click here |
| SN74HC595 | Click here | Click here | Click here | Click here | Click here |

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------|--------------------------------------|----------------------|--------------|------------------------------------|-------------------------|
| 5962-86816012A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Non-Green | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-86816012A SNJ54HC 595FK | Samples |
| 5962-8681601EA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Non-Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8681601EA SNJ54HC595J | Samples |
| 5962-8681601VEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Non-Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8681601VE A SNV54HC595J | Samples |
| 5962-8681601VFA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Non-Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8681601VF A SNV54HC595W | Samples |
| SN54HC595J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Non-Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54HC595J | Samples |
| SN74HC595D | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DBR | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DBRE4 | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DBRG4 | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DE4 | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DG4 | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DRE4 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DRG3 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DRG4 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DT | ACTIVE | SOIC | D | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|--------------------------------------|----------------------|--------------|--|-------------------------|
| SN74HC595DWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DWRE4 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595DWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU SN | N / A for Pkg Type | -40 to 85 | SN74HC595N | Samples |
| SN74HC595NE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC595N | Samples |
| SN74HC595NSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595PW | ACTIVE | TSSOP | PW | 16 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595PWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SN74HC595PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC595 | Samples |
| SNJ54HC595FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Non-Green | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 86816012A SNJ54HC 595FK | Samples |
| SNJ54HC595J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Non-Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8681601EA SNJ54HC595J | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC595, SN54HC595-SP, SN74HC595 :

- Catalog: [SN74HC595](#), [SN54HC595](#)

- Automotive: [SN74HC595-Q1](#), [SN74HC595-Q1](#)

- Enhanced Product: [SN74HC595-EP](#), [SN74HC595-EP](#)

- Military: [SN54HC595](#)

- Space: [SN54HC595-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC595DR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC595DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC595DRG3 | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC595DRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC595DRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC595DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| SN74HC595DWRG4 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| SN74HC595NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC595PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC595PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC595PWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC595DR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74HC595DR | SOIC | D | 16 | 2500 | 853.0 | 449.0 | 35.0 |
| SN74HC595DRG3 | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74HC595DRG4 | SOIC | D | 16 | 2500 | 853.0 | 449.0 | 35.0 |
| SN74HC595DRG4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74HC595DWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| SN74HC595DWRG4 | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| SN74HC595NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74HC595PWR | TSSOP | PW | 16 | 2000 | 853.0 | 449.0 | 35.0 |
| SN74HC595PWR | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74HC595PWRG4 | TSSOP | PW | 16 | 2000 | 853.0 | 449.0 | 35.0 |

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |

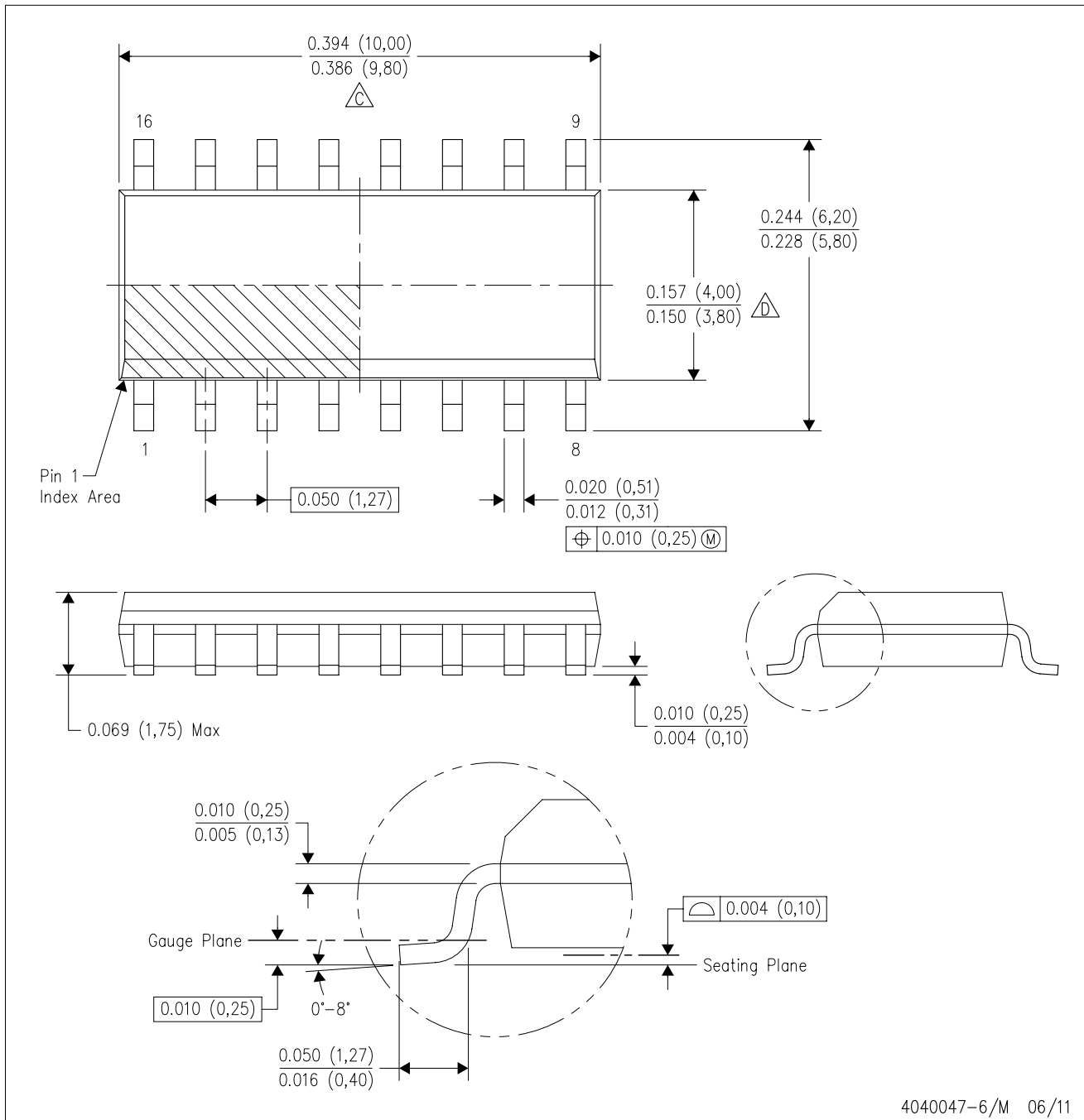


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

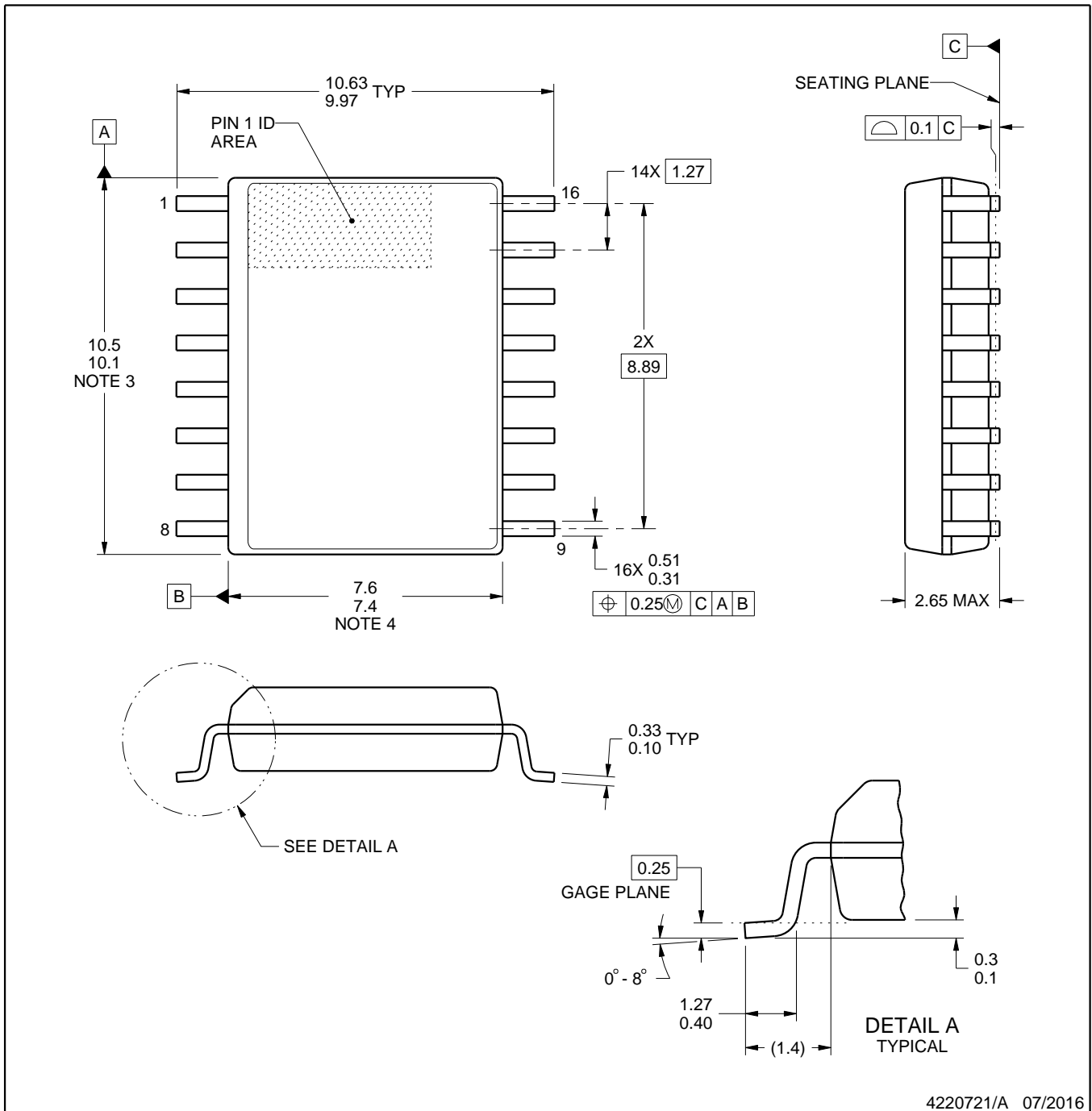


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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