Dual Synchronous DC/DC Controllers with Current Sharing Control

Features

- Two Operation Modes
  - Independent Operation
  - Two-Phase Operation with Current Sharing
- Driving N-Channel MOSFETs
- 300kHz Constant Frequency Operation
- Built-in Feedback Compensation
  - Voltage-Mode PWM Control
  - Fast Transient Response
- ±1% VREF Accuracy Over Temperature
- Adjustable Output Voltage by an External Resistor Divider
- Phase-Shifted Switchers to Minimize Ripple
- Current Limit with 50% Fold-Back
- Soft-Start and Enable Function
- Power-ON Reset (POR) Monitor
- Power Good Monitor for Outputs

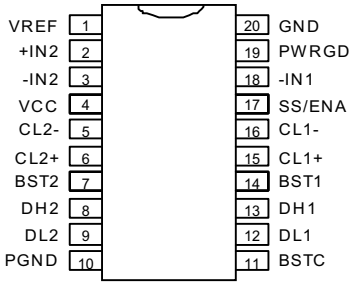
Applications

- Graphics Cards
- DDR Memory
- SSTL-2 Termination
- Power Supply Requiring Two Outputs

General Description

The APW1175 is a two-phase, synchronous, and voltage mode PWM controller to provide dual channel or single outputs in two distinct operation modes. In independent mode, the two PWM converters supply two independently regulated voltages by converting a common or two different power inputs. In two-phase mode, the two PWM converters supply one regulated voltage with programmable current sharing control by converting a common or two different power inputs. The two-phase mode can supply the larger power than that provided each single channel. APW1175 features an internal 300KHz oscillator, VCC Power-On-Reset (POR), an external adjustable soft-start and the programmable output current limit with 50% fold-back. The two PWM controllers are 180° out of phase to minimize the input ripple (common power input) and the output ripple (two-phase mode).

Pin Description



Ordering and Marking Information

APW1175 □□-□□ □

- Lead Free Code
- Handling Code
- Temp. Range
- Package Code

Package Code
K : SOP-20
Temp. Range
C : 0 to 70°C
Handling Code
TU : Tube TR : Tape & Reel
Lead Free Code
L : Lead Free Device Blank : Orginal Device

APW1175 K :

XXXXX - Date Code

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

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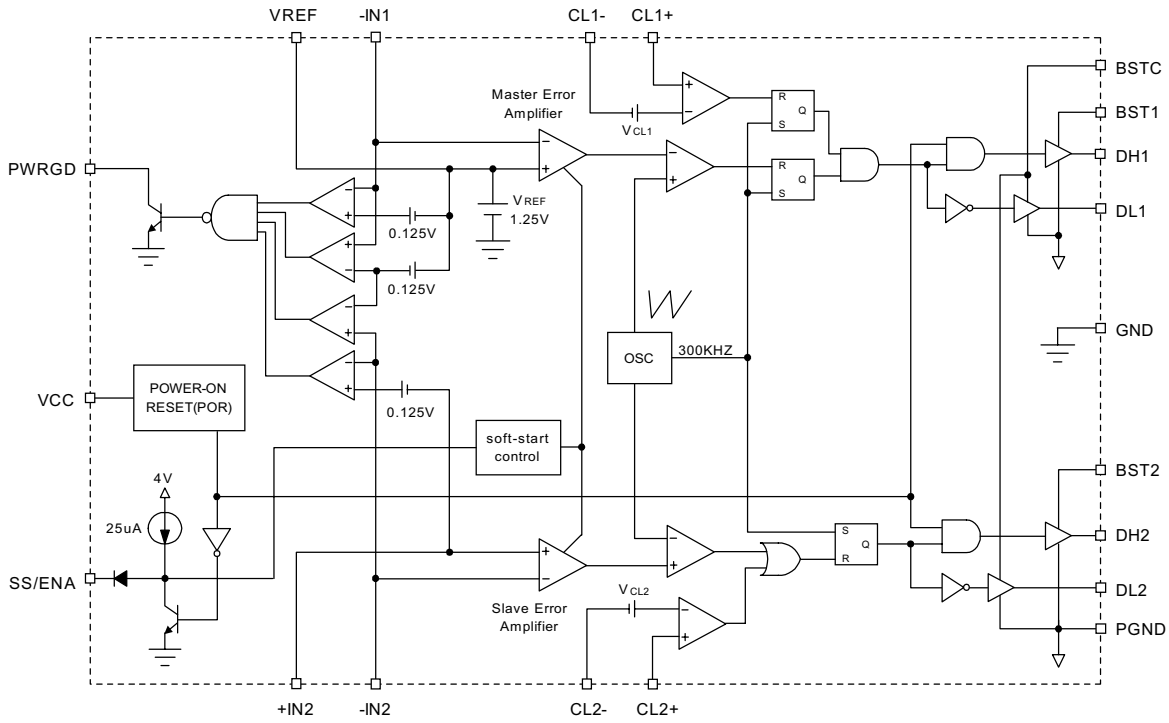
Block Diagram



Absolute Maximum Ratings

- VCC to GND . . . . . -0.3V ~ 15V
- PGND to GND . . . . . ±1V
- BST to GND . . . . . -0.3V ~ 22V
- Junction Temperature . . . . . 150°C
- Storage Temperature . . . . . -65°C ~ 150°C
- Soldering Temperature . . . 300°C , 10 Seconds
- Minimum ESD Rating . . . . . ±3kV

Operating Conditions

- VCC . . . . . 4.2V ~ 15V
- BST. . . . . 5V ~ 17V
- Ambient Temperature Range . . . 0°C to 85°C
- Junction Temperature Range. . . . 0°C to 125°C

Thermal Characteristics

Symbol	Parameter	Rating	Unit
R_{JA}	Thermal Resistance in Free Air		
	SOIC	75	°C/W
	SOIC(with 3in^2 of Copper)	65	

Electrical Characteristics

Unless otherwise specified, these specifications apply over VCC=4.75~5.25V, GND=PGND=0V, and T_A=0~85°C. Typical values refer to T_A=25°C.

Symbol	Parameter	Test Conditions	APW1175			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{CC}	V_{CC} Supply Current	V_{CC}=5~15V, F_{OSC}=300kHz		9		mA
I_{BSTC}	BSTC Supply Current	BSTC=5V, DL1,2=Open, F_{OSC}=300kHz		2.8		mA
$I_{BST1,2}$	BST1,2 Supply Current	BST1,2=10V, DH1,2=Open, F_{OSC}=300kHz		1.6		mA
POWER-ON RESET						
	V_{CC} POR Threshold Voltage	V_{CC} Rising		3.6	4.2	V
OSCILLATOR						
F_{OSC}	Oscillator Frequency		270	300	330	KHz
	Maximum Duty Cycle	DH1	80	90		%
		DH2		100		
ΔV_{OSC}	Ramp Amplitude			1.1		V
ERROR AMPLIFIER						
A_{OL}	Error Amplifier Voltage Gain			35		dB
	Input Bias Current (-IN1, +IN2, -IN2)	Input Voltage = 1.25V		0.5	1	µA
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage	Measure Pin 1	1.238	1.250	1.262	V
	V_{REF} Load Regulation	I_{REF} = 1mA		3.5		mV
	V_{REF} Line Regulation	V_{CC} = 5~15V			0.5	%
PWM CONTROLLERS GATE DRIVERS						
	DH Source	BSTH-DH=5V BSTH-DH=2.5V	1 0.5			A
	DH Sink	DH-PGND=3.5V DH-PGND=1.75V	1 0.5			A
	DL Source	BSTL-DL=5V BSTL-DL=2.5V	1 0.5			A
	DL Sink	DL-PGND=3.5V DL-PGND=1.75V	1 0.5			A
	Dead Time		50	200		nS
CURRENT LIMIT PROTECTION						
V_{CL}	Current Limit Voltage		60	70	80	mV
	Fold Back Current	V_{OUT}=0V (refer to application circuit)		50%		I_{LIM}
	Fold Back Voltage Knee	I=I_{LIM} (refer to application circuit)	1.25		V_{OUT}	V
SOFT-START						
I_{SS}	Soft-Start Current	V_{SS}=1V		25		µA
	Soft-Start Transition	Synchronous PWM		3.3		V

Electrical Characteristics Cont.

Symbol	Parameter	Test Conditions	APW1175			Unit
			Min	Typ	Max	
POWER GOOD						
	Upper -IN1 Threshold			110%		V_{REF}
	Lower –IN1 Threshold			90%		V_{REF}
	Upper –IN2 Threshold			V_{+IN2} +0.1V_{REF}		V
	Lower –IN2 Threshold			90%		V_{REF}
	PWRGD Voltage Low	I_{PWRGD}=-5mA			0.8	V

Functional Pin Description

VREF (Pin 1)

Internal 1.25V reference voltage . This pin is internally connected to the positive input of the master channel error amplifier.

+IN2 (Pin 2)

Positive input of the slave channel error amplifier. Connect this pin to 1.25V reference (Pin 1) for the two independent channel configuration.

-IN2, -IN1 (Pin 3, 18)

Negative inputs of the slave and master error amplifier.

VCC (Pin 4)

Connect this pin to 5V~15 V power to provides the bias for the control circuitry. Need a 1uF multi-layer ceramic decoupling capacitor to GND (Pin 20). The voltage at this pin is also monitored for Power-On Reset (POR) purpose.

CL2-, CL2+, CL1+, CL1- (Pin 5,6,15,16)

Current sense input pins. Connect the positive and negative inputs to output current sense resistor for each channel. A current limit comparator for each channel to limit the output current while the difference voltage between the positive and negaive inputs is greater than the 75mV reference.

A RC filter is required for noise rejection.

BST2,BST1 (Pin 7,14)

Power inputs to the high-side MOSFET drivers. A boot-strap circuit may be used to pump a boot voltage .

DH2, DH1 (Pin 8,13)

High-side MOSFET drivers to provide strong drive current to drive each high-side MOSFET. A small series resistor to the gate of the MOSFET maybe required for each pin.

DL2, DL1 (Pin 9,12)

Low-side MOSFET drivers to provide strong drive current to drive each low-side MOSFET. A small series resistor to the gate of the MOSFET maybe required for each pin.

PGND (Pin 10)

Power ground connection. The pin provide the path for return of gate drive currents.

BSTC (Pin 11)

This pin provide supply voltage to the low-side MOSFET drivers.

SS/ENA (Pin 17)

Connect a capacitor from this pin to ground.This capacitor, along with an internal 25uA current source, sets the soft-start interval, preventing the outputs from overshoot as well as limiting the input current. Pull this pin to below 1.4V to shutdown the outputs

PWRGD (Pin 19)

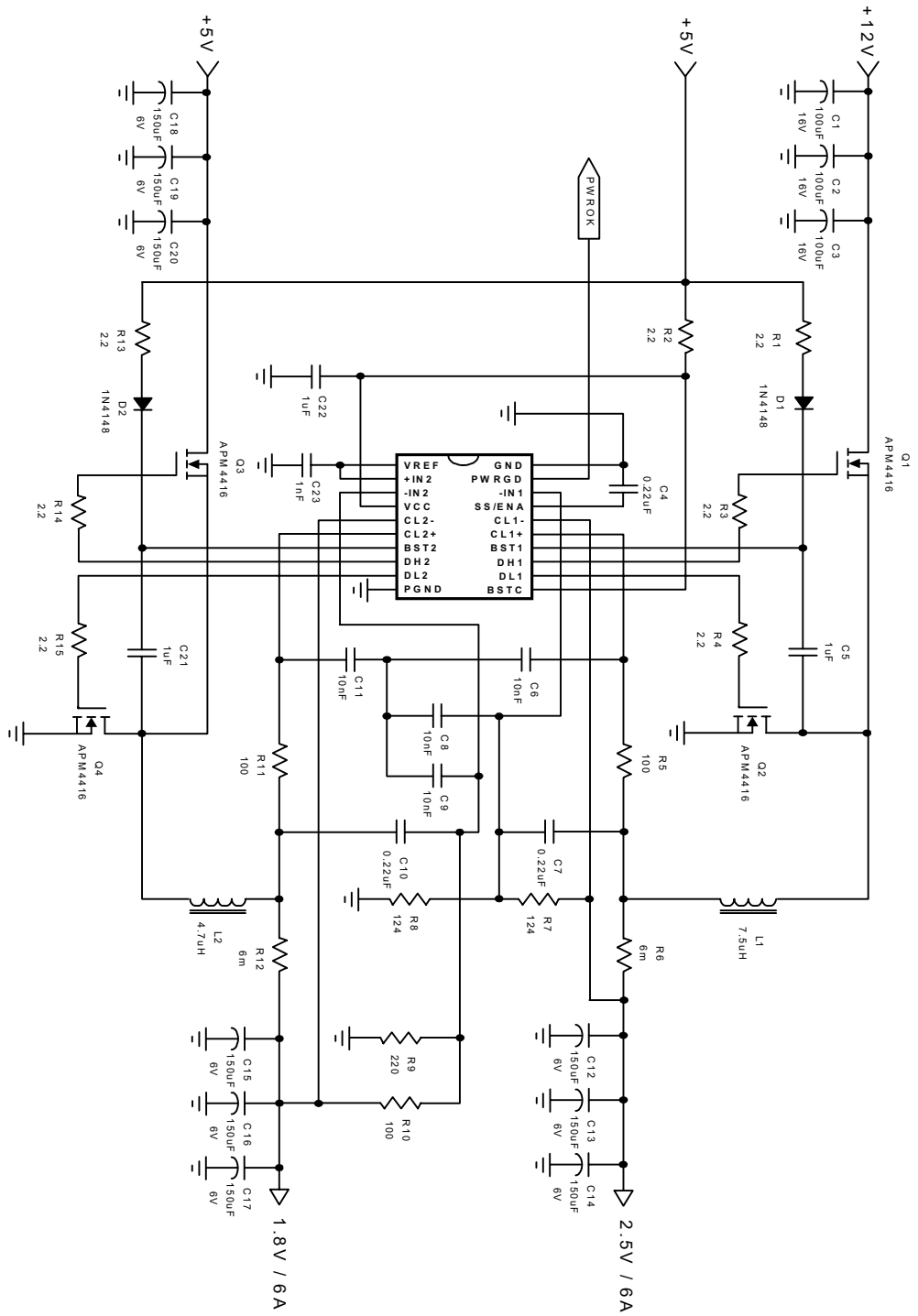
Power good signal output pin. This pin is an open collector output, which is pulled low if the output voltage is outside the power good window.

GND (Pin 20)

Signal ground for the control circuitry. All voltage levels are measured with respect to this pin.

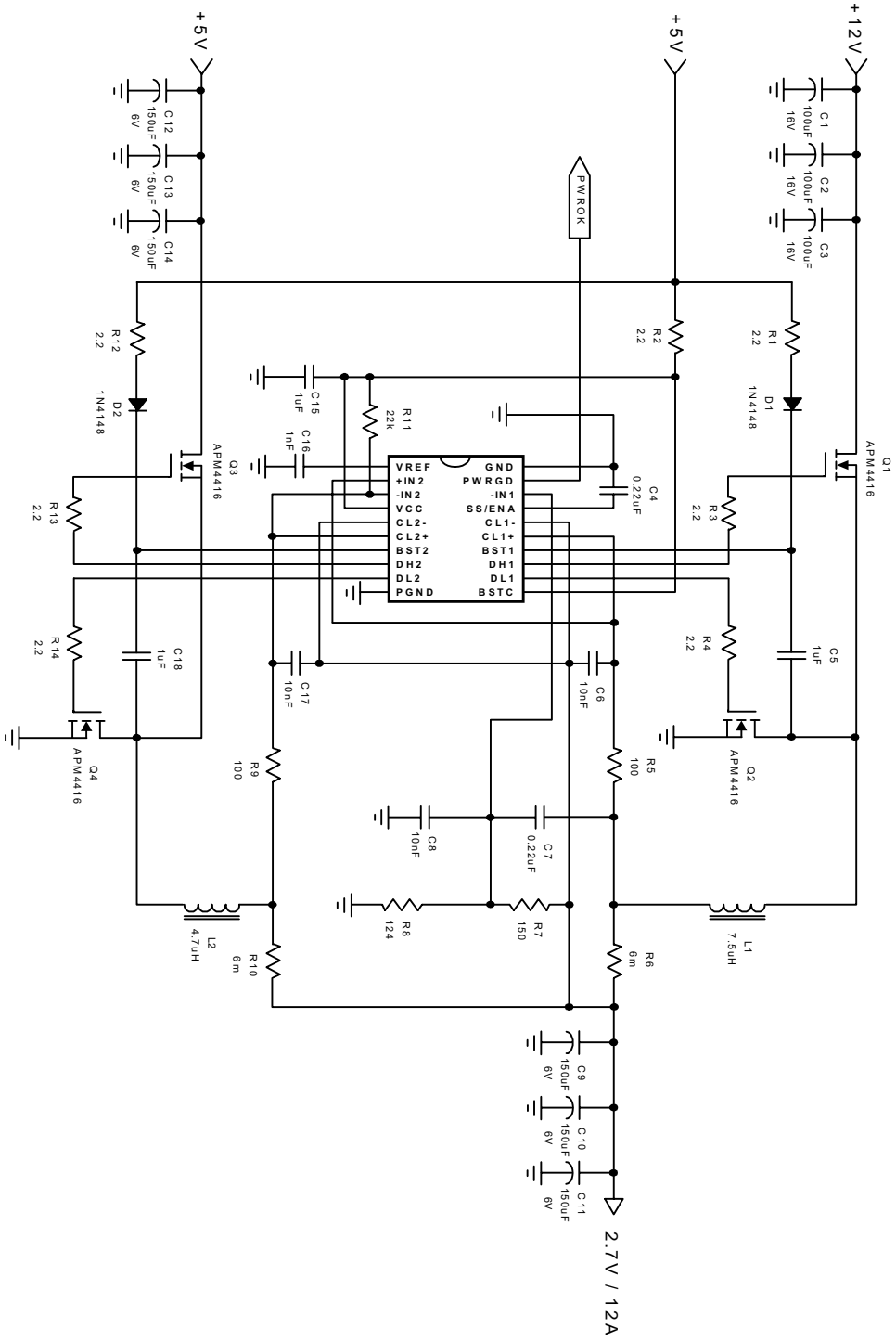
Typical Application

1. Independent Operation



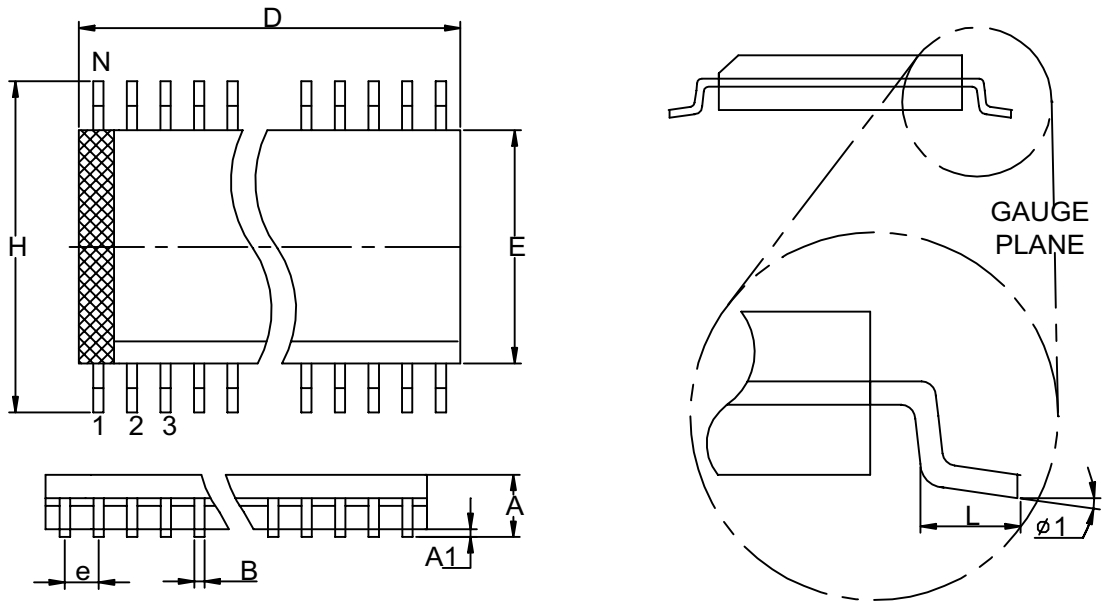
Typical Application

2. Two-Phase Operation with Current Sharing Control



Packaging Information

SO – 300mil (Reference JEDEC Registration MS-013)



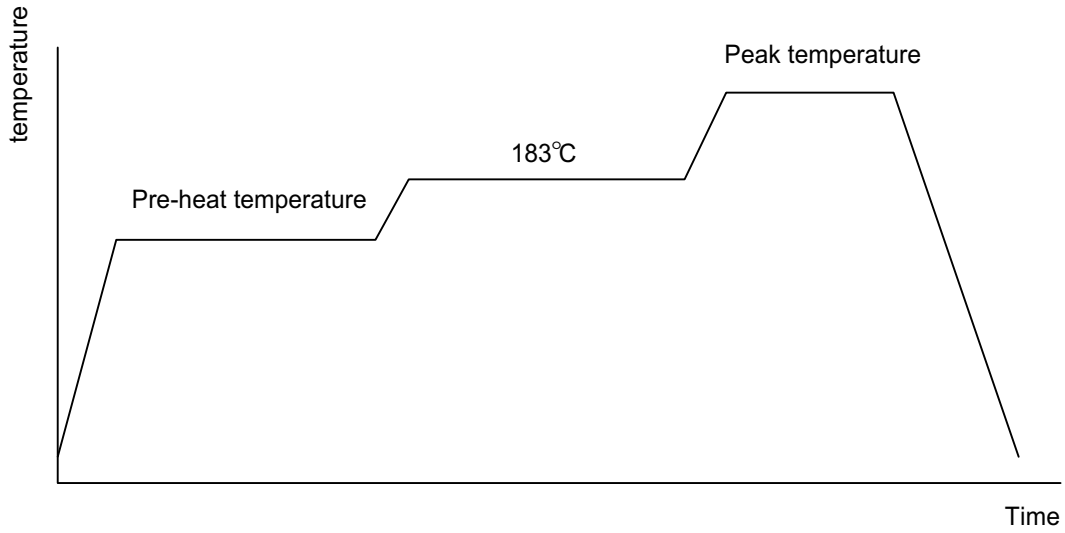
Dim	Millimeters		Variations- D			Dim	Inches		Variations- D		
	Min.	Max.	Variations	Min.	Max.		Min.	Max.	Variations	Min.	Max.
A	2.35	2.65	SO-16	10.10	10.50	A	0.093	0.1043	SO-16	0.398	0.413
A1	0.10	0.30	SO-18	11.35	11.76	A1	0.004	0.0120	SO-18	0.447	0.463
B	0.33	0.51	SO-20	12.60	13	B	0.013	0.020	SO-20	0.496	0.512
D	See variations		SO-24	15.20	15.60	D	See variations		SO-24	0.599	0.614
E	7.40	7.60	SO-28	17.70	18.11	E	0.2914	0.2992	SO-28	0.697	0.713
e	1.27BSC		SO-14	8.80	9.20	e	0.050BSC		SO-14	0.347	0.362
H	10	10.65				H	0.394	0.419			
L	0.40	1.27				L	0.016	0.050			
N	See variations					N	See variations				
ϕ 1	0°	8°				ϕ 1	0°	8°			

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb)
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A APRIL 1999



Classification Reflow Profiles

	Convection or IR/ Convection	VPR
Average ramp-up rate(183°C to Peak)	3°C/second max.	10 °C /second max.
Preheat temperature 125 ± 25°C)	120 seconds max	
Temperature maintained above 183°C	60 – 150 seconds	
Time within 5°C of actual peak temperature	10 –20 seconds	60 seconds
Peak temperature range	220 +5/-0°C or 235 +5/-0°C	215-219°C or 235 +5/-0°C
Ramp-down rate	6 °C /second max.	10 °C /second max.
Time 25°C to peak temperature	6 minutes max.	

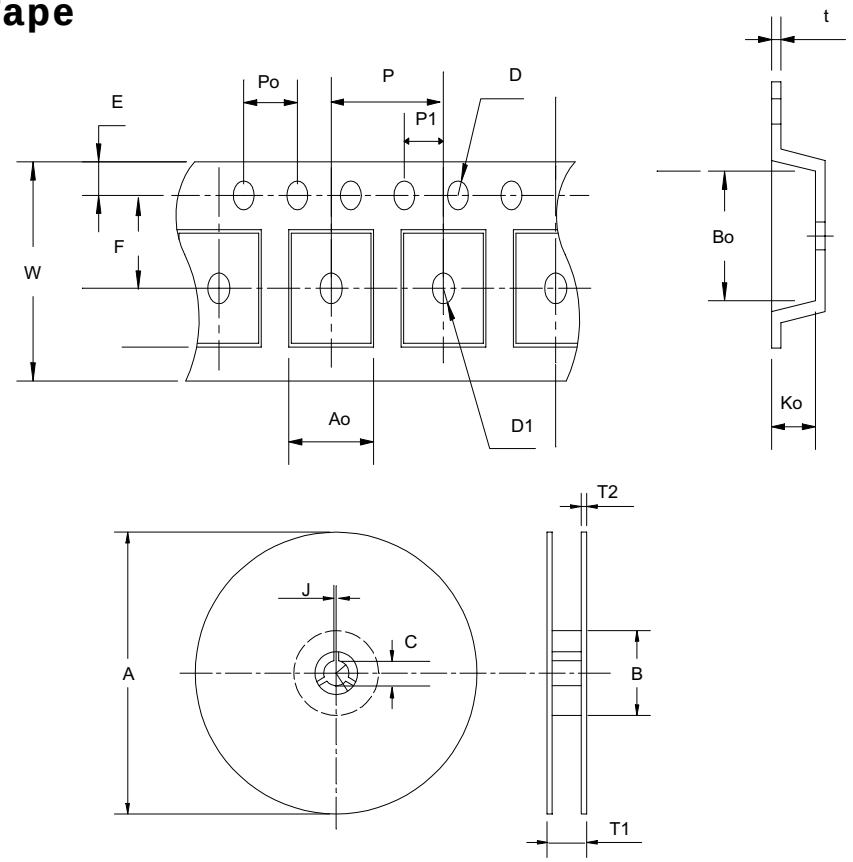
Package Reflow Conditions

pkg. thickness ≥ 2.5mm and all bgas	pkg. thickness < 2.5mm and pkg. volume ≥ 350 mm³	pkg. thickness < 2.5mm and pkg. volume < 350mm³
Convection 220 +5/-0 °C		Convection 235 +5/-0 °C
VPR 215-219 °C		VPR 235 +5/-0 °C
IR/Convection 220 +5/-0 °C		IR/Convection 235 +5/-0 °C

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Carrier Tape



Application	A	B	C	J	T1	T2	W	P	E
SOP- 20	330±1	62 ±1.5	12.75 + 0.15	2 + 0.6	24.4 + 0.2	2 ± 0.2	24 + 0.3 -0.1	12 + 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	11.5 ± 0.1	1.5 +0.1	1.5+ 0.25	4.0 ± 0.1	2.0 ± 0.1	8.2 ± 0.1	13± 0.1	2.5± 0.1	.35±0.013

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOP- 20	24	21.3	1000

Customer Service

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