

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ CFD2 650V

650V CoolMOS™ CFD2 Power Transistor
IPx65R660CFD

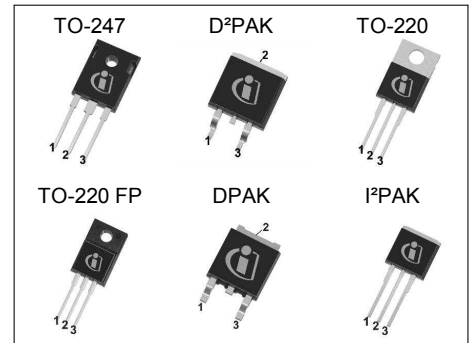
Data Sheet

Rev. 2.7
Final

Industrial & Multimarket

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFD2 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter, and cooler.



Features

- Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM $R_{ds(on)} \cdot Q_g$ and E_{oss}
- Easy to use/drive
- Fully qualified according to JEDEC for Industrial Applications
- Pb-free plating, available in Halogen free mold compound^{a)}

Applications

650V CoolMOS™ CFD2 is especially suitable for resonant switching PWM stages for e.g. PC Silverbox, LCD TV, Lighting, Server, Telecom, and Solar.

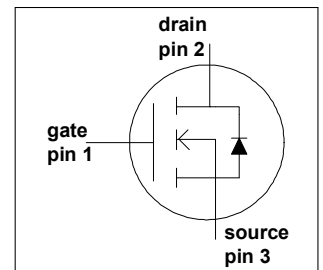


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j \max}$	700	V
$R_{DS(on), \max}$	0.66	Ω
Q_g, typ	22	nC
I_D, pulse	17	A
$E_{oss} @ 400V$	1.8	μJ
Body diode di/dt	900	A/ μs
Q_{rr}	0.2	μC
t_{rr}	65	ns
I_{rrm}	4.5	A

Type / Ordering Code	Package	Marking	Related Links
IPW65R660CFD	PG-TO 247	65F6660	see Appendix A
IPB65R660CFD	PG-TO 263		
IPP65R660CFD	PG-TO 220		
IPA65R660CFD	PG-TO 220 FullPAK		
IPD65R660CFD	PG-TO 252		
IPI65R660CFD	PG-TO 262		



Table of Contents

Description	2
Table of Contents	3
Maximum ratings	4
Thermal characteristics	5
Electrical characteristics	6
Electrical characteristics diagrams	8
Test Circuits	13
Package Outlines	14
Appendix A	20
Revision History	21
Disclaimer	21

2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D			6.0	A	$T_C = 25^\circ\text{C}$
				3.8		$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$			17	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}			115	mJ	$I_b = 1.2\text{A}$, $V_{DD} = 50\text{V}$
Avalanche energy, repetitive	E_{AR}			0.21	mJ	$I_b = 1.2\text{A}$, $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}			1.2	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC ($f > 1\text{ Hz}$)
Power dissipation (non FullPAK) TO-247, TO-220, I ² PAK	P_{tot}			62.5	W	$T_C = 25^\circ\text{C}$
Power dissipation (FullPAK) TO-220 FP	P_{tot}			27.8	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-55		150	$^\circ\text{C}$	
Mounting torque (non FullPAK) TO-247, TO-220, I ² PAK				60	Ncm	M3 and M3.5 screws
Mounting torque (FullPAK) TO-220 FP				50	Ncm	M2.5 screws
Continuous diode forward current	I_S			6.0	A	$T_C = 25^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$			17	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_b$, $T_j = 25^\circ\text{C}$
Maximum diode commutation speed	di_f/dt			900	A/ μs	

¹⁾ Limited by $T_{j\text{ max}}$.

²⁾ Pulse width t_p limited by $T_{j\text{ max}}$

³⁾ $V_{peak} < V_{(BR)DSS}$, $T_j < T_{j\text{ max}}$, identical low side and high side switch with same Rg

3 Thermal characteristics

Table 3 Thermal characteristics TO-247, TO-220, I²PAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			2	°C/W	
Thermal resistance, junction - ambient	R_{thJA}			62	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}			260	°C	1.6 mm (0.063 in.) from case for 10s

Table 4 Thermal characteristics TO-220 FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			4.5	°C/W	
Thermal resistance, junction - ambient	R_{thJA}			80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}			260	°C	1.6 mm (0.063 in.) from case for 10s

Table 5 Thermal characteristics D²PAK, DPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			2	°C/W	
Thermal resistance, junction - ambient ¹⁾	R_{thJA}			62	°C/W	SMD version, device on PCB, minimal footprint
			35			SMD version, device on PCB, 6cm ² cooling area
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}			260	°C	reflow MSL

¹⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650			V	$V_{GS} = 0V, I_D = 1mA$
Gate threshold voltage	$V_{GS(th)}$	3.5	4	4.5	V	$V_{DS} = V_{GS}, I_D = 0.2mA$
Zero gate voltage drain current	I_{DSS}			1	μA	$V_{DS} = 650V, V_{GS} = 0V, T_j = 25^\circ C$
			100			$V_{DS} = 650V, V_{GS} = 0V, T_j = 150^\circ C$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS} = 20V, V_{DS} = 0V$
Drain-source on-state resistance	$R_{DS(on)}$		0.594	0.66	Ω	$V_{GS} = 10V, I_D = 2.1A, T_j = 25^\circ C$
			1.544			$V_{GS} = 10V, I_D = 2.1A, T_j = 150^\circ C$
Gate resistance	R_G		6.5		Ω	$f = 1MHz, \text{open drain}$

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		615		pF	$V_{GS} = 0V, V_{DS} = 100V, f = 1MHz$
Output capacitance	C_{oss}		33		pF	
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$		21		pF	$V_{GS} = 0V, V_{DS} = 0 \dots 400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$		88		pF	$I_D = \text{constant}, V_{GS} = 0V, V_{DS} = 0 \dots 400V$
Turn-on delay time	$t_{d(on)}$		9		ns	$V_{DD} = 400V, V_{GS} = 13V, I_D = 3.2A, R_G = 6.8\Omega$
Rise time	t_r		8		ns	
Turn-off delay time	$t_{d(off)}$		40		ns	
Fall time	t_f		10		ns	

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		3.5		nC	$V_{DD} = 480V, I_D = 3.2A, V_{GS} = 0 \text{ to } 10V$
Gate to drain charge	Q_{gd}		12		nC	
Gate charge total	Q_g		22		nC	
Gate plateau voltage	$V_{plateau}$		6.4		V	

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	$V_{GS} = 0V, I_F = 3.2A, T_j = 25^\circ C$
Reverse recovery time	t_{rr}		65		ns	$V_R = 400V, I_F = 3.2A, dI/dt = 100A/\mu s$
Reverse recovery charge	Q_{rr}		0.2		μC	
Peak reverse recovery current	I_{rrm}		4.5		A	

5 Electrical characteristics diagrams

Table 10

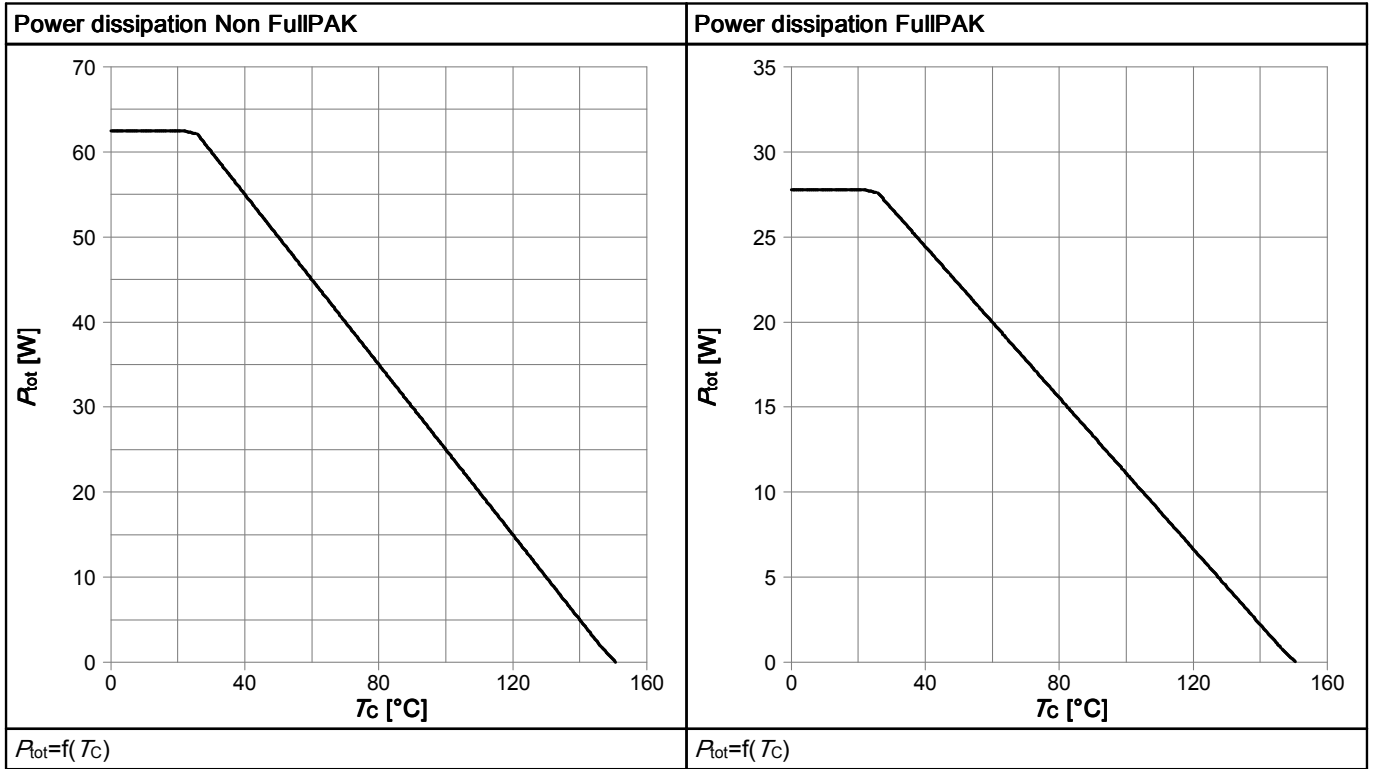


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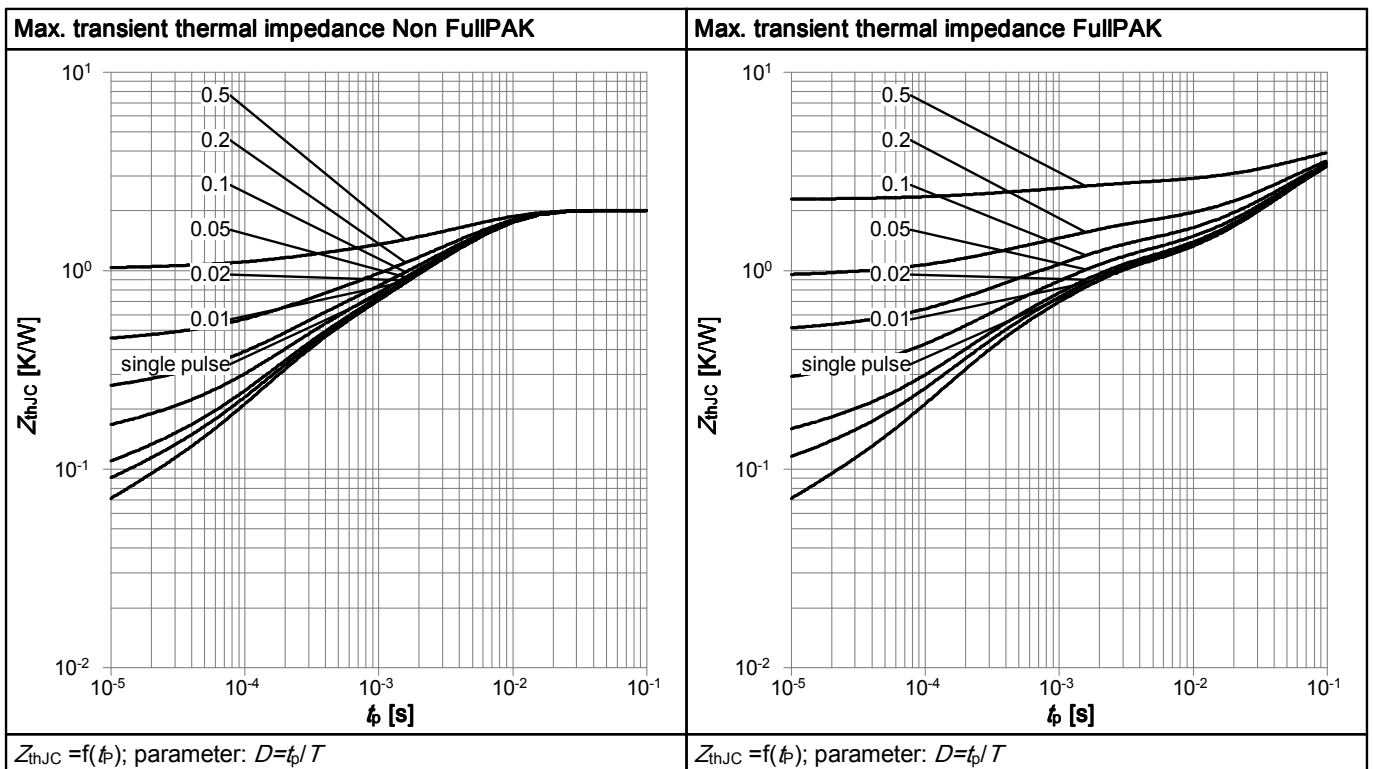


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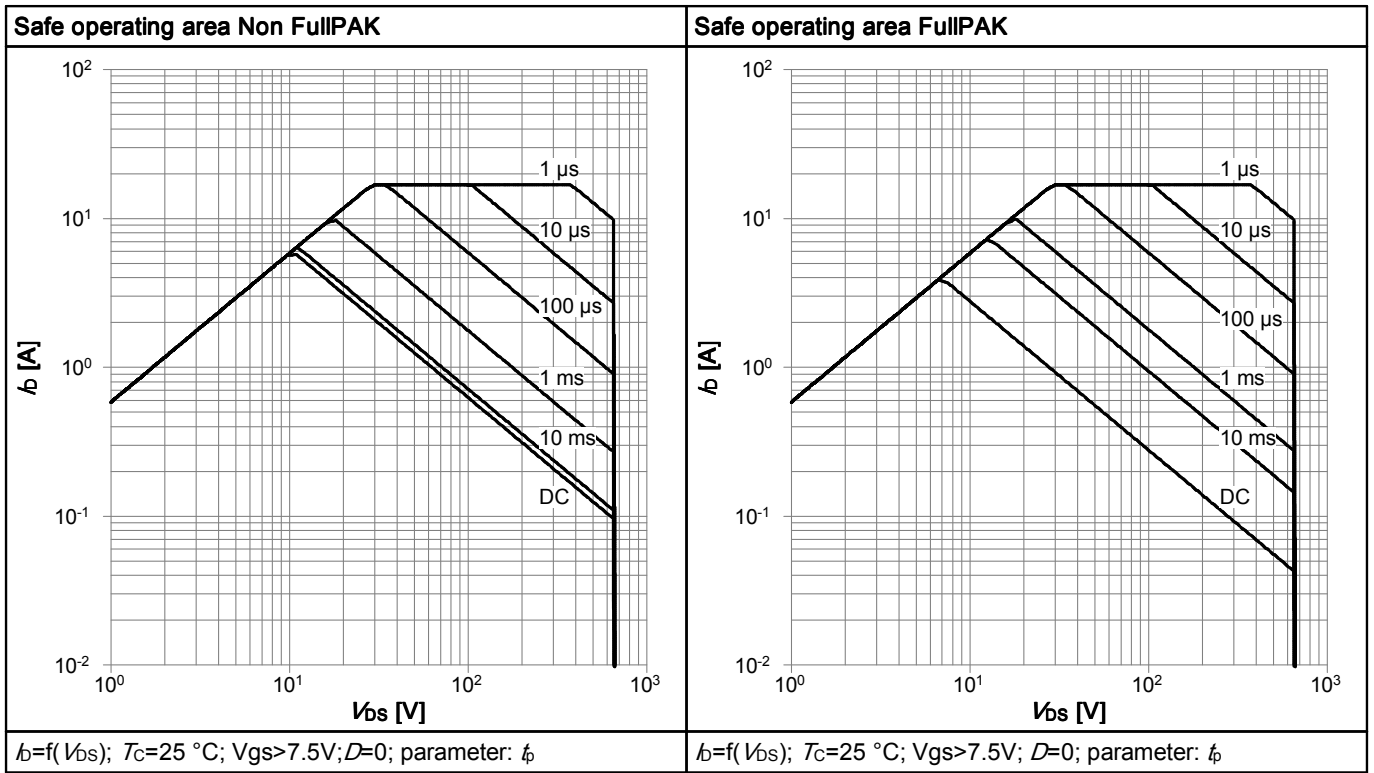


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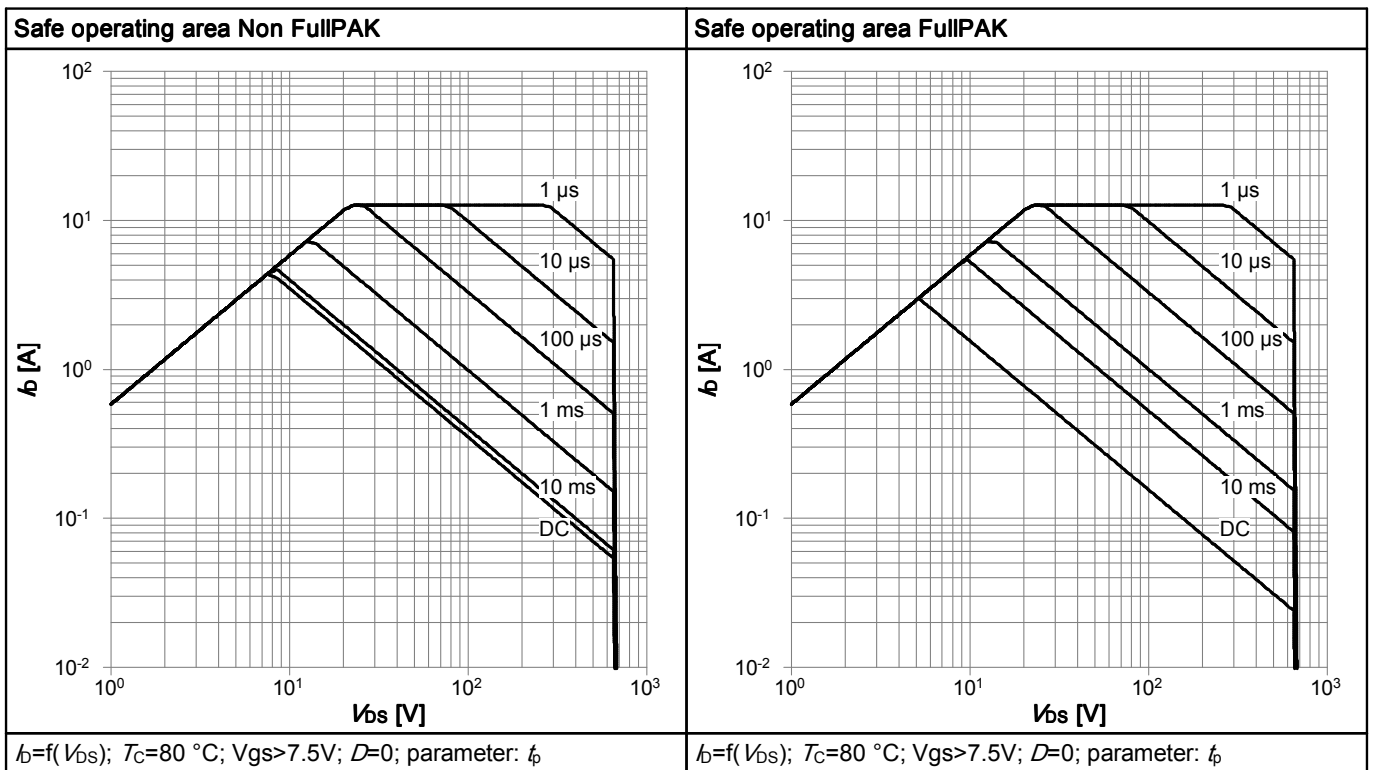


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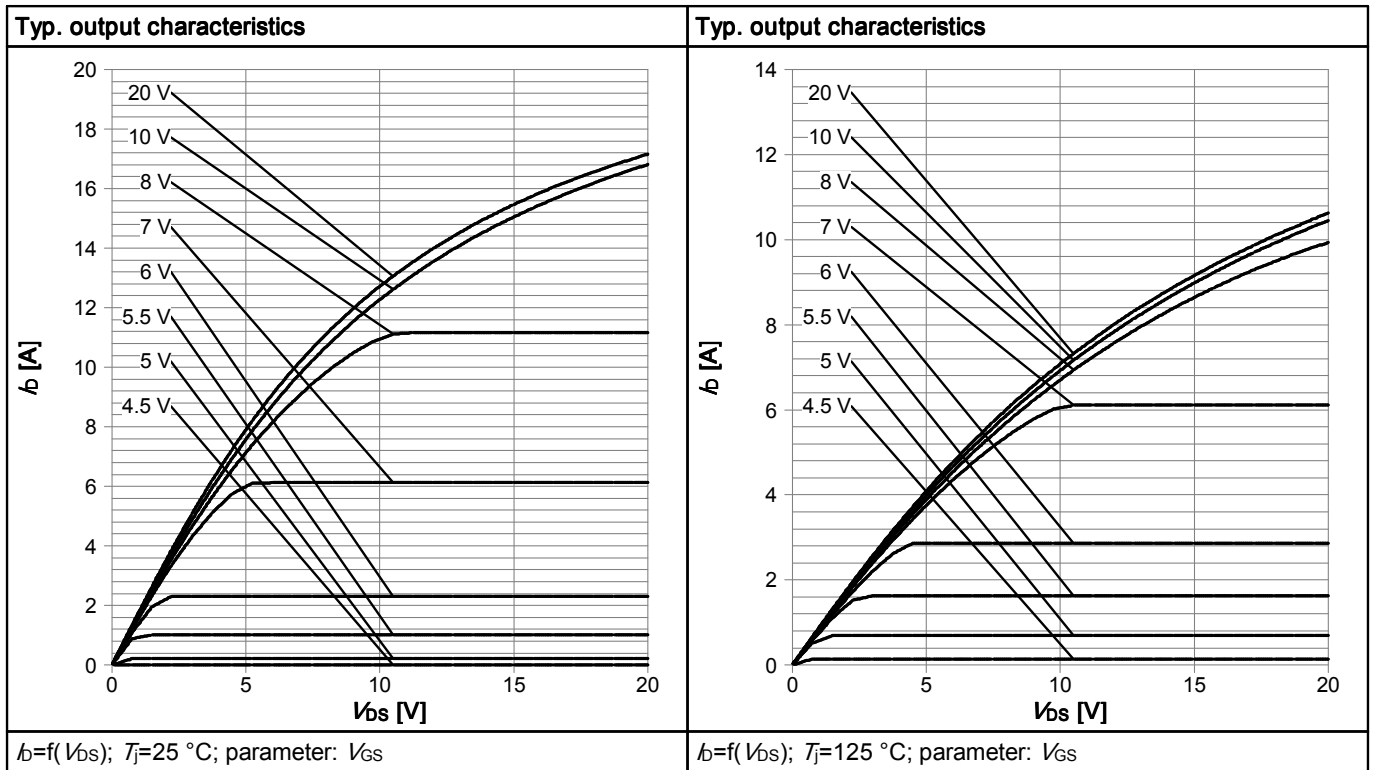


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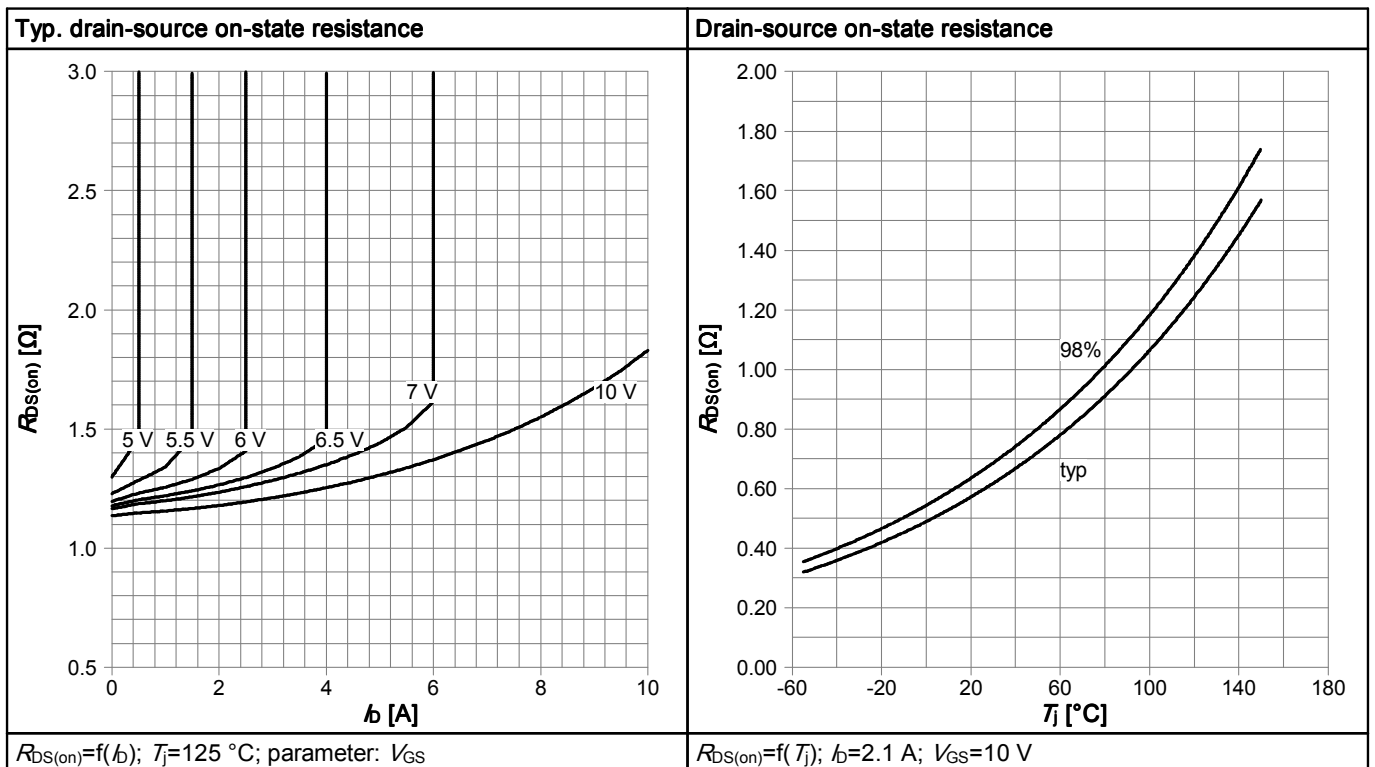


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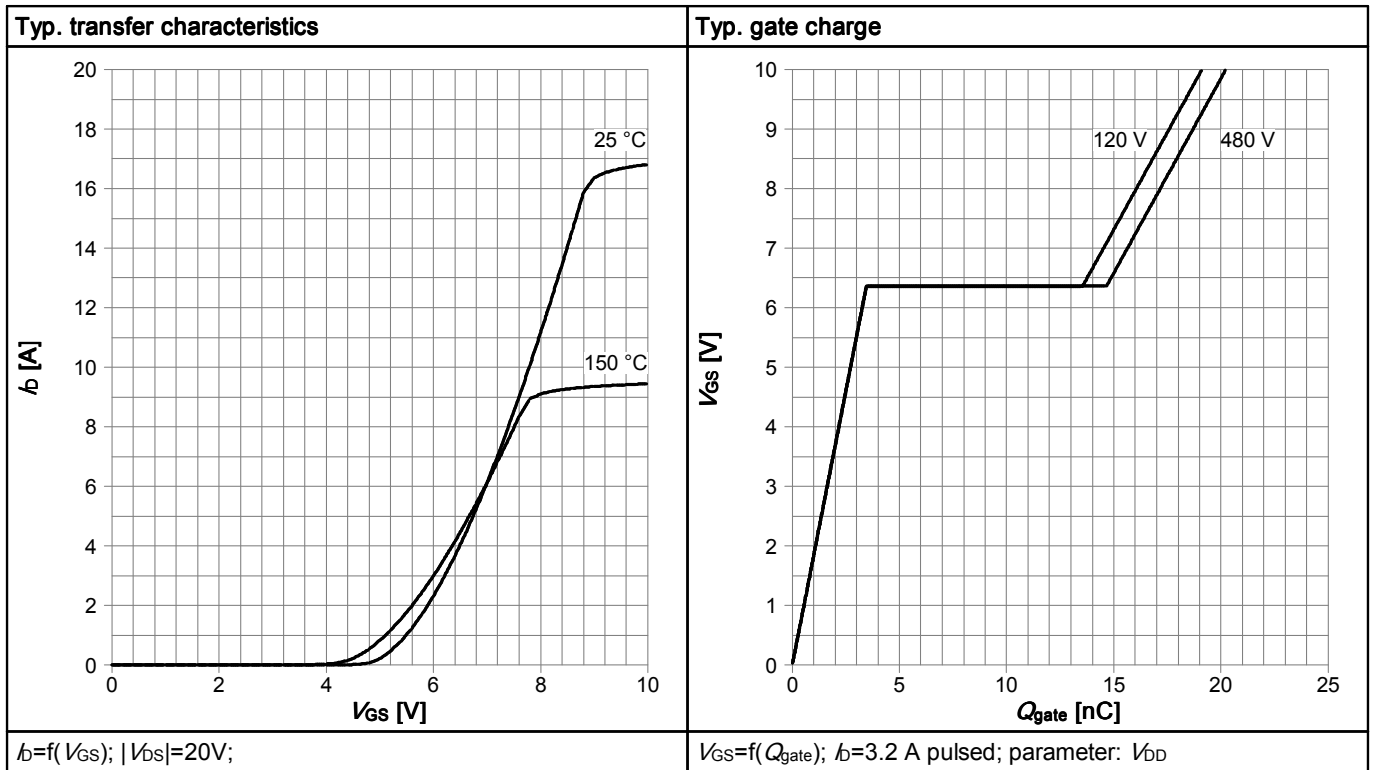


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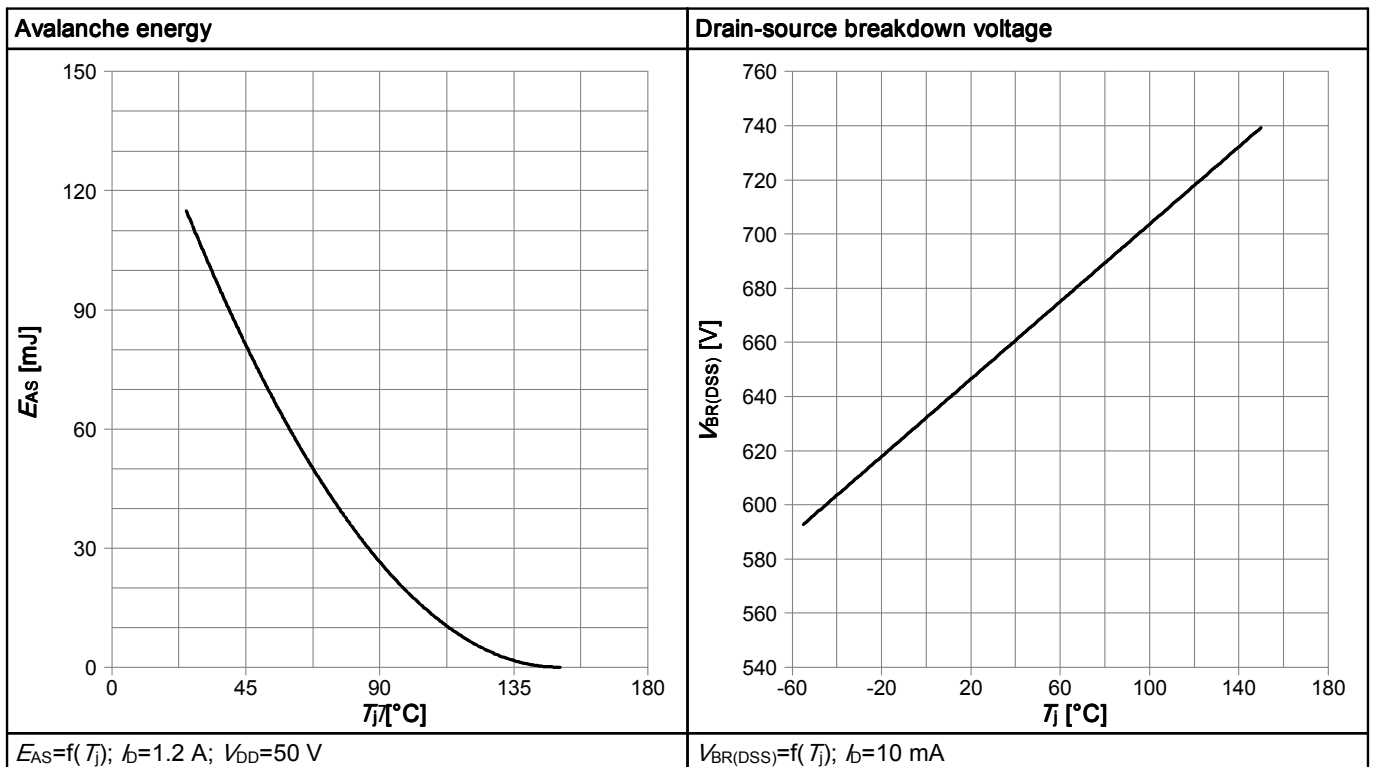


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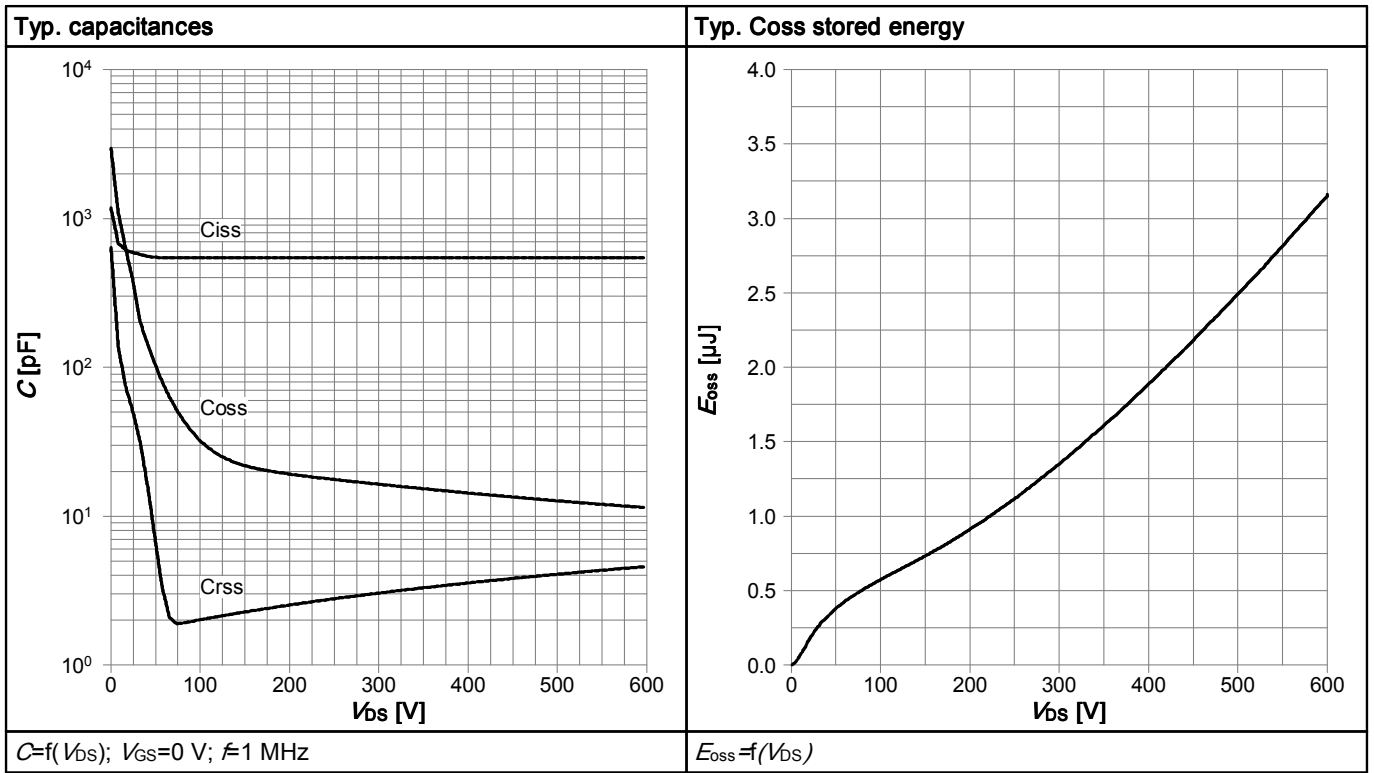
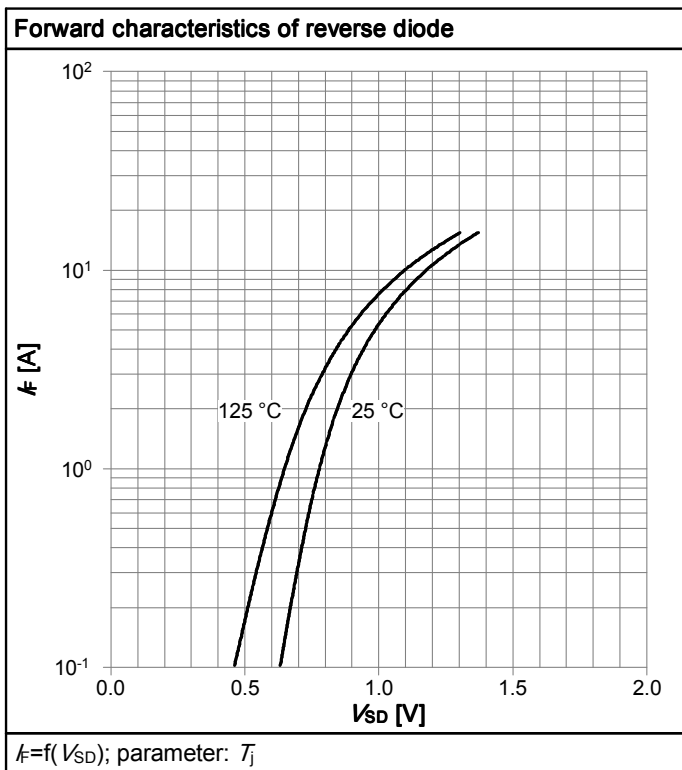


Table 19



6 Test Circuits

Table 20 Diode_characteristics

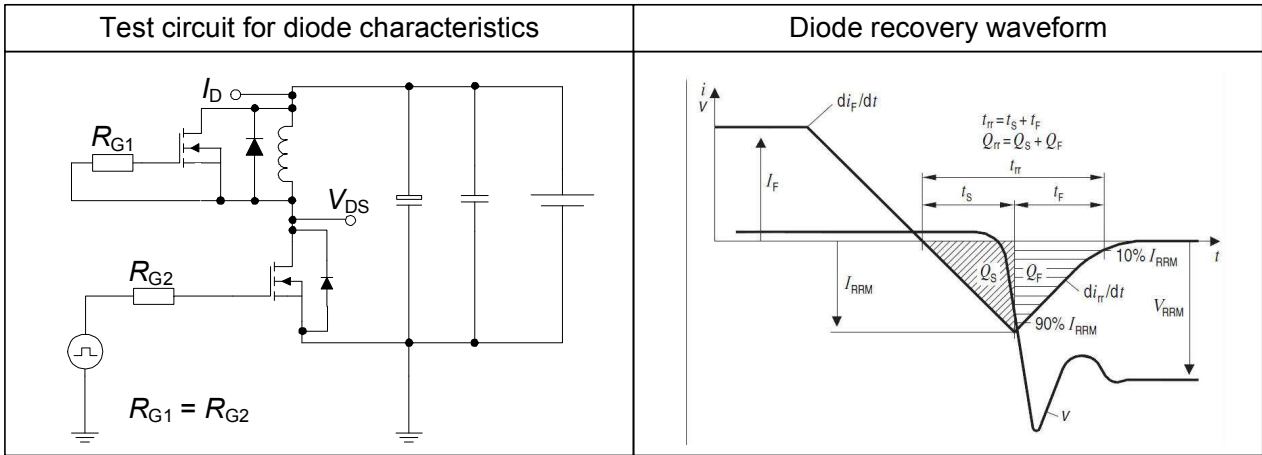


Table 21 Switching_times

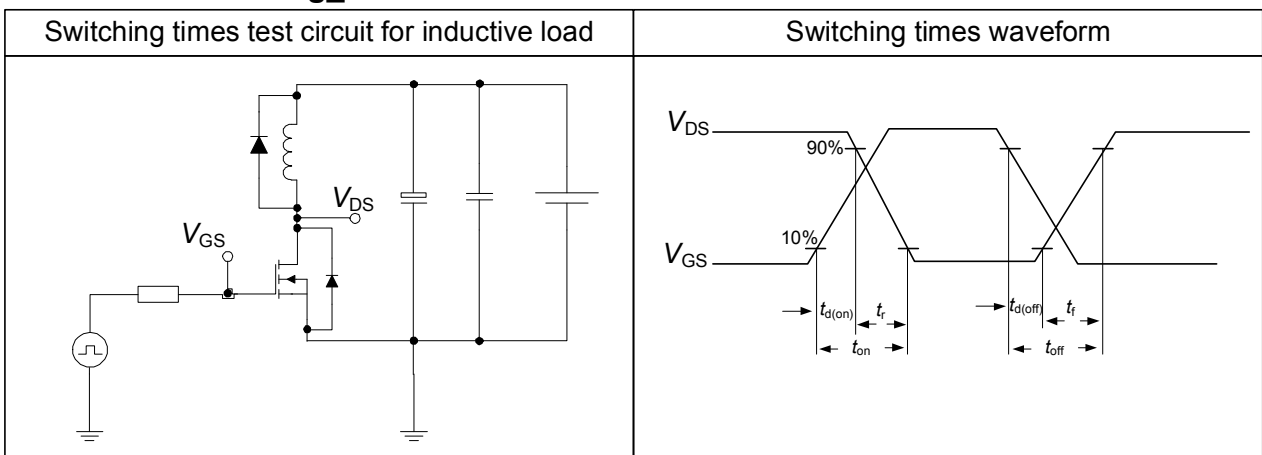
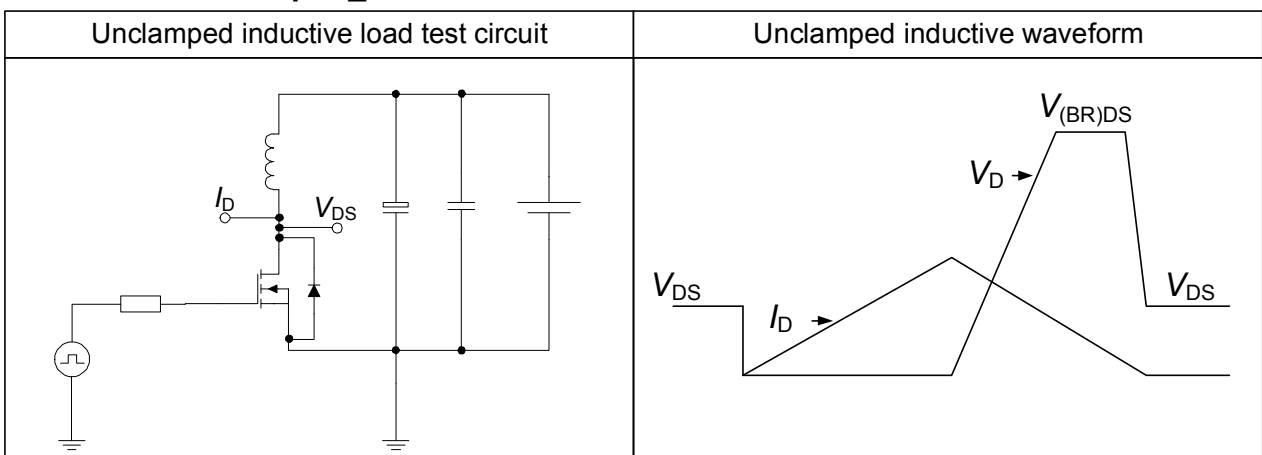


Table 22 Unclamped_inductive



7 Package Outlines

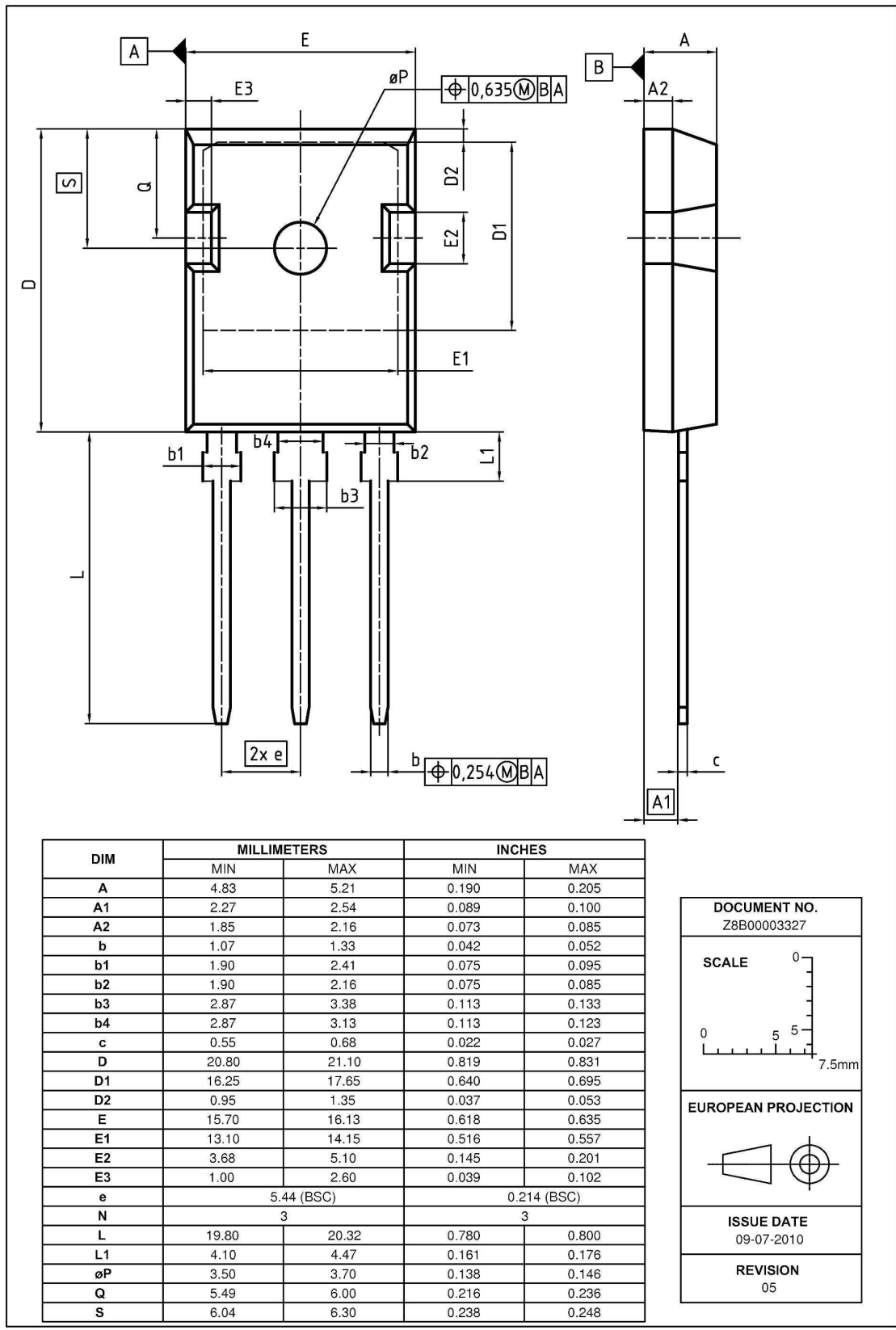


Figure 1 Outline PG-TO 247, dimensions in mm/inches

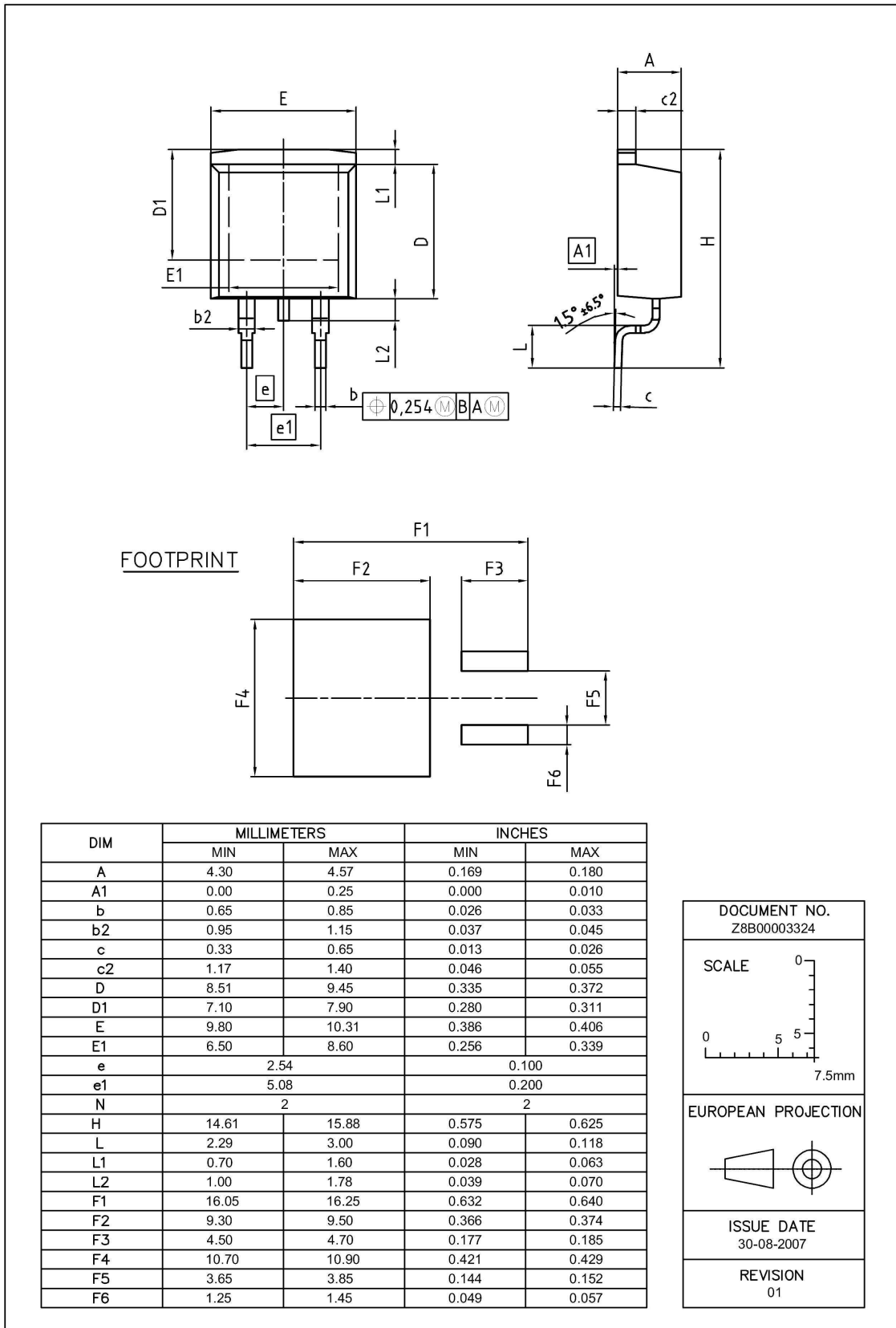


Figure 2 Outline PG-TO 263, dimensions in mm/inches

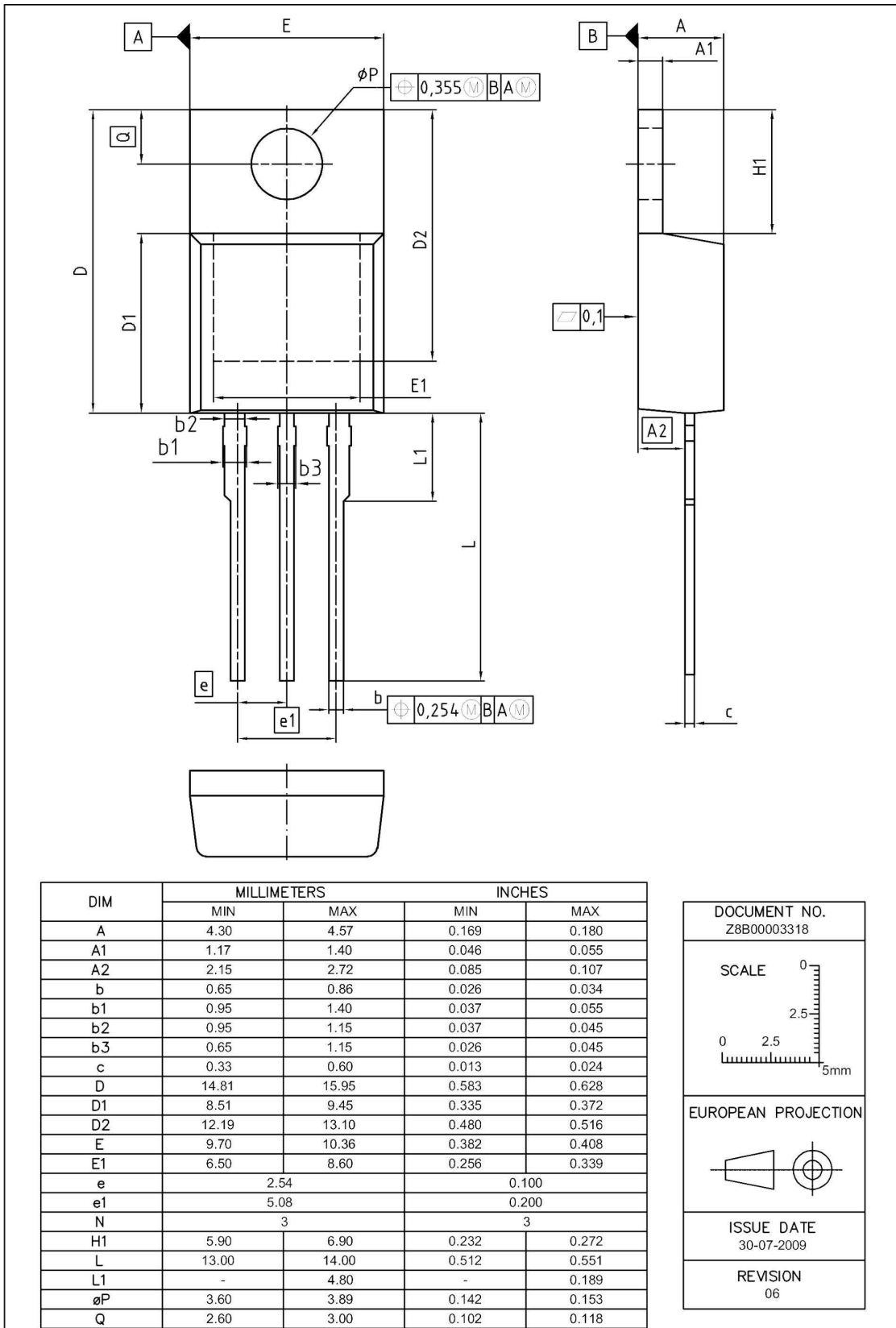


Figure 3 Outline PG-TO 220, dimensions in mm/inches

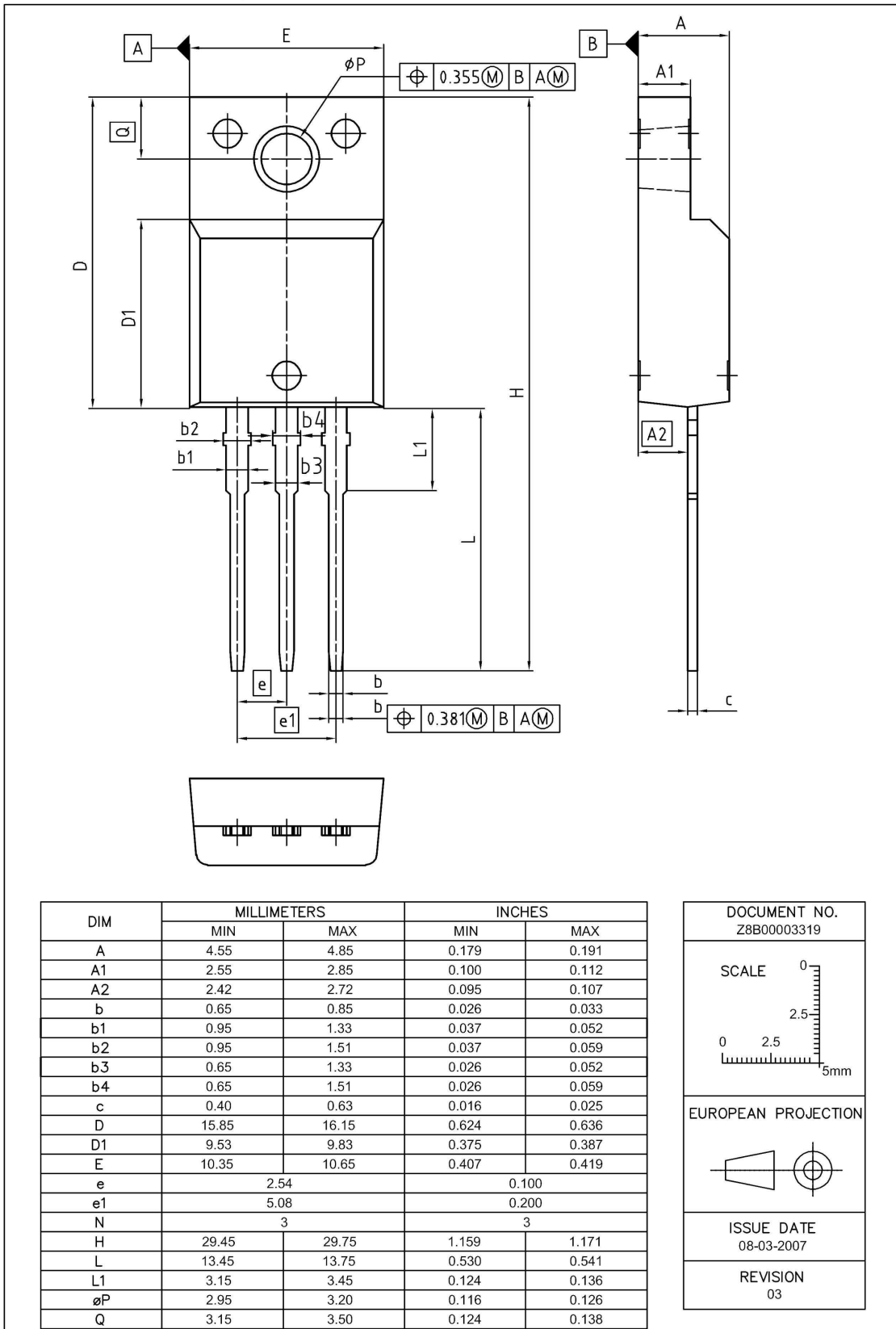
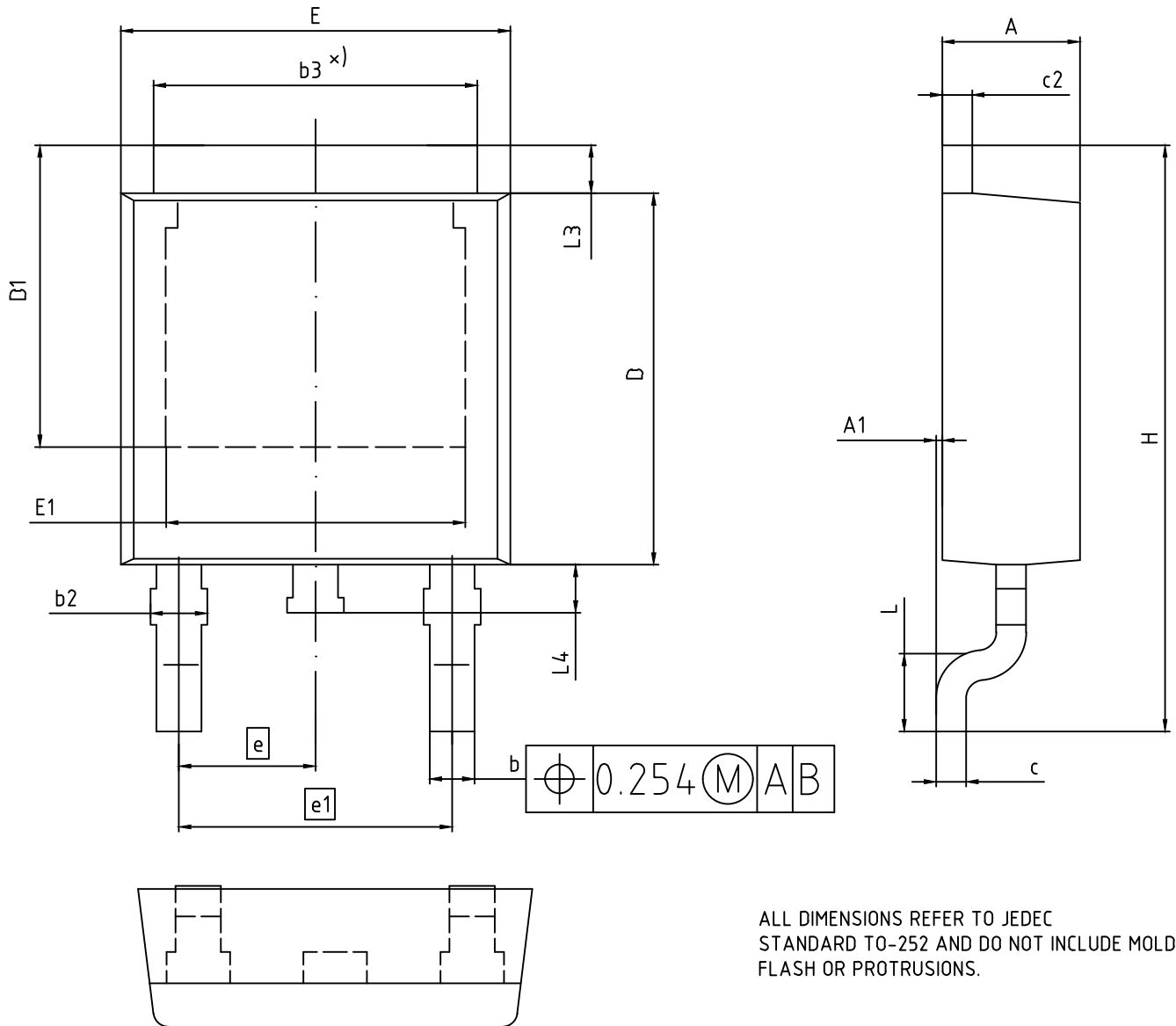


Figure 4 Outline PG-TO 220 FullPAK, dimensions in mm/inches

7 Package Outlines



ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	2.16	2.41
A1	0.00	0.15
b	0.64	0.89
b2	0.65	1.15
b3	4.95	5.50
c	0.46	0.61
c2	0.40	0.98
D	5.97	6.22
D1	5.02	5.84
E	6.35	6.73
E1	4.32	5.50
e	2.29	
e1	4.57	
N	3	
H	9.40	10.48
L	1.18	1.78
L3	0.89	1.27
L4	0.51	1.02

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EUROPEAN PROJECTION
ISSUE DATE 01.04.2020

Figure 5 Outline PG-TO 252, dimensions in mm/inches

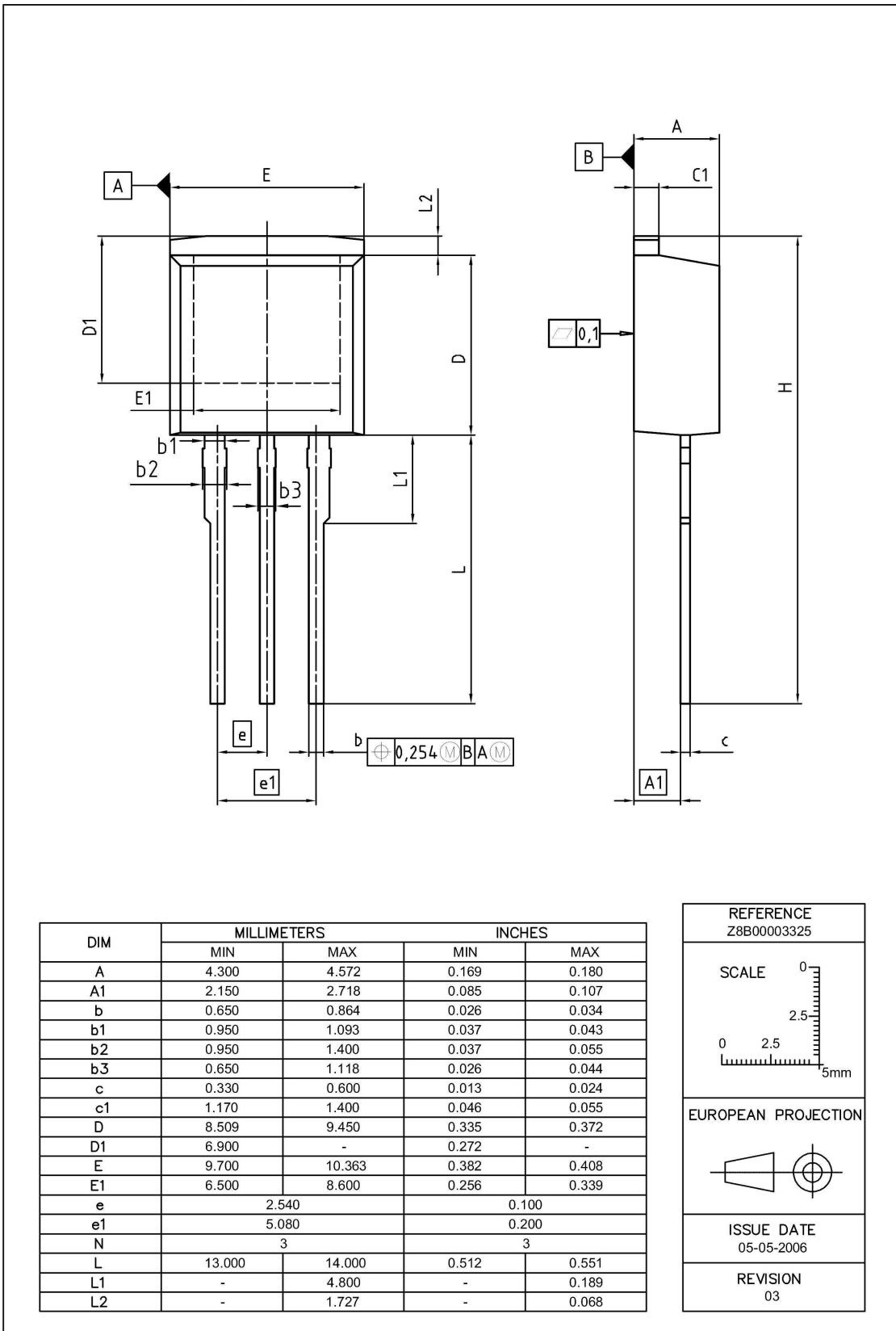


Figure 6 Outline PG-TO 262, dimensions in mm/inches



8 Appendix A

Table 23 Related Links

- **IFX Design Tools:**
<http://www.infineon.com/cms/en/product/promopages/designtools/index.html>
- **IFX CoolMOS Webpage:**
<http://www.infineon.com/cms/en/product/channel.html?channel=ff80808112ab681d0112ab6a628704d8>

Revision History

IPx65R660CFD

Revision: 2020-05-26, Rev. 2.7

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2011-08-29	update to CFD2 standard
2.2	2011-09-15	update pin naming
2.3	2011-09-15	update pin naming
2.4	2011-09-15	release of new pin naming
2.5	2011-09-27	update Igss test condition
2.7	2020-05-26	Update package outline

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