



# LA6541D

## 4-channel Bridge Driver for Compact Discs

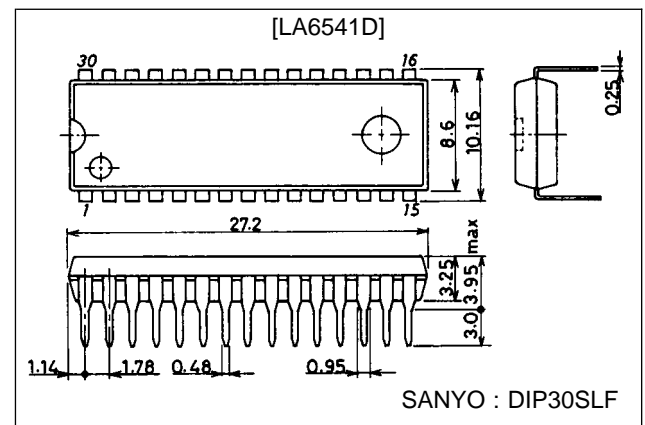
### Functions and Features

- 4-channel bridge (BTL) power amplifier.
- $I_O$  max. 700 mA.
- With mute circuit  
(Affects all amplifier outputs, Amp 1 to Amp 8).  
(When the mute voltage is low, the outputs turn off;  
when the mute voltage is high, the outputs turn on).
- 5.0 V regulator built in (Uses external PNP transistor).
- Reset circuit built in (The reset output delay time can be adjusted through an external capacitor).

### Package Dimensions

unit : mm

#### 3196-DIP30SLF



### Specifications

#### Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max		14	V
Maximum input voltage	$V_{IN}$		13	V
Mute pin voltage	$V_{Mute}$		13	V
Allowable power dissipation	$P_d$ max	When using standard board (material: glass epoxy)	2.5	W
Operating temperature	$T_{opr}$		-20 to +75	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

#### Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Operating voltage	$V_{CC}$		5.6 to 13	V
Reset output source current	$I_{ORH}$		0 to 200	$\mu\text{A}$
Reset output sink current	$I_{ORL}$		0 to 2	mA

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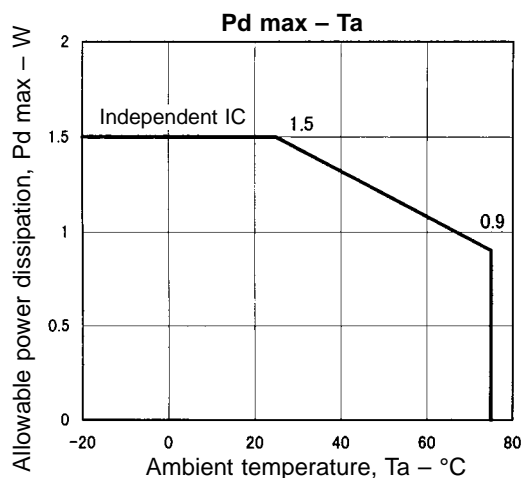
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### Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{CC} = 8.0\text{ V}$ , $V_{REF} = 4\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
No-load current drain	$I_{CC1}$	When all amplifier outputs are on (Mute high)		20	40	mA
	$I_{CC2}$	When all amplifier outputs are off (Mute low)		15	35	mA
Output offset voltage	$V_{OF1}$	Amplifier 1 to 2 ( $V_{O1}$ to $V_{O2}$ ), Amplifier 3 to 4 ( $V_{O3}$ to $V_{O4}$ )	-50		50	mV
	$V_{OF2}$	Amplifier 5 to 6 ( $V_{O5}$ to $V_{O6}$ ), Amplifier 7 to 8 ( $V_{O7}$ to $V_{O8}$ )	-50		50	mV
Buffer amplifier input voltage range	$V_{BIN}$		1.5		$V_{CC}-1.5$	V
Input voltage range	$V_{IN}$		1.0		$V_{CC}-1.5$	V
Output source voltage	$V_{O1}$	Note 1, when $R_L = 8.0\ \Omega$	5.0	5.6		V
Output sink voltage	$V_{O2}$	Note 2, when $R_L = 8.0\ \Omega$		1.8	2.4	V
Closed-circuit voltage gain	$V_G$	Between bridge amplifiers		9		dB
Slew rate	$SR$			0.15		V/ $\mu\text{s}$
Mute on voltage	$V_{Mute}$	Note 3		1.2		V
[Power Supply] (with 2SK632K connected externally)						
Output voltage	$V_{OUT1}$	$I_O = 200\text{ mA}$	4.75	5.0	5.25	V
Line regulation	$\Delta V_{OLN1}$	$5.6 \leq V_{IN1} \leq 12\text{ V}$		20	100	mV
Load regulation	$\Delta V_{OLD1}$	$5\text{ mA} \leq I_O \leq 200\text{ mA}$		50	150	mV
[Reset]						
High reset output voltage	$V_{ORH}$	$I_{ORH} = 200\ \mu\text{A}$ , Cd pin open	4.73	4.98	5.23	V
Low reset output voltage	$V_{ORL}$	$I_{SRL} = 2\text{ mA}$ , Cd is shorted to GND		100	200	mV
Reset threshold voltage	$V_{RT}$	Note 4		4.3		V
Reset hysteresis voltage	$V_{hys}$	Note 5	40	100	200	mV
Reset output delay time	$t_d$	$C_d = 0.1\ \mu\text{F}$		10		ms

Notes:

- Source voltage to ground when an  $8\ \Omega$  load is connected between bridge amplifier outputs.
- Sink voltage to ground when an  $8\ \Omega$  load is connected between bridge amplifier outputs.
- When the mute signal is high, all amplifier outputs turn on, and when low, all amplifier outputs turn off. When the mute signal is low, amplifier output is undefined.
- 5 V supply voltage when the reset output goes low.
- Potential difference from the 5 V supply voltage when the reset output goes low and when it goes high.



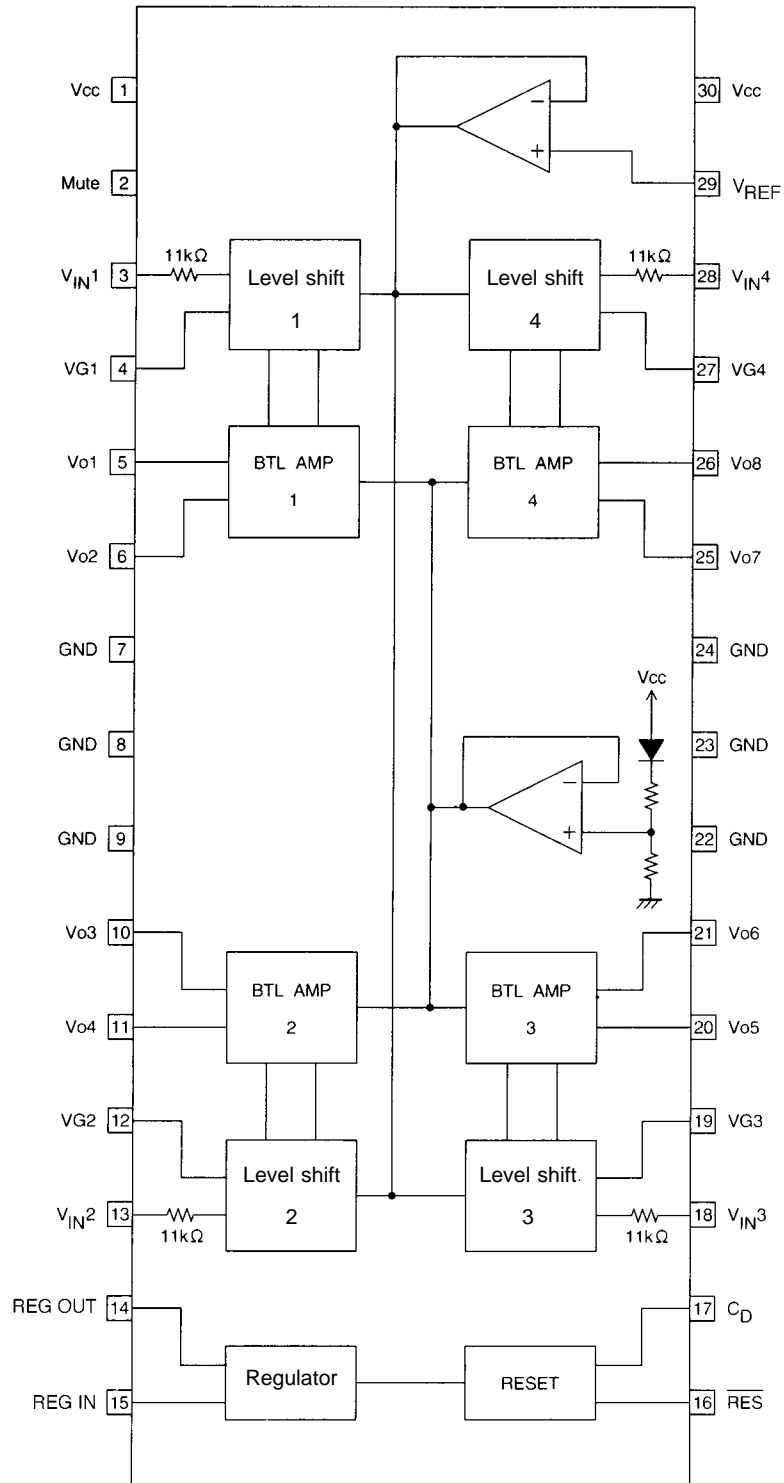
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### Pin Functions

Pin No.	Pin Name	Description (Function)
1	V <sub>CC</sub>	Power supply (shorted with pin 30)
2	Mute	ON/OFF control for all BTL AMP outputs
3	V <sub>IN1</sub>	BTL AMP 1 input
4	VG1	BTL AMP 1 input (for gain control)
5	V <sub>O1</sub>	BTL AMP 1 output (non-inverting side)
6	V <sub>O2</sub>	BTL AMP 1 output (inverting side)
7	GND	GND (minimum electric potential)
8	GND	GND (minimum electric potential)
9	GND	GND (minimum electric potential)
10	V <sub>O3</sub>	BTL AMP 2 output (inverting side)
11	V <sub>O4</sub>	BTL AMP 2 output (non-inverting side)
12	VG2	BTL AMP 2 input (for gain control)
13	V <sub>IN2</sub>	BTL AMP 2 input
14	REG OUT	Connection for collector of external transistor (PNP); 5 V supply output
15	REG IN	Connection for base of external transistor (PNP)
16	$\overline{\text{RES}}$	Reset output
17	C <sub>D</sub>	Reset output delay time setting (with capacitor)
18	V <sub>IN3</sub>	BTL AMP 3 input
19	VG3	BTL AMP 3 input (for gain control)
20	V <sub>O5</sub>	BTL AMP 3 output (non-inverting side)
21	V <sub>O6</sub>	BTL AMP 3 output (inverting side)
22	GND	GND (minimum electric potential)
23	GND	GND (minimum electric potential)
24	GND	GND (minimum electric potential)
25	V <sub>O7</sub>	BTL AMP 4 output (inverting side)
26	V <sub>O8</sub>	BTL AMP 4 output (non-inverting side)
27	VG4	BTL AMP 4 input (for gain control)
28	V <sub>IN4</sub>	BTL AMP 4 input
29	V <sub>REF</sub>	Reference voltage input for level shift circuit
30	V <sub>CC</sub>	Power supply (shorted with pin 1)

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## Pin Assignment (Block Diagram)

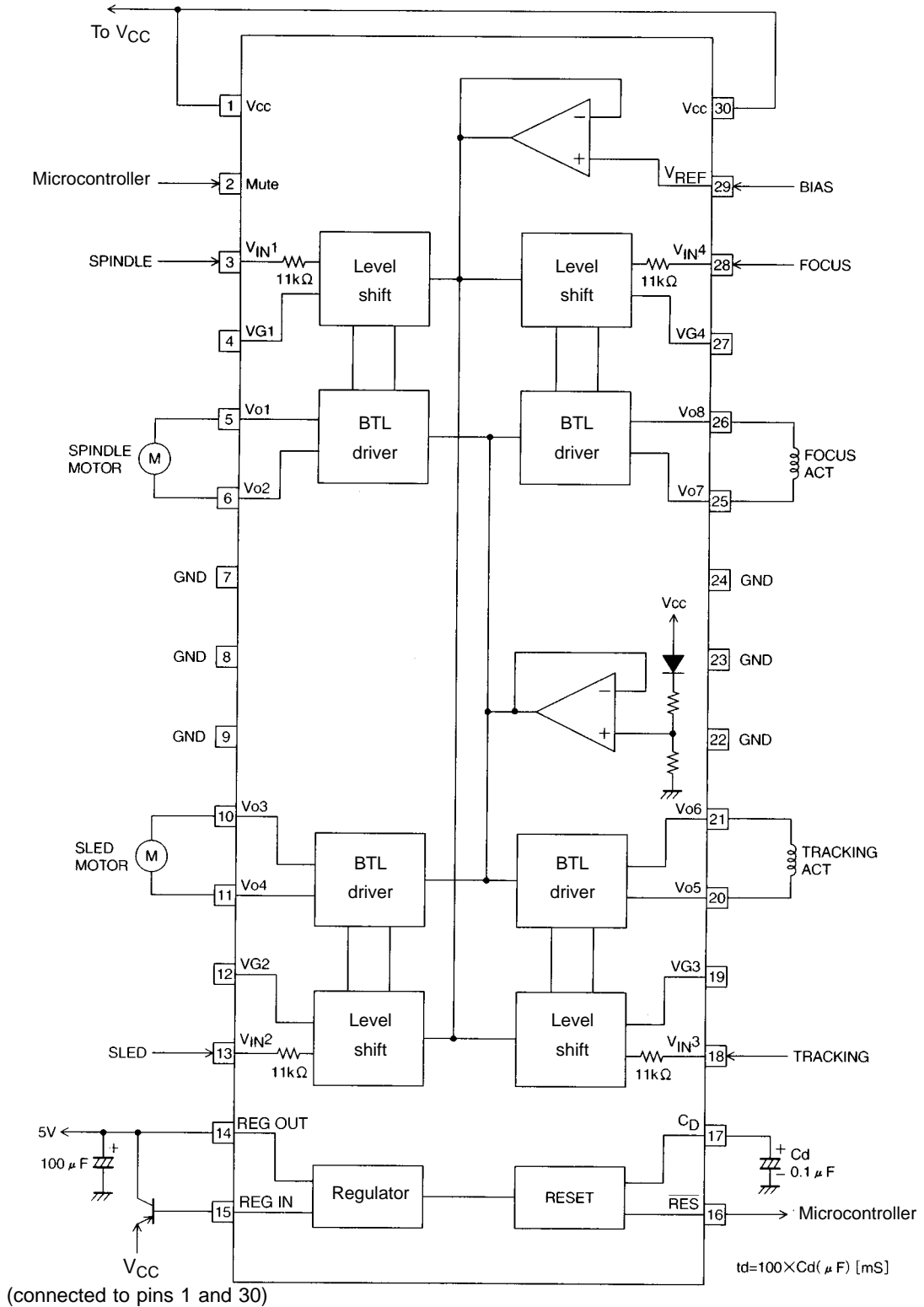


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Top view

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## Sample Application Circuit



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Note: Use a delay capacitor (Cd) whose capacitance does not change much according to the temperature.

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## Pin Functions

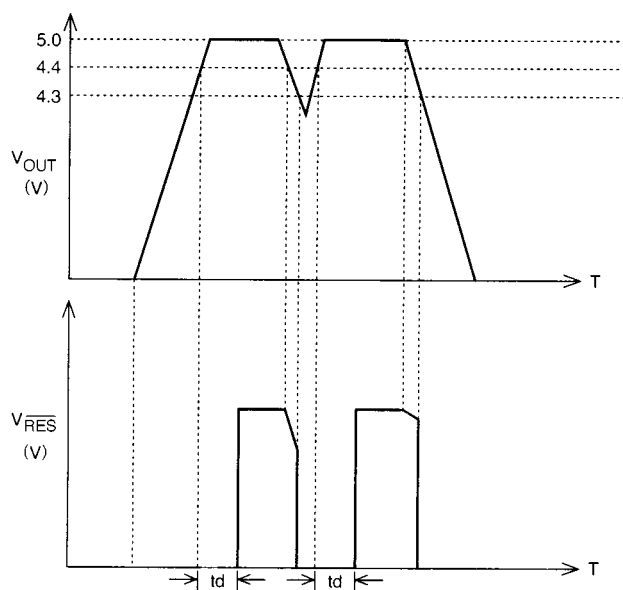
Pin	Name	Pin No.	Equivalent Circuit	Description
Input	V <sub>IN1</sub> V <sub>IN2</sub> V <sub>IN3</sub> V <sub>IN4</sub> VG1 VG2 VG3 VG4	3 13 18 28 4 12 19 27	<p style="text-align: right;">A06424</p>	Input pins
Output	V <sub>O1</sub> , V <sub>O2</sub> V <sub>O3</sub> , V <sub>O4</sub> V <sub>O5</sub> , V <sub>O6</sub> V <sub>O7</sub> , V <sub>O8</sub>	5, 6 10, 11 20, 21 25, 26	<p style="text-align: right;">A06425</p>	Output pins
Mute	Mute	2	<p style="text-align: right;">A06426</p>	Output ON/OFF

## Truth Table

Input	MUTE	CH1		CH2		CH3		CH4	
		V <sub>O1</sub> (Amp1)	V <sub>O2</sub> (Amp2)	V <sub>O3</sub> (Amp3)	V <sub>O4</sub> (Amp4)	V <sub>O5</sub> (Amp5)	V <sub>O6</sub> (Amp6)	V <sub>O7</sub> (Amp7)	V <sub>O8</sub> (Amp8)
H	H	H	L	L	H	H	L	L	H
	L	—	—	—	—	—	—	—	—
L	H	L	H	H	L	L	H	H	L
	L	—	—	—	—	—	—	—	—

\* The “—” symbol means “undefined.”

## Reset Operation



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