22 W BTL or 2 × 11 W stereo power amplifier

TDA1519C

FEATURES

- Requires very few external components for Bridge-Tied Load (BTL)
- Stereo or BTL application
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/standby switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Pin compatible with TDA1519B (TDA1519C and TDA1519CSP).

GENERAL DESCRIPTION

The TDA1519C is an integrated class-B dual output amplifier in a 9-lead plastic single in-line (SIL) power or 20-lead heatsink small outline package.

For the TDA1519CTH (SOT418-2) the heatsink is positioned on top of the package, thereby allowing an external heatsink to be mounted on top. The heatsink of the TDA1519CTD (SOT397-1) is facing the PCB thereby allowing the heatsink to be soldered on the copper area of the PCB.

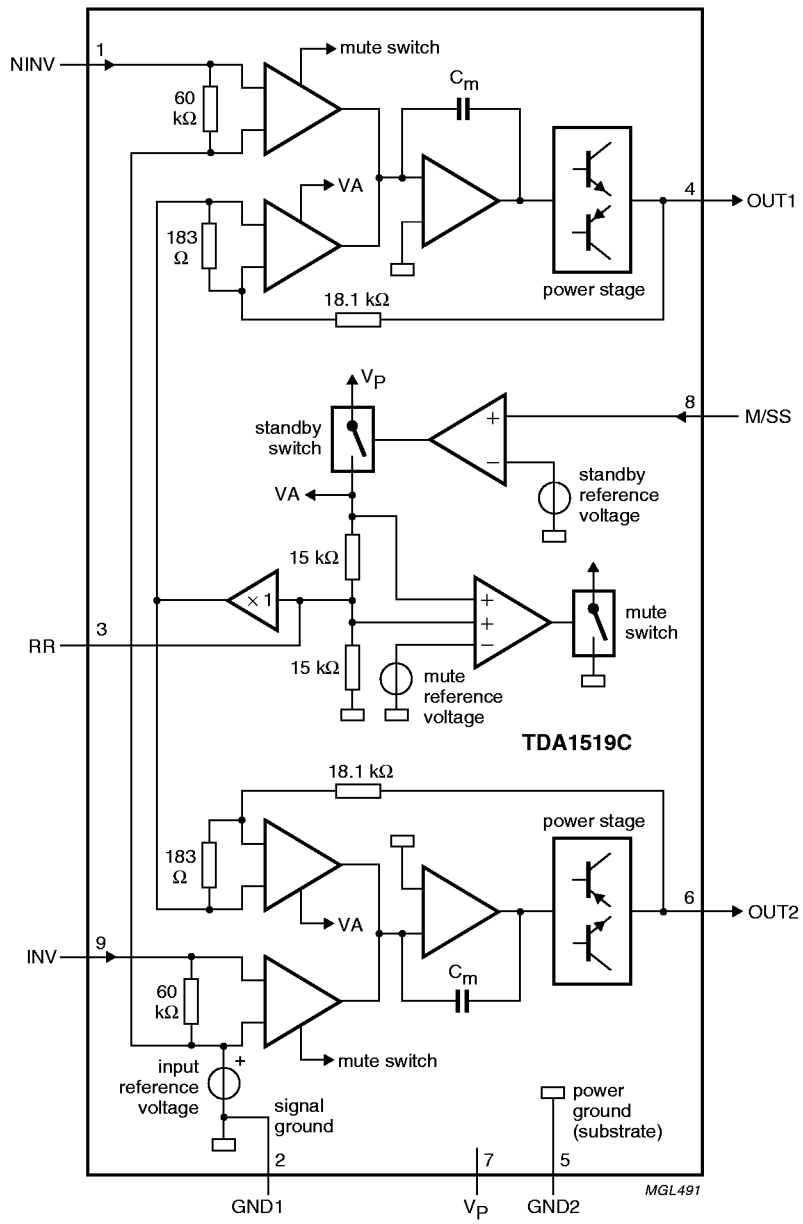
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1519C	SIL9P	plastic single in-line power package; 9 leads	SOT131-2
TDA1519CSP	SMS9P	plastic surface mounted single in-line power package; 9 leads	SOT354-1
TDA1519CTH	HSOP20	heatsink small outline package; 20 leads; low stand-off	SOT418-2
TDA1519CTD	HSOP20	heatsink small outline package; 20 leads	SOT397-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage	operating	6.0	14.4	17.5	V
		non-operating	–	–	30	V
		load dump protected	–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current		–	40	80	mA
I_{stb}	standby current		–	0.1	100	μA
$I_{sw(on)}$	switch-on current		–	–	40	μA
Inputs						
$\lvert Z_i \rvert$	input impedance	BTL	25	–	–	kΩ
		stereo	50	–	–	kΩ
Stereo application						
P_o	output power	THD = 10%				
		R_L = 4 Ω	–	6	–	W
		R_L = 2 Ω	–	11	–	W
α_{cs}	channel separation		40	–	–	dB
$V_{n(o)(rms)}$	noise output voltage (RMS value)		–	150	–	μV
BTL application						
P_o	output power	THD = 10%; R_L = 4 Ω	–	22	–	W
SVRR	supply voltage ripple rejection	R_S = 0 Ω				
		f = 100 Hz	34	–	–	dB
		f = 1 to 10 kHz	48	–	–	dB
$\lvert \Delta V_{OO} \rvert$	DC output offset voltage		–	–	250	mV
T_j	junction temperature		–	–	150	°C

BLOCK DIAGRAM



The pin numbers refer to the TDA1519C and TDA1519CSP.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN			DESCRIPTION
	TDA1519C; TDA1519CSP	TDA1519CTD	TDA1519CTH	
NINV	1	19	2	non-inverting input
GND1	2	20	1	ground 1 (signal)
RR	3	1	20	supply voltage ripple rejection
OUT1	4	3	18	output 1
GND2	5	5	16	ground 2 (substrate)
OUT2	6	8	13	output 2
V_P	7	10	11	positive supply voltage
M/SS	8	11	10	mute/standby switch input
INV	9	12	9	inverting input
n.c.	–	2, 4, 6, 7, 9 and 13 to 18	3 to 8, 12, 14, 15, 17 and 19	not connected

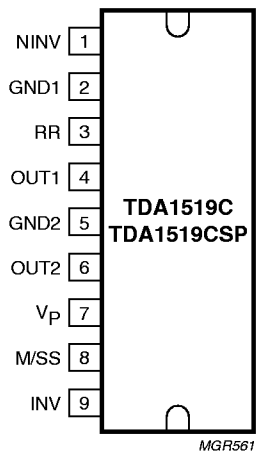


Fig.2 Pin configuration (SOT131-2 and 354-1).

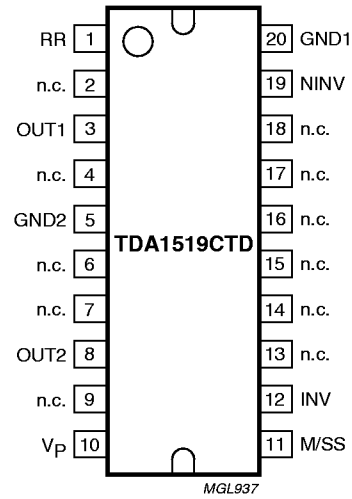


Fig.3 Pin configuration (SOT397-1).

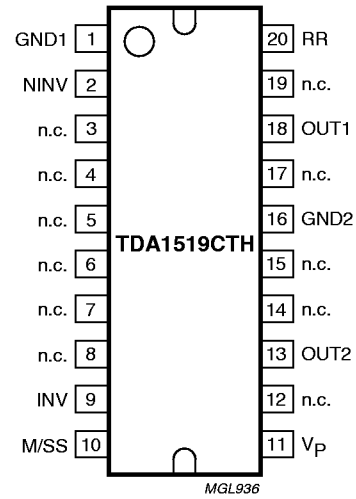


Fig.4 Pin configuration (SOT418-2).

FUNCTIONAL DESCRIPTION

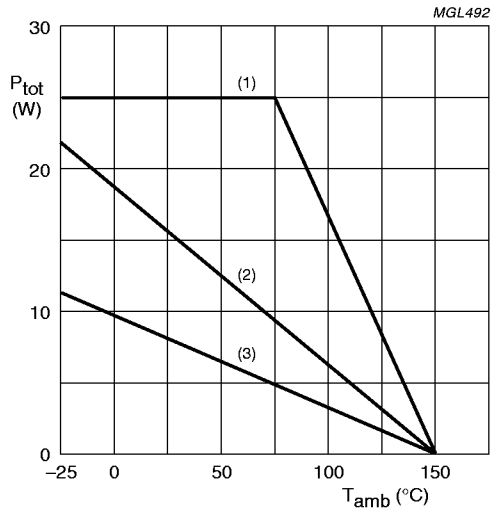
The TDA1519C contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/standby switch which has the following features:

- Low standby current (<100 μA)
- Low mute/standby switching current (low cost supply switch)
- Mute condition.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	–	17.5	V
		non-operating	–	30	V
		load dump protected; during 50 ms; $t_r \geq 2.5$ ms	–	45	V
V_{sc}	AC and DC short-circuit-safe voltage		–	17.5	V
V_{rp}	reverse polarity voltage		–	6	V
	energy handling capability at outputs	V_P = 0 V	–	200	mJ
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
P_{tot}	total power dissipation	see Fig.5	–	25	W
T_j	junction temperature		–	150	°C
T_{stg}	storage temperature		–55	+150	°C



(1) Infinite heatsink.
(2) $R_{th(c-a)}$ = 5 K/W.
(3) $R_{th(c-a)}$ = 13 K/W.

Fig.5 Power derating curve for SIL9P.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA1519C		40	K/W
	TDA1519CTH and TDA1519CTD		40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case			
	TDA1519C		3	K/W
	TDA1519CTH and TDA1519CTD		3	K/W

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage	note 1	6.0	14.4	17.5	V
$I_{q(tot)}$	total quiescent current		–	40	80	mA
V_O	DC output voltage	note 2	–	6.95	–	V
$\lvert\Delta V_{OO}\rvert$	DC output offset voltage		–	–	250	mV
Mute/standby switch						
$V_{sw(on)}$	switch-on voltage level		8.5	–	–	V
Mute condition						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	–	–	20	mV
$\lvert\Delta V_{OO}\rvert$	DC output offset voltage		–	–	250	mV
Standby condition						
V_{stb}	standby voltage	standby mode	0	–	2	V
I_{stb}	standby current	standby mode	–	–	100	μA
$I_{sw(on)}$	switch-on current		–	12	40	μA

Notes

1. The circuit is DC adjusted at V_P = 6 to 17.5 V and AC operating at V_P = 8.5 to 17.5 V.
2. At V_P = 17.5 to 30 V, the DC output voltage $\leq 0.5V_P$.

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo application (see Fig.6)						
P_o	output power	note 1				
		THD = 0.5%	4	5	–	W
		THD = 10%	5.5	6.0	–	W
		R_L = 2 Ω; note 1				
		THD = 0.5%	7.5	8.5	–	W
		THD = 10%	10	11	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
$f_{ro(l)}$	low frequency roll-off	−3 dB; note 2	–	45	–	Hz
$f_{ro(h)}$	high frequency roll-off	−1 dB	20	–	–	kHz
$G_{v(cl)}$	closed-loop voltage gain		39	40	41	dB
SVRR	supply voltage ripple rejection	on; notes 3 and 4	40	–	–	dB
		on; notes 3 and 5	45	–	–	dB
		mute; notes 3 and 6	45	–	–	dB
		standby; notes 3 and 6	80	–	–	dB
$\lvert Z_i \rvert$	input impedance		50	60	75	kΩ
$V_{n(o)(rms)}$	noise output voltage (RMS value)	note 7				
		on; R_S = 0 Ω	–	150	–	μV
		on; R_S = 10 kΩ	–	250	500	μV
		mute; note 8	–	120	–	μV
α_{cs}	channel separation	R_S = 10 kΩ	40	–	–	dB
$\lvert \Delta G_{v(ub)} \rvert$	channel unbalance		–	0.1	1	dB
BTL application (see Fig.7)						
P_o	output power	note 1				
		THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
	output power at V_P = 13.2 V	note 1				
		THD = 0.5%	–	13	–	W
		THD = 10%	–	17.5	-	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
B_p	power bandwidth	THD = 0.5%; P_o = −1 dB; with respect to 15 W	–	35 to 15000	–	Hz
$f_{ro(l)}$	low frequency roll-off	−1 dB; note 2	–	45	–	Hz
$f_{ro(h)}$	high frequency roll-off	−1 dB	20	–	–	kHz
$G_{v(cl)}$	closed-loop voltage gain		45	46	47	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SVRR	supply voltage ripple rejection	on; notes 3 and 4	34	–	–	dB
		on; notes 3 and 5	48	–	–	dB
		mute; notes 3 and 6	48	–	–	dB
		standby; notes 3 and 6	80	–	–	dB
$\lvert Z_i \rvert$	input impedance		25	30	38	kΩ
$V_{n(o)(rms)}$	noise output voltage (RMS value)	note 7				
		on; R_S = 0 Ω	–	200	–	μV
		on; R_S = 10 kΩ	–	350	700	μV
		mute; note 8	–	180	–	μV

Notes

1. Output power is measured directly at the output pins of the IC.
2. Frequency response externally fixed.
3. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
4. Frequency f = 100 Hz.
5. Frequency between 1 and 10 kHz.
6. Frequency between 100 Hz and 10 kHz.
7. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
8. Noise output voltage independent of R_S (V_i = 0 V).

APPLICATION INFORMATION

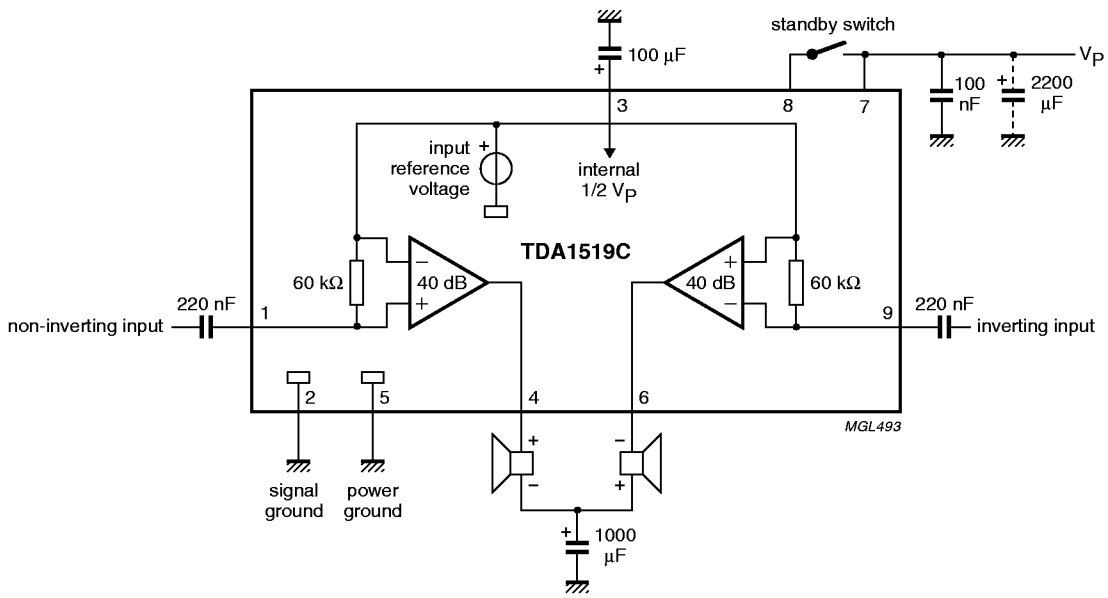


Fig.6 Stereo application diagram (SOT131-2 and SOT354-1).

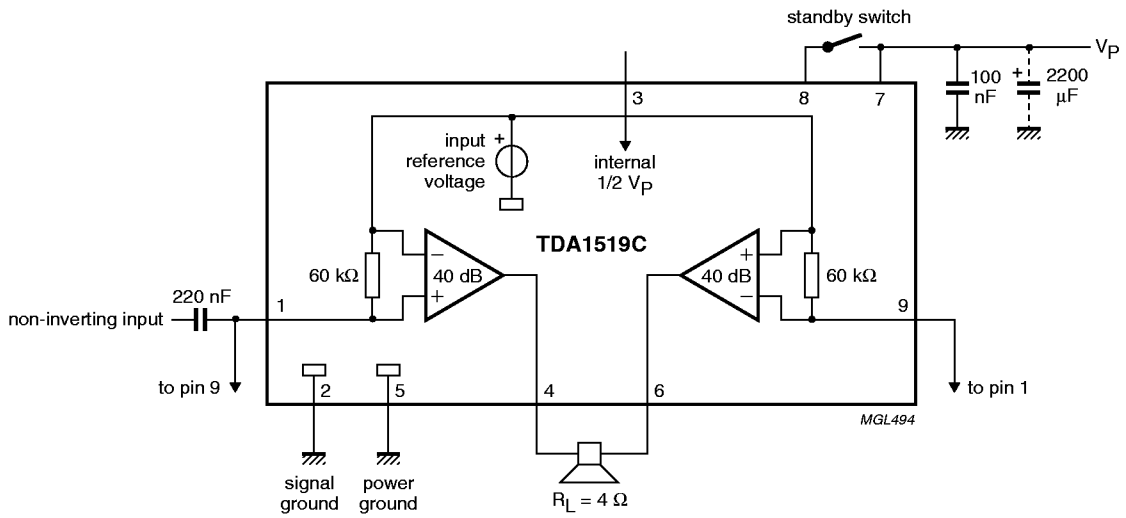


Fig.7 BTL application diagram (SOT131-2 and SOT354-1).

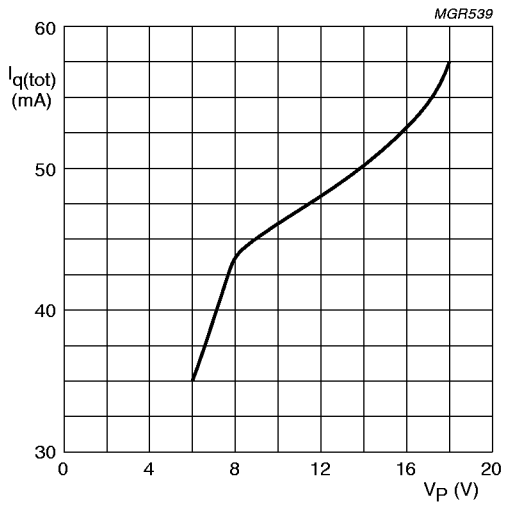


Fig.8 Total quiescent current ($I_{q(tot)}$) as a function of supply voltage (V_P).

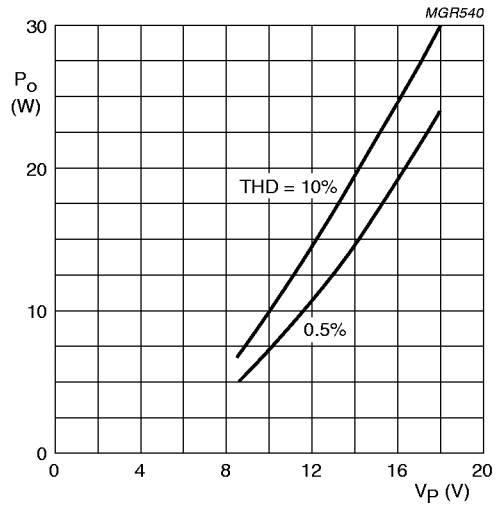


Fig.9 Output power (P_o) as a function of supply voltage (V_P) for BTL application at $R_L = 4\ \Omega$; f = 1 kHz.

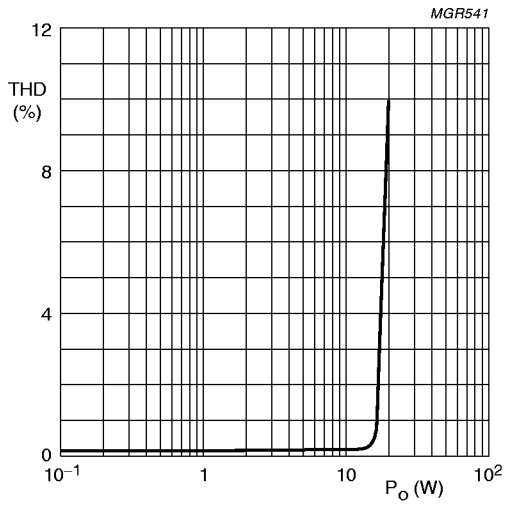


Fig.10 Total harmonic distortion (THD) as a function of output power (P_o) for BTL application at R_L = 4 Ω; f = 1 kHz.

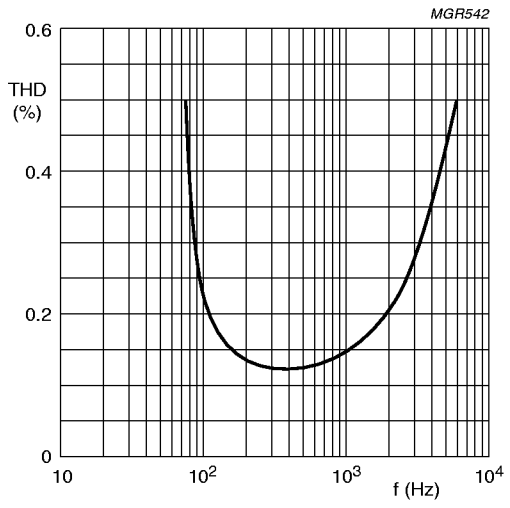
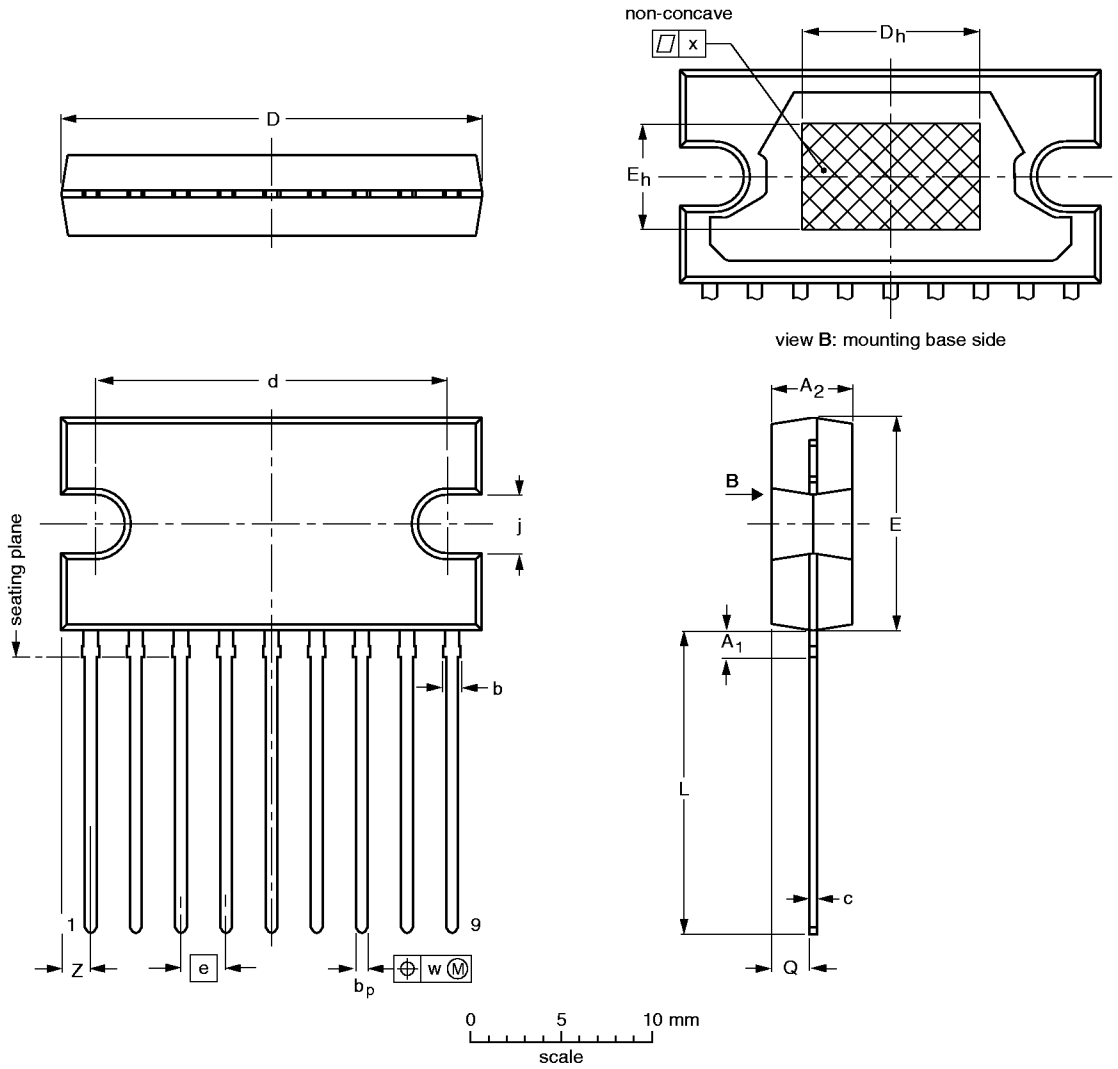


Fig.11 Total harmonic distortion (THD) as a function of operating frequency (f) for BTL application at R_L = 4 Ω; P_o = 1 W.

PACKAGE OUTLINES

SIL9P: plastic single in-line power package; 9 leads **SOT131-2**



DIMENSIONS (mm are the original dimensions)

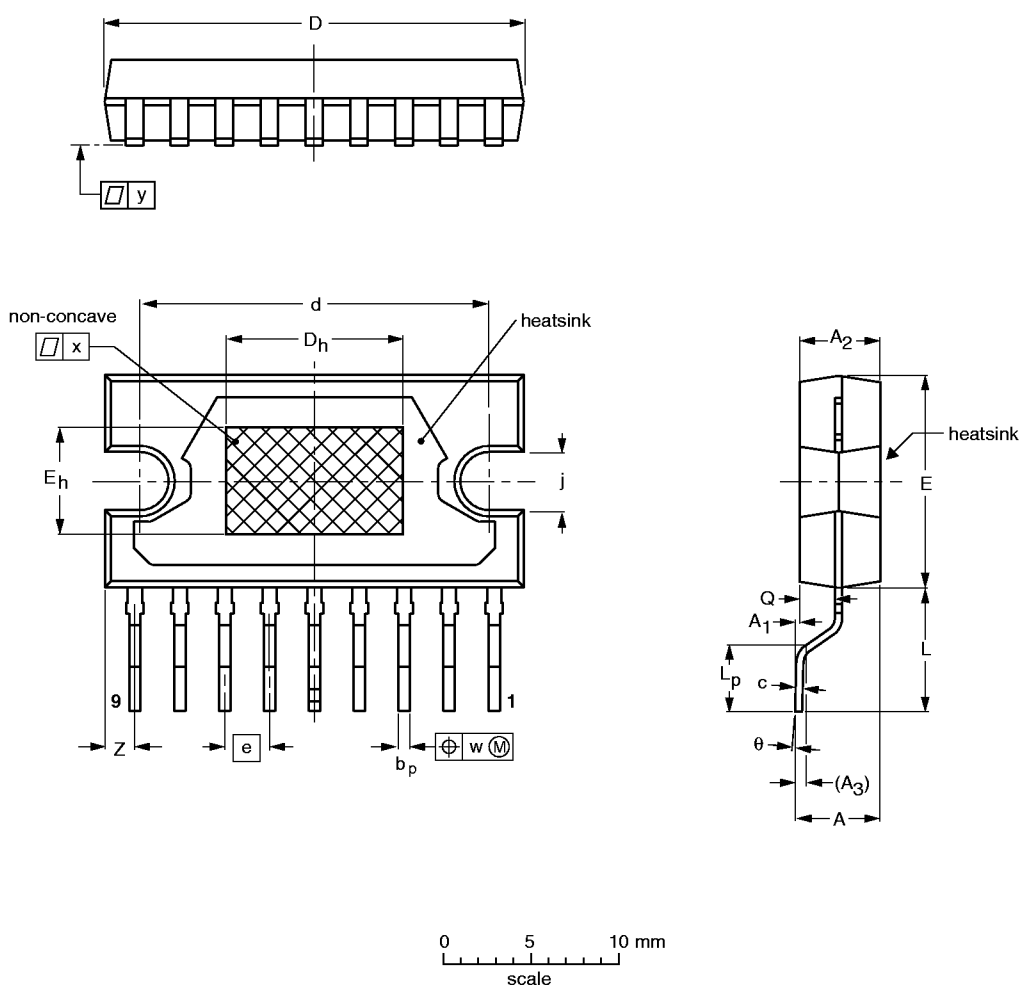
UNIT	A_1 max.	A_2	b max.	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	E_h	j	L	Q	w	x	$Z^{(1)}$
mm	2.0	4.6 4.4	1.1	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	17.2 16.5	2.1 1.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT131-2						~~95-03-11~~ 99-12-17

SMS9P: plastic surface mounted single in-line power package; 9 leads **SOT354-1**



DIMENSIONS (mm are the original dimensions)

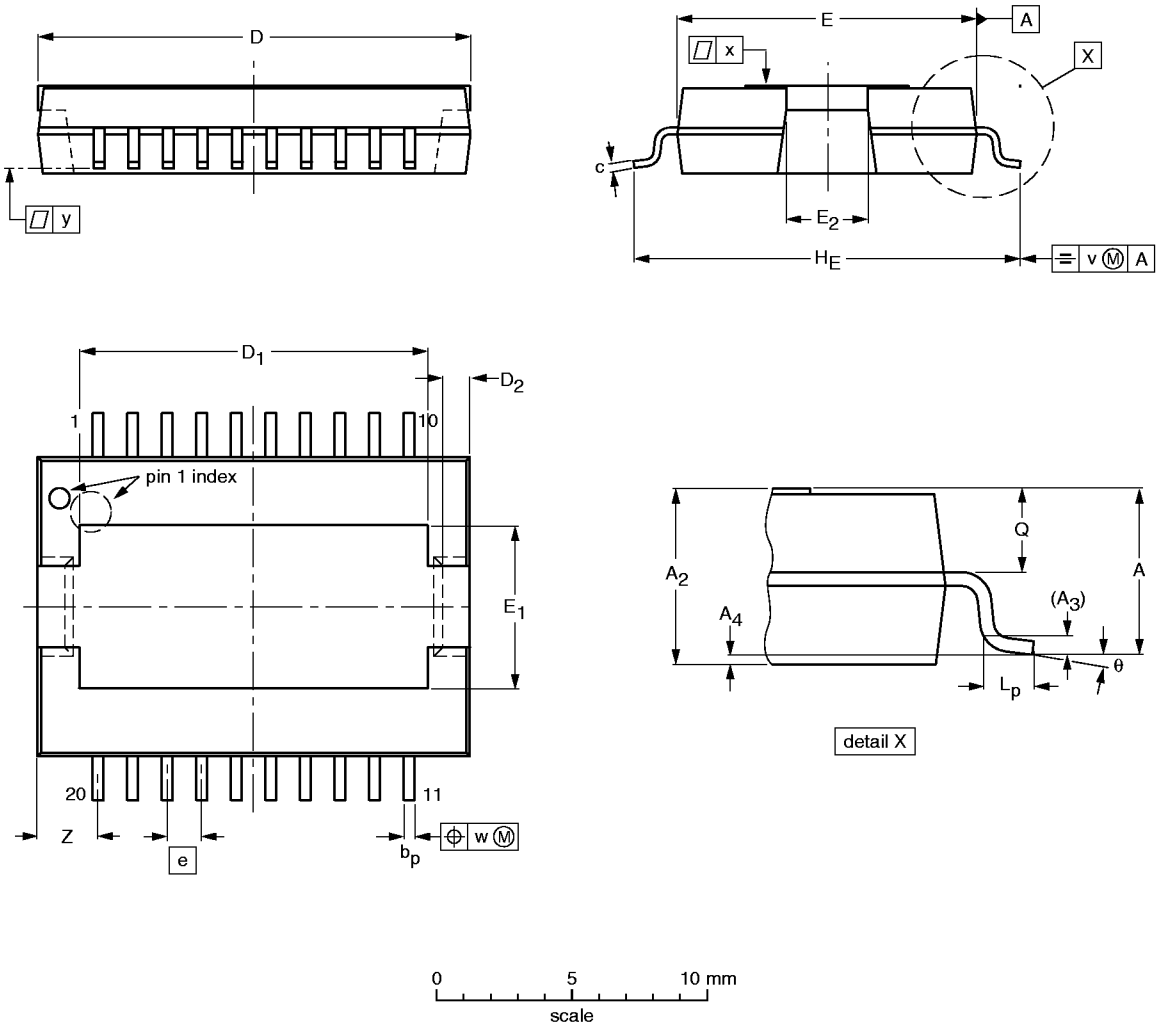
UNIT	A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	E_h	j	L	L_p	Q	w	x	y	$Z^{(1)}$	θ
mm	4.9 4.2	0.35 0.05	4.6 4.4	0.25	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	7.4 6.6	3.4 2.8	2.1 1.9	0.25	0.03	0.15	2.00 1.45	3° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT354-1						~~98-10-08~~ 99-12-17

HSOP20: plastic, heatsink small outline package; 20 leads; low stand-off height **SOT418-2**



DIMENSIONS (mm are the original dimensions)

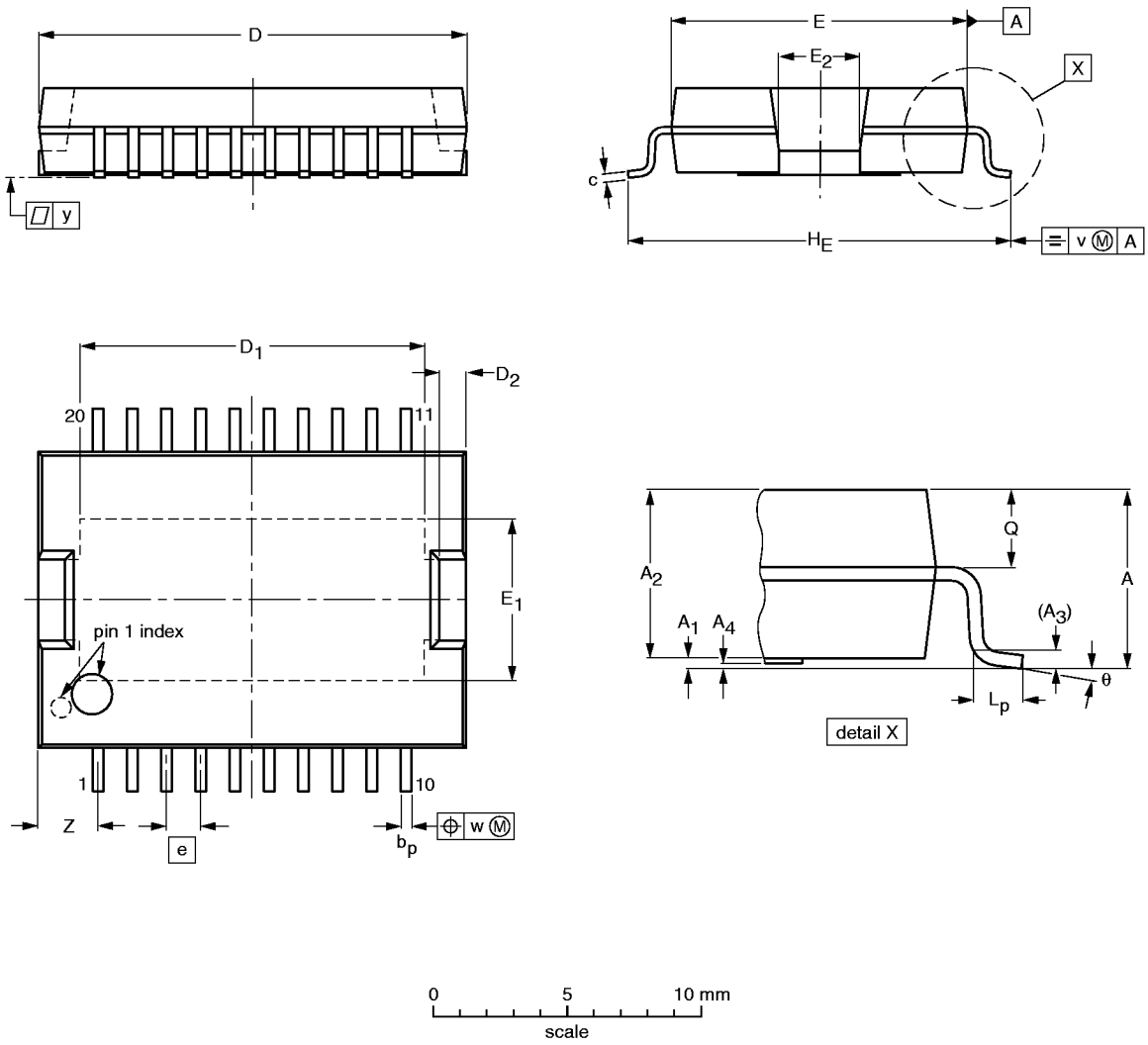
UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.12 −0.02	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.5 2.0	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT418-2						~~98-02-25~~ 99-11-12

HSOP20: plastic, heatsink small outline package; 20 leads **SOT397-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	A_4	b_p	c	$D^{(1)}$	D_1	D_2	$E^{(1)}$	E_1	E_2	e	H_E	L_p	Q	v	w	y	Z	θ
mm	3.6	0.3 0.1	3.3 3.0	0.35	0.1 0	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.5 1.4	0.25	0.25	0.1	2.5 2.0	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT397-1						~~97-11-03~~ 99-11-12

SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW(1)	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable(2)	–	suitable
Surface mount	BGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(3)	suitable	–
	PLCC(4), SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended(4)(5)	suitable	–
	SSOP, TSSOP, VSO	not recommended(6)	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.