ELECTRONIC GLOBAL

# EG8025 Datasheet

Single Phase SPWM controller

# Revision History

| Version | Date | Description |
|---|---|---|
| V1.0 | 2019-10-12 | Creation |
| | | |
| | | |

# Contents

# EG8025 Datasheet V1.0

## 1. Features

- Current-Mode SPWM controller, Center-aligned PWM modulation mode, can carry resistive, inductive and capacitive loads
- 20KHz Modulation frequency，suitable for IGBT and power MOSFET applications
- Integrated with two 600V half bridge gate drivers, +2A source/-2A sink output current capability per channel
- Provides independent four channels current protection circuit for IGBT/MOSFET, and four comparator with 200mV reference source, which are used for peak current limitation of H-bridge's IGBT/MOSFET
- Built in four high-speed OPamps and one high-speed comparator, two of OPamps are used for load current feedback, one for AC voltage feedback, another for short circuit protection, one of comparator is used for over current protection
- AC output voltage and output current are processed in each cycle of PWM，can achieve fast load response
- Integrated synchronous zero-crossing signal output and configurable 0-degree/120-degree phase tracking, can realize the function of three-phase inverter through ZC signal cascade
- Support for multi-inverter parallel applications
- Settable functions via pins
  - H-bridge control signal interchange for left and right bridge
  - 4 settings of dead time are 300nS,500nS,1uS,1.5uS
  - 2 settings of output frequency are 50Hz,60Hz
  - Soft start enable and disable
- The protection functions
  - Over voltage and under voltage protection for DC bus
  - Over load protection
  - Over current protection
  - One channel of over temperature protection for PCB space, another is for IGBT
  - Short circuit protection
- Settable parameters via UART
  - 50Hz output frequency
  - 60Hz output frequency
  - AC output voltage
  - Over temperature protection value
  - Rated power protection value
  - Rated current protection value
  - Fault reset
- Readable parameters via UART
  - AC output voltage
  - AC output frequency
  - AC output power

- AC output current
- DC bus voltage
- Fault code

# 2. Description

EG8025 is a digital pure sine wave inverter ASIC (Application Specific Integrated Circuit) that uses current-mode SPWM controlling, center-aligned PWM modulation and built-in two 600V half bridge gate drivers, which is dedicated to power inverter products.

EG8025 is a CMOS IC that integrates SPWM sinusoid generator, dead time control circuit, output voltage and output current feedback circuit, protection circuit, UART serial communication, and etc.

EG8025 is available in an 80-Pin LQFP80 package, requiring a minimum number of external components to implement power inverter functions.it has high output voltage accuracy, output harmonic distortion is less than 1.5% at light load, and output harmonic distortion is less than 3% at heavy load, which can meet the waveform requirement of the inverter products.

Integrated with two 600V half bridge gate drivers, +2A source/-2A sink output current capability per channel. Built in four independent cycle by cycle edge-triggered shutdown logic, which can effectively prevent excessive peak current damaging IGBT/MOSFET in extreme cases. Built in two SD pins SD1 and SD2, and SD1 is shutdown input pin of gate driver 1 for HO1 and LO1, and SD2 is shutdown input pin of gate driver 2 for HO2 and LO2,which can be implemented short circuit protection by SD1 and SD2 pins.

EG8025 provides various protection functions, such as over voltage and under voltage for DC bus, over load, over current, over temperature, short circuit, and etc.

EG8025 provides two UART serial ports. User can set parameters or reset AC output through the UART serial ports, and can also read the running status and related data of inverter through the UART serial ports.

EG8025 supports the function of group three-phase inverter, which is through AC zero-crossing signal output and synchronous phase signal input, as well as ZC(zero-crossing) signal cascade and optocoupler isolator circuit.

# 3. Applications

- Single-Phase sinusoid inverter
- Three-Phase sinusoid inverter
- UPS(Uninterruptible power supply)
- Solar power generation inverter
- Wind power generation inverter
- Digital generator
- Energy storage power

# 4. Pinouts

## 4.1 Pin map

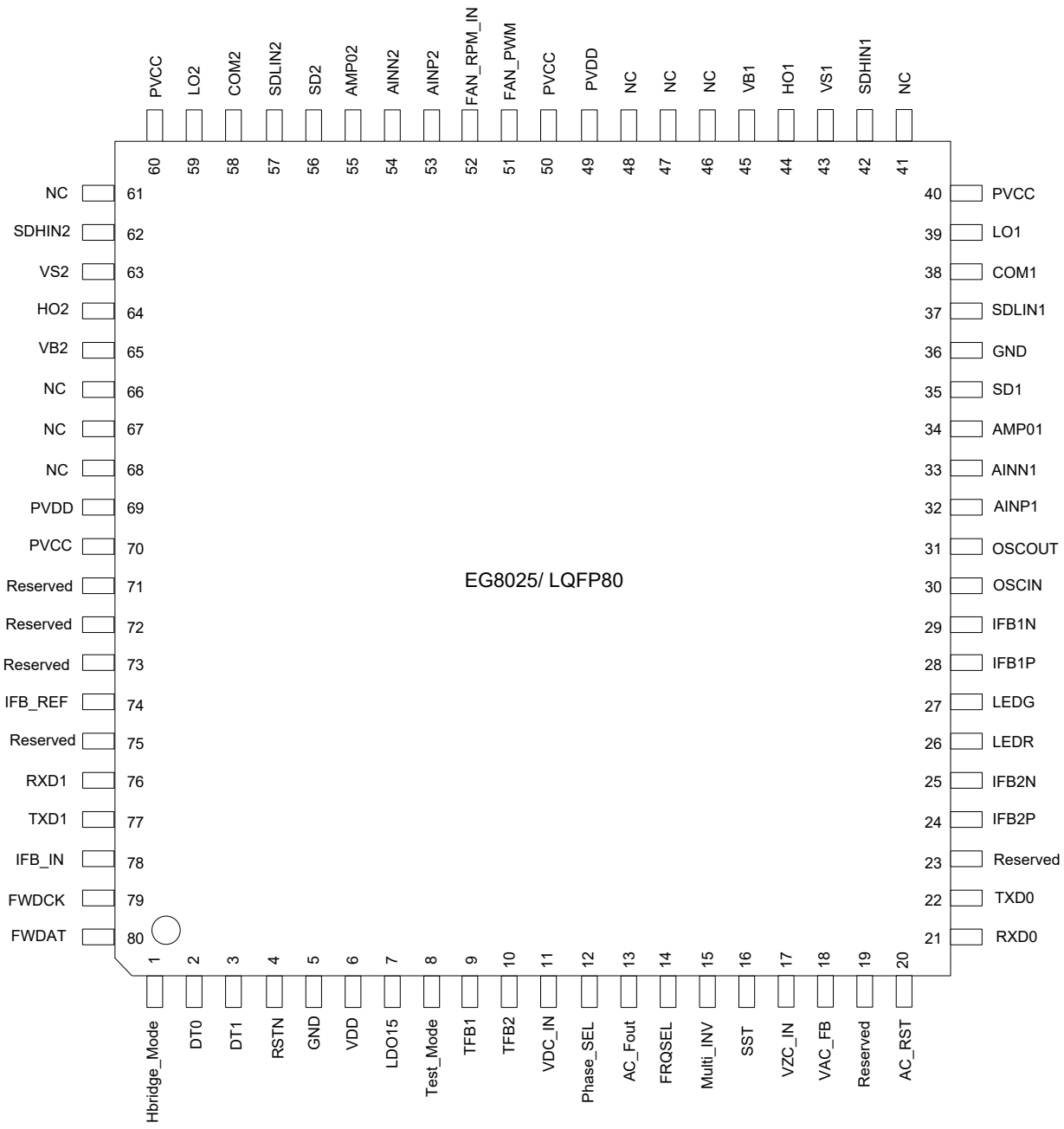



Figure 4-1. EG8025 pin map

## 4.2 Pin Descriptions

| Designator | Name | I/O | Description |
|---|---|---|---|
| 1 | HBridge_Mode | I | H-bridge control signal interchange for left and right bridge |
| 2 | DT0 | I | DT1(Pin3),DT0（Pin2）:Dead time setup<br>“00”:300nS<br>“01”:500nS<br>“10”:1.0uS<br>“11”:1.5uS |
| 3 | DT1 | I | |
| 4 | RSTN | I | Reset input, active-low available |
| 5 | GND | GND | Analog ground |
| 6 | VDD | Power | +5V Power supply input |
| 7 | LDO15 | Power | +1.5V Supply voltage output, requiring an external 1uF capacitor |
| 8 | Test_Mode | I | Test_Mode setup(it cannot be left floating）<br>“0” : Normal mode<br>“1” :Test Mode, SPWM open-loop output for debugging external circuits |
| 9 | TFB1 | I | Temperature feedback input 1.When TFB1 input is higher than 3V,it will cause over temperature protection |
| 10 | TFB2 | I | Temperature feedback input 2.When TFB2 input is higher than 3V,it will cause over temperature protection |
| 11 | VDC_IN | I | DC bus voltage feedback input. When VDC_IN input is lower than 1.8V or higher than 2.8V, it will cause under voltage or over voltage protection of the DC bus. |
| 12 | Phase_SEL | I | Phase Selection input for zero-crossing synchronization or 120-degree phase delay processing<br>“0”:zero-crossing synchronization, which can realize the application of parallel or the host of group three-phase inverter<br>“1”:120 degree phase delay processing after zero-crossing input,<br>which is only for group three-phase inverter |
| 13 | AC_Fout | O | Zero-crossing output signal |
| 14 | FRQSEL | I | AC output frequency select(it cannot be left floating)<br>“0”:50Hz<br>“1”:60Hz |
| 15 | Multi_INV | I | Single/Multiple Inverters select(it cannot be left floating)<br>“0”: It is applied to single inverter or the host of Multi-inverters<br>“1”: It is applied to inverters in parallel or group three-phase inverter through the combination with the pin 12. See Figure 10.a and Fig10.b |

| | | | |
|---|---|---|---|
| 16 | SST | I | Soft start enable<br>“0”:disable<br>“1”:Enable, and one second soft start time |
| 17 | VZC_IN | I | Zero-crossing signal input(it cannot be left floating) |
| 18 | VAC_FB | I | AC output voltage feedback input |
| 19 | Reserved | - | Reserved |
| 20 | AC_RST | I | Enable/Disable AC output voltage (it cannot be left floating)<br>"0":Disable<br>"1":Enable |
| 21 | RXD0 | I | UART0 data receiver (it cannot be left floating) |
| 22 | TXD0 | O | UART0 data transmitter |
| 23 | Reserved | - | Reserved |
| 24 | IFB2P | I | Non-inverting input to the internal operation amplifier 2 for AC current sense 2 |
| 25 | IFB2N | I | Inverting input to the internal operation amplifier 2 for AC current sense 2 |
| 26 | LEDR | O | Fault LED indication |
| 27 | LEDG | O | Running LED indication |
| 28 | IFB1P | I | Non-inverting input to the internal operation amplifier 1 for AC current sense 1 |
| 29 | IFB1N | I | Inverting input to the internal operation amplifier 1 for AC current sense 1 |
| 30 | OSC_IN | I | 4M extern crystal oscillator input |
| 31 | OSC_OUT | O | 4M extern crystal oscillator output |
| 32 | AINP1 | I | Non-inverting input terminal of operation amplifier of internal gate driver 1 |
| 33 | AINN1 | I | Inverting input terminal of operation amplifier of internal gate driver 1 |
| 34 | AMP01 | O | Output terminal of operation amplifier of internal gate driver 1 |
| 35 | SD1 | I | Shutdown input pin for gate driver 1 |
| 36 | GND | GND | Analog ground of internal gate driver 1 |
| 37 | SDLIN1 | I | Peak current limitation input to gate driver 1 for low side MOSFET, with internal reference voltage 200mV |
| 38 | COM1 | I | Low side return of gate driver 1 |
| 39 | LO1 | O | Output of gate driver 1 for low side MOSFET |
| 40 | PVCC | Power | +15V Power supply voltage input for gate driver 1, the voltage range is from 10V to 20V |
| 41 | NC | - | Not connect |
| 42 | SDHIN1 | I | Peak current limitation input to gate driver 1 for high side MOSFET, with internal reference voltage 200mV |
| 43 | VS1 | O | High side bootstrap return of gate driver 1 |

| | | | |
|---|---|---|---|
| 44 | HO1 | O | Output of gate driver 1 for high side MOSFET |
| 45 | VB1 | Power | Bootstrap supply of gate driver 1,requiring an external 10uF Capacitor |
| 46 | NC | - | Not connect for pins isolation |
| 47 | NC | - | Not connect for pins isolation |
| 48 | NC | - | Not connect for pins isolation |
| 49 | PVDD | Power | +5V Power supply voltage input for gate drive 1 |
| 50 | PVCC | Power | +15V Power supply voltage input for gate driver 1, the voltage range is from 10V to 20V |
| 51 | FAN_PWM | O | Control FAN signal output |
| 52 | FAN_RPM_IN | I | Fan speed signal input(it cannot be left floating) |
| 53 | AINP2 | I | Non-inverting input terminal of operation amplifier of internal gate driver 2 |
| 54 | AINN2 | I | Inverting input terminal of operation amplifier of internal gate driver 2 |
| 55 | AMP02 | O | Output terminal of operation amplifier of internal gate driver 2 |
| 56 | SD2 | I | Shutdown input pin for gate driver 2 |
| 57 | SDLIN2 | I | Peak current limitation input to gate driver 2 for low side MOSFET, with internal reference voltage 200mV |
| 58 | COM2 | GND | Low side return of gate driver 2 |
| 59 | LO2 | O | Output of gate driver 2 for low side MOSFET |
| 60 | PVCC | Power | +15V Power supply voltage input for gate driver 2, the voltage range is from 10V to 20V |
| 61 | NC | - | Not connect for pins isolation |
| 62 | SDHIN2 | I | Peak current limitation input to gate driver 2 for low side MOSFET, with internal reference voltage 200mV |
| 63 | VS2 | O | High side bootstrap return of gate driver 2 |
| 64 | HO2 | O | Output of gate driver 2 for high side MOSFET |
| 65 | VB2 | Power | Bootstrap supply of gate driver 2,requiring an external 10uF Capacitor |
| 66 | NC | - | Not connect for pins isolation |
| 67 | NC | - | Not connect for pins isolation |
| 68 | NC | - | Not connect for pins isolation |
| 69 | PVDD | Power | +5V Power supply voltage input for gate drive 2 |
| 70 | PVCC | Power | +15V Power supply voltage input for gate driver 2, the voltage range is from 10V to 20V |
| 71 | Reserved | - | Reserved |
| 72 | Reserved | - | Reserved |
| 73 | Reserved | - | Reserved |
| 74 | IFB_REF | I | External over current reference voltage input |
| 75 | Reserved | - | Reserved |

| | | | |
|---|---|---|---|
| 76 | RXD1 | I | UART1 data receiver (it cannot be left floating) |
| 77 | TXD1 | O | UART1 data transmitter |
| 78 | IFB_IN | I | External current signal input |
| 79 | FWCLK | I | Firmware update clock port |
| 80 | FWDAT | I | Firmware update data port |

# 5. Block Diagram

## 5.1 EG8025 Block Diagram

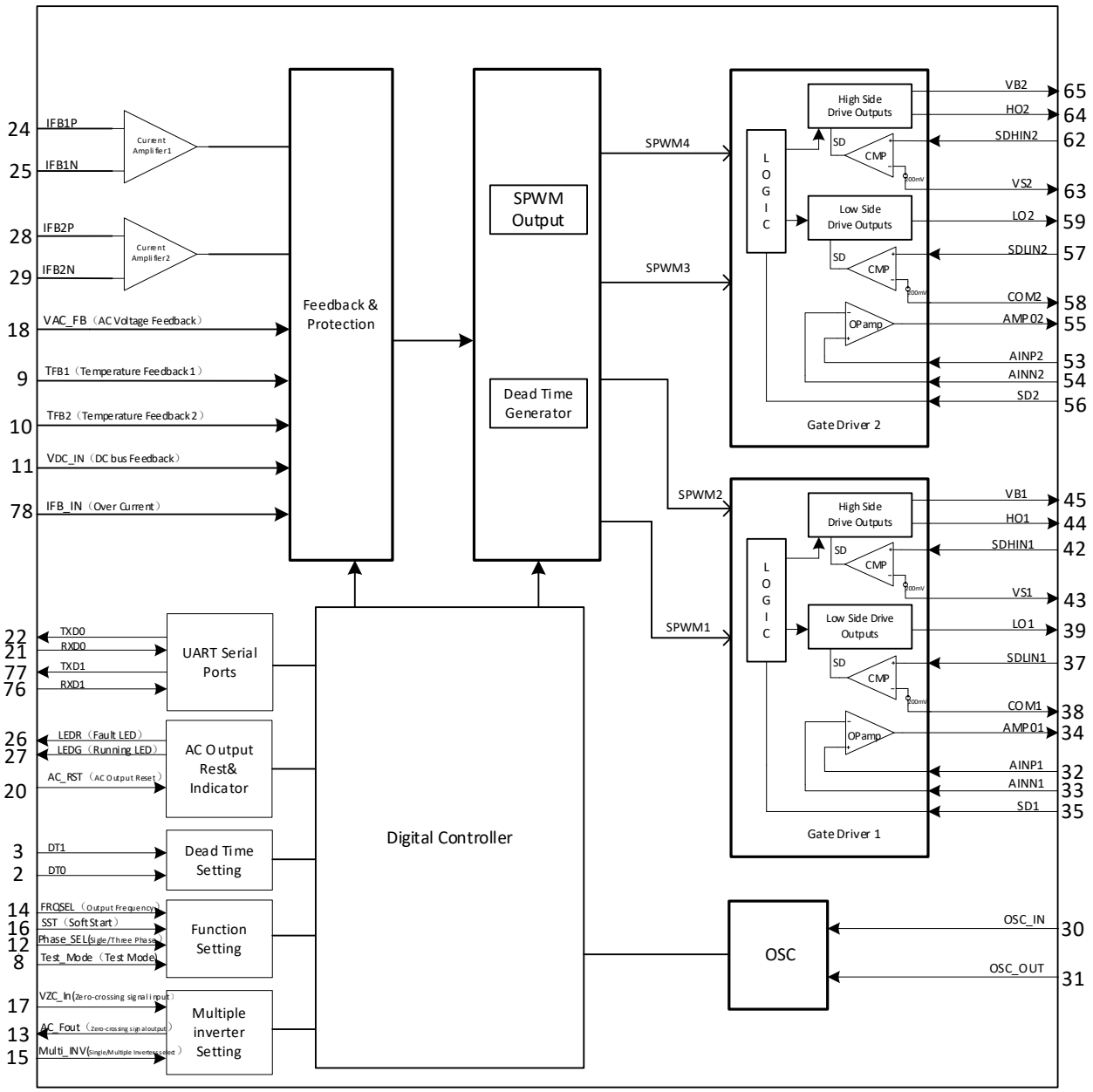



Figure 5-1. EG8025 Block Diagram

## 5.2 System Block Diagram Based on EG8025+EG1611

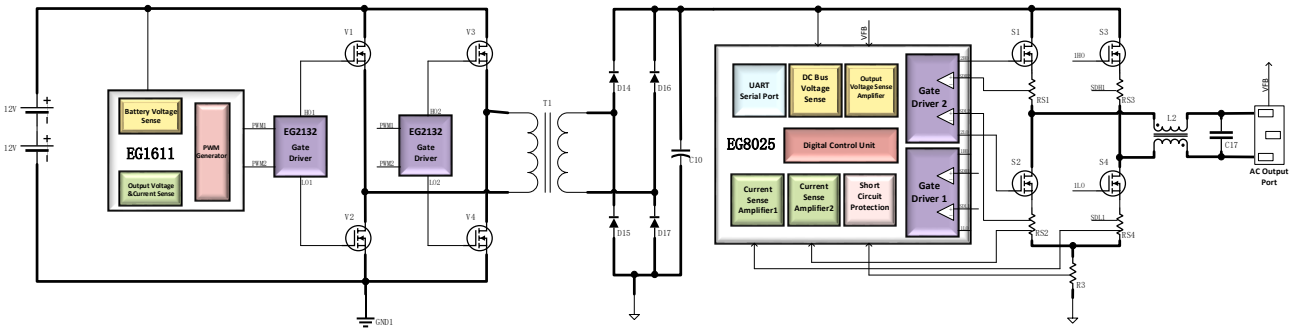



Figure 5-2. EG8025 Inverter System Block Diagram

# 6. Typical Application Schematic

## 6.1 EG8025 DC to AC Driver Board Schematic

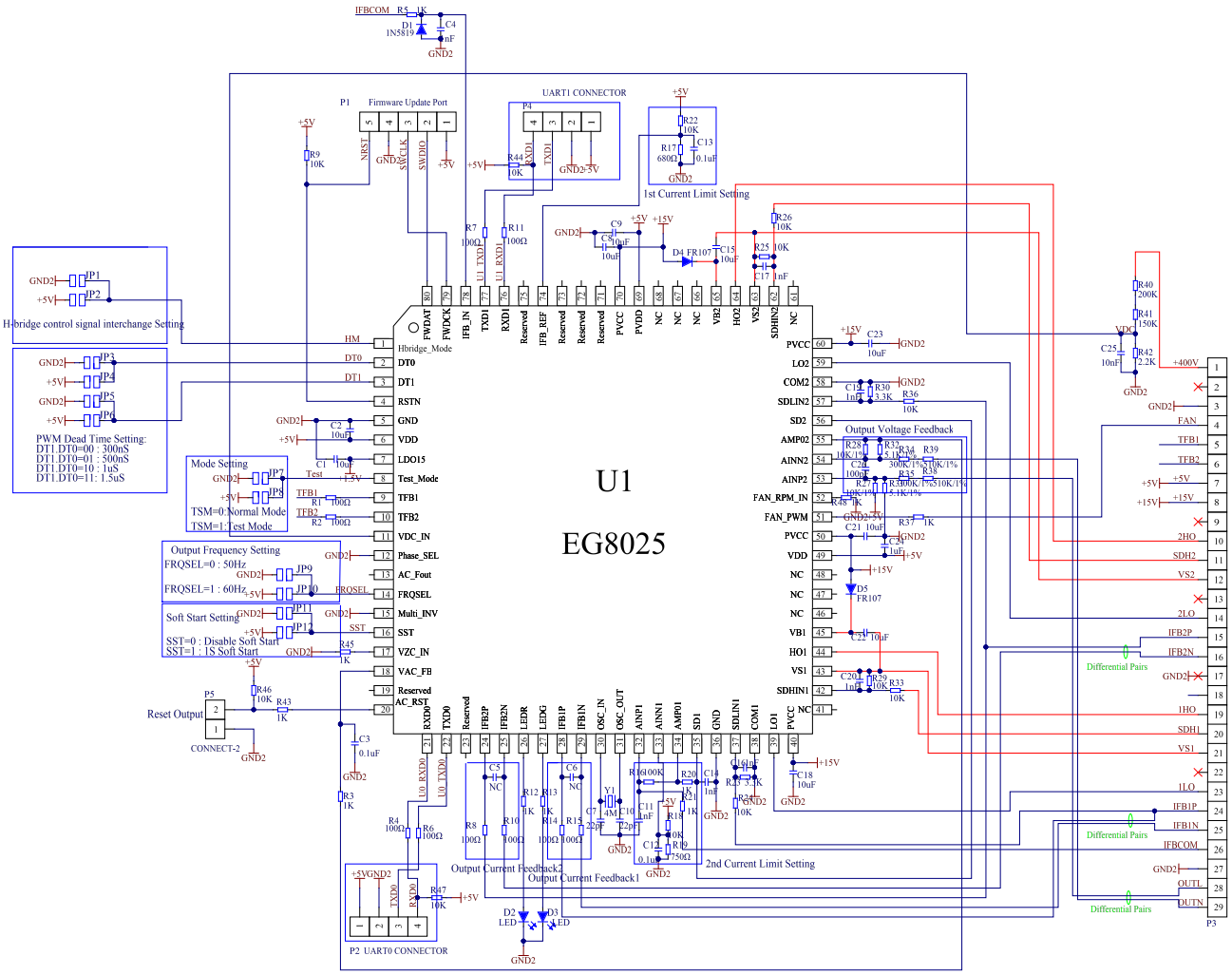



Figure 6-1. EG8025 DC to AC Driver Board Application Schematic

## 6.2 1KW Main Board Schematic of Power Inverter for 12VDC/220VAC

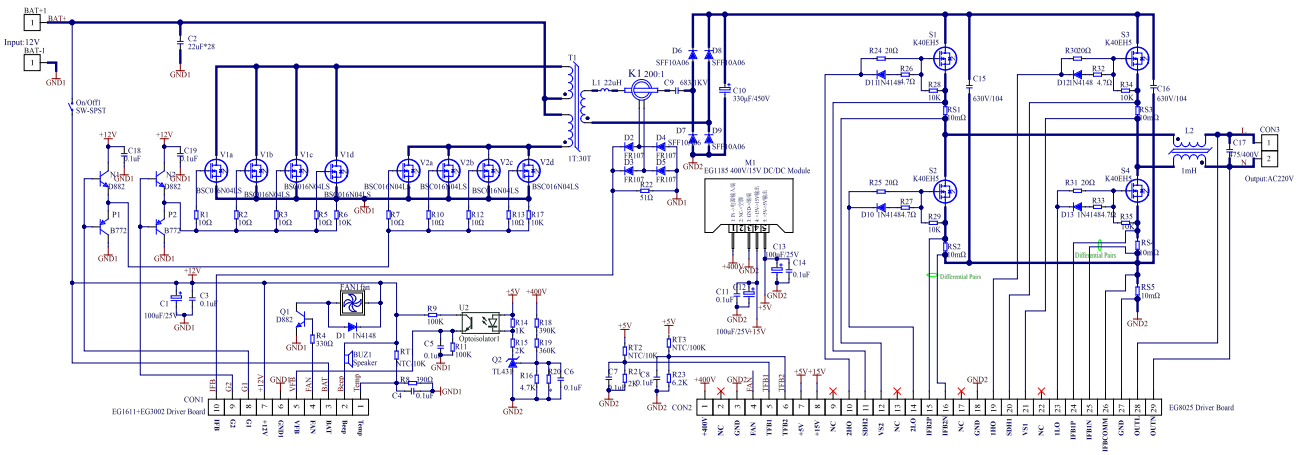


Figure 6-2. 1KW 12VDC/220VAC Power Inverter Application Schematic

## 6.3 1KW Main Board Schematic of Power Inverter for 24VDC/220VAC

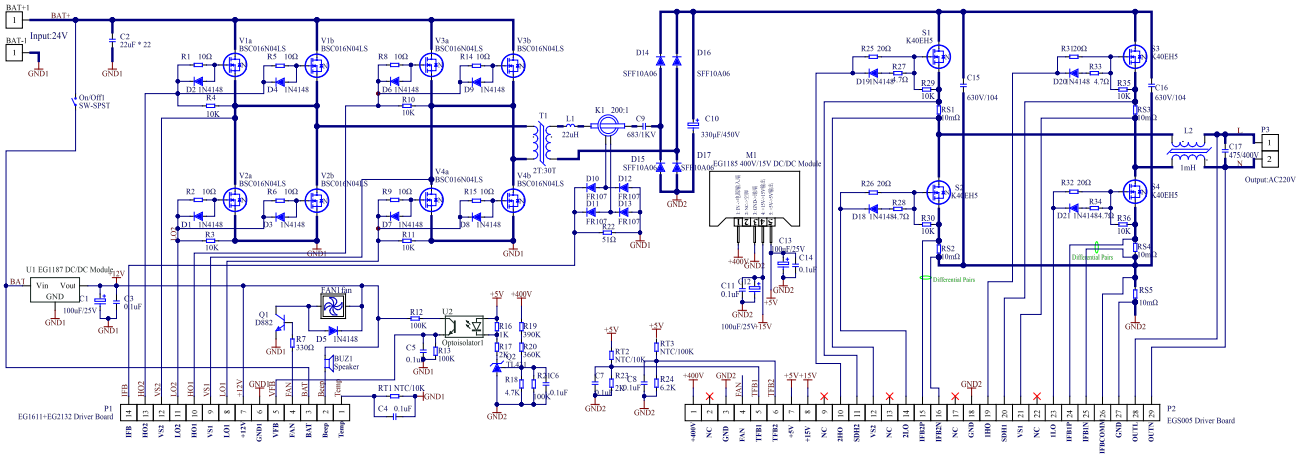


Figure 6-3. 1KW 24VDC/220VAC Power Inverter Application Schematic

## 6.4 1KW Main Board Schematic of Power Inverter for 48VDC/220VAC

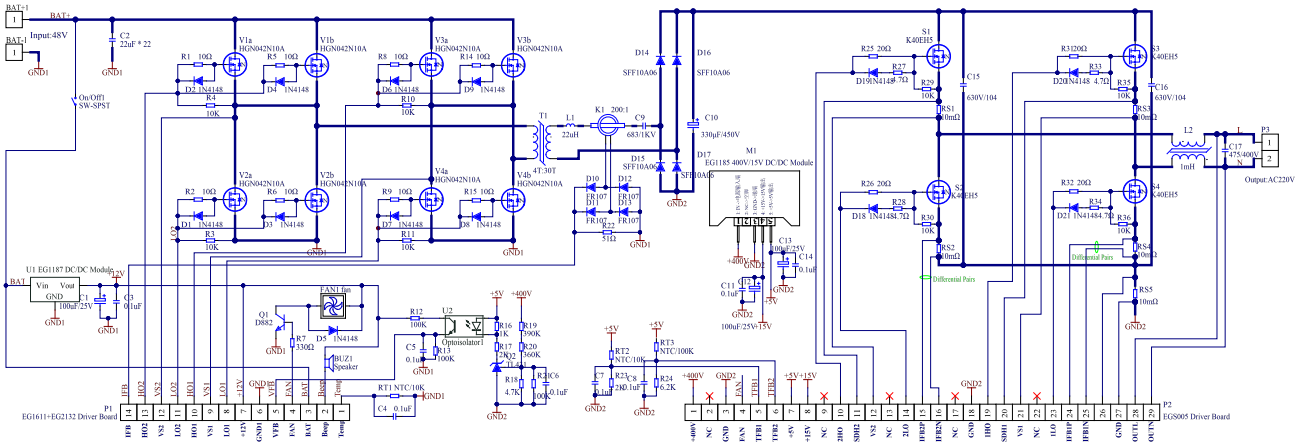


Figure 6-4. 1KW 48VDC/220VAC Power Inverter Application Schematic

## 6.5 EG1611+EG3002 Driver Board Schematic for 12VDC Input

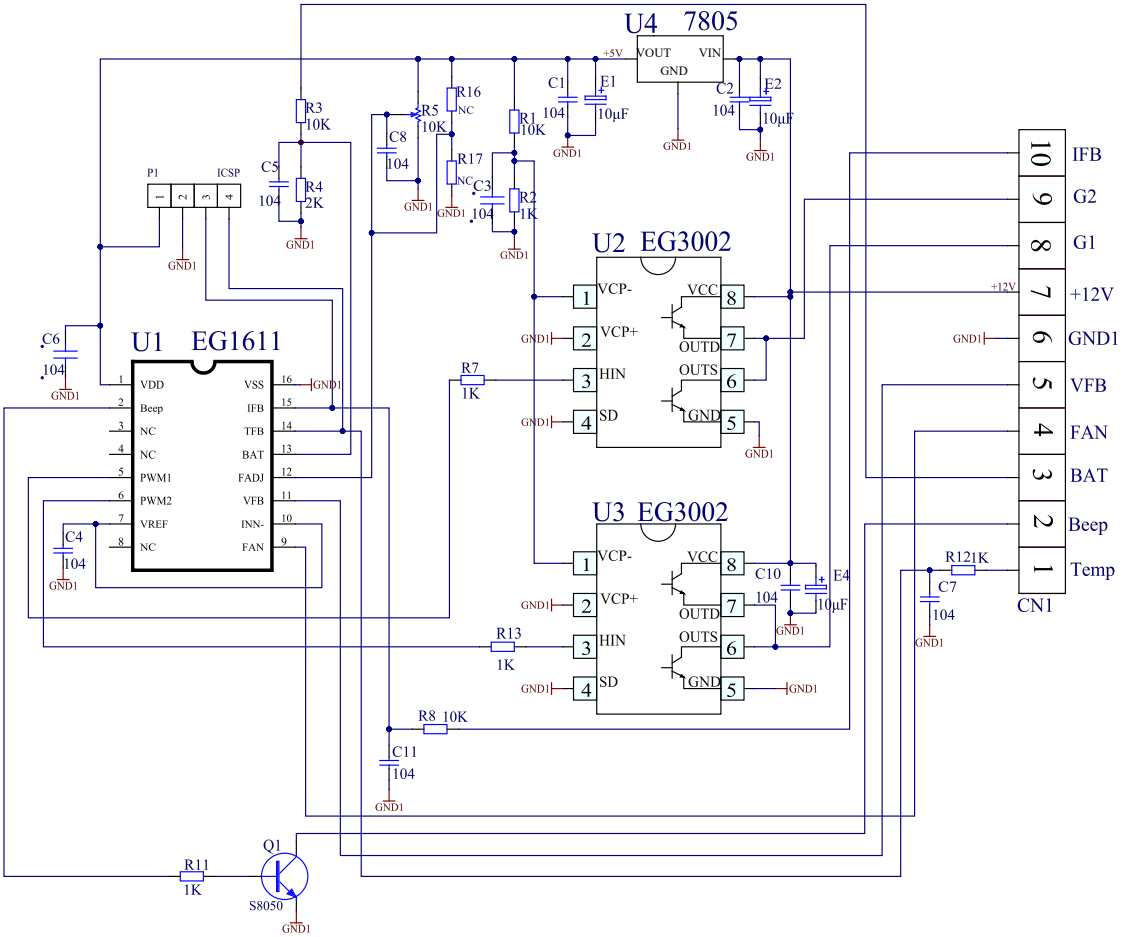



Figure 6-5. 12V Boost Stage Driver Board Application Schematic

## 6.6 EG1611+EG2132 Driver Board Schematic for 24VDC and 48VDC Input

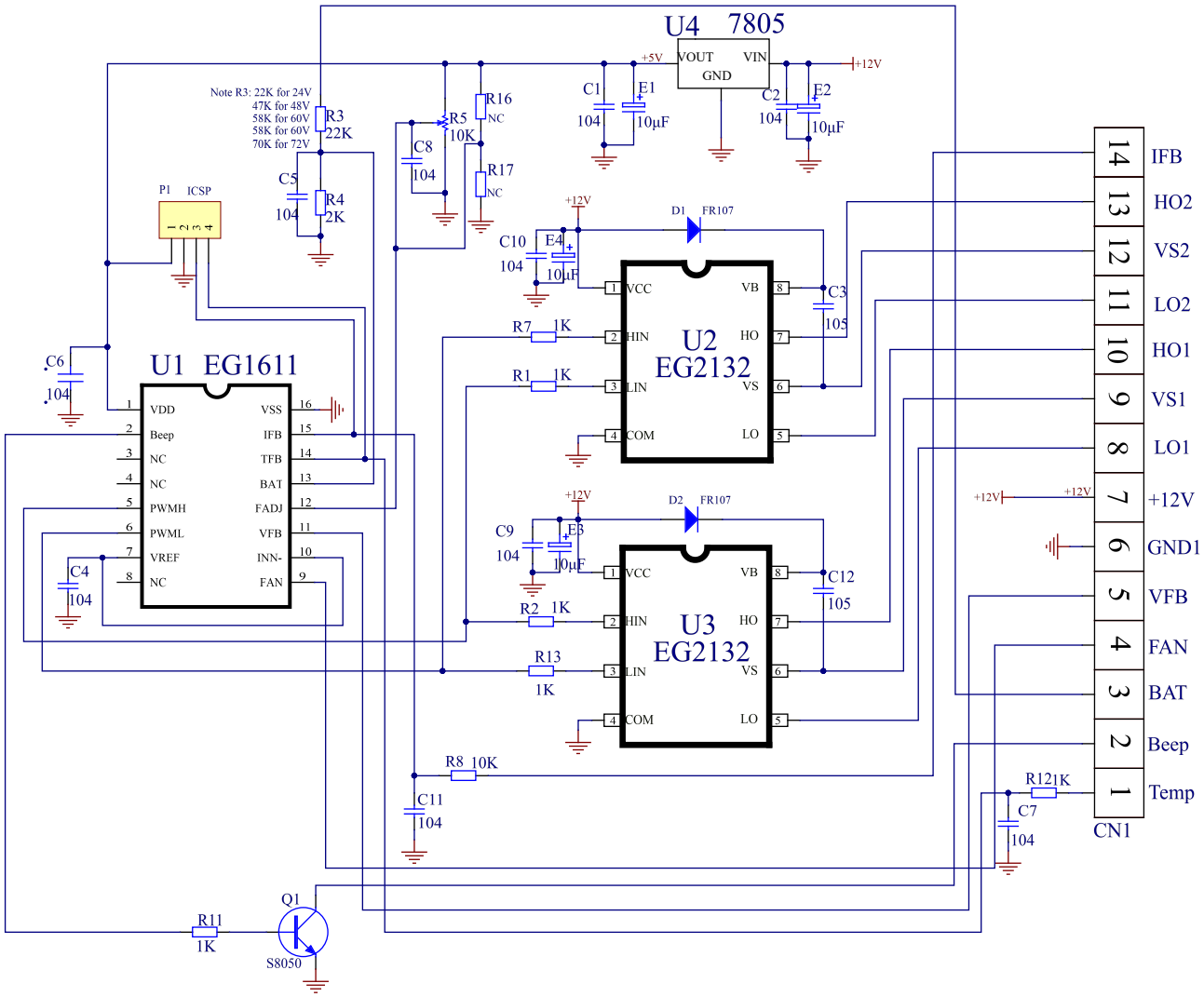



Figure 6-6. 24V and 48V Boost Stage Driver Board Application Schematic

# 7. Electrical Characteristics

## 7.1 Absolute maximum ratings

TA=25℃ unless otherwise specified

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **Gate Drivers Section** | | | | | |
| PVCC | Supply Voltage for Gate Drivers | PVCC with respect to the COM | -0.3 | 20 | V |
| PVDD | Logic Supply Voltage for Gate Drivers | PVDD with respect to the GND | -0.3 | 5.5 | V |
| VB1，VB2 | High Side Floating Supply Voltage | - | -0.3 | 600 | V |
| HO1，HO2 | High Side Drive Outputs | - | VS-0.3 | VB+0.3 | V |
| VS1，VS2 | High Side Floating Supply Offset Voltage | - | VB-20 | VB+0.3 | V |
| SDHIN1，SDHIN2 | High Side Shutdown Input Pins | - | VS-0.3 | VS+5 | V |
| LO1，LO2 | Low Side Drive Outputs | - | -0.3 | PVCC+0.3 | V |
| SDLIN1，SDLIN2， | Low Side Shutdown Input Pins | - | -0.3 | 5.5 | V |
| SD1，SD2 | Shutdown Input Pins | - | -0.3 | 5.5 | V |
| AINP1，AINP2，AINN1，AINN2，AMP01，AMP02 | Operation Amplifiers | - | -0.3 | 5.5 | V |
| **Control Section** | | | | | |
| VDD | Supply Voltage for control | VDD with respect to the GND | -0.3 | 7 | V |
| I/O | Control Input/Output Pins | - | -0.3 | 7 | V |
| Isink | Output sink current for control IO | - | - | 10 | mA |
| Isource | Output source current for control IO | - | - | -10 | mA |
| TA | Ambient Temperature | - | -45 | 105 | ℃ |
| Tstr | Storage Temperature | - | -65 | 125 | ℃ |

Note:Exceeding extreme conditions may permanently damage the chip.EG8025's reliability may be affected running at the extreme conditions for a long time.

## 7.2 Typical ratings

TA=25℃,OSC=4MHz unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | TYP | Max | Unit |
|---|---|---|---|---|---|---|
| PVCC | Supply Voltage for Gate Drivers | PVCC with respect to the COM | 10 | 15 | 18 | V |
| PVDD | Logic Supply Voltage for Gate Drivers | PVDD with respect to the GND | 3 | 5 | - | V |
| VDD | Supply Voltage for control | VDD with respect to the GND | 2.7 | 5 | 5.5 | V |
| Ipvcc | PVCC Supply Current | PVCC=15V | - | 1 | 1.2 | mA |
| Ipvdd | PVDD Supply Current | PVDD=5V | - | 1 | 1.2 | mA |
| Ivdd | VDD Supply Current | VDD=5V | - | 30 | 50 | mA |
| **Gate Drivers** | | | | | | |
| VB1，VB2 | High Side Floating Supply Voltage | VB1,VB2 with respect to the COM | 10 | | 600 | V |
| SDHIN1，SDHIN2 | High Side Shutdown Input Pins | SDHIN1,SDHIN2 with respect to the VS1,VS2 | - | 200 | - | mV |
| SDLIN1，SDLIN2 | Low Side Shutdown Input Pins | SDLIN1,SDLIN2 with respect to the COM | - | 200 | - | mV |
| SD1，SD2 | Shutdown Input Pins | SD1,SD2 with respect to the GND | 0 | | 5 | V |
| **Feedback** | | | | | | |
| VAC_FB | DC Common Voltage for Voltage Feedback | VDD=5V | - | 1.65 | - | V |
| | AC Reference Amplitude for Voltage | VDD=5V | - | 1.36 | - | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | Feedback | | | | | |
| IFB1P，IFB1N | Maximum Voltage Input for AC Current Feedback 1 | VDD=5V | - | | 320 | mV |
| IFB2P，IFB2N | Maximum Voltage Input for AC Current Feedback 2 | VDD=5V | - | | 320 | mV |
| TFB1 | Over Temperature input 1 | VDD=5V | - | 3.3 | - | V |
| TFB2 | Over Temperature input 1 | VDD=5V | - | 3.3 | - | V |
| VDC-IN | Under Voltage and Over Voltage Input for DC Bus | VDD=5V | 1.8 | - | 2.8 | V |
| **UART Ports** | | | | | | |
| TXD0，TXD1 | Vout(H) Output High Voltage | VDD=5V, IOH=-10mA | 3.5 | 5.0 | - | V |
| | Vout(L) Output Low Voltage | VDD=5V, IOL=10mA | - | 0 | 0.3 | V |
| RXD0，RXD1 | Vin(H) Input High Voltage Level | VDD=5V | 3.0 | 5.0 | 5.5 | V |
| | Vin(L) Input High Voltage Level | VDD=5V | -0.3 | 0 | 1 | V |
| **Control** | | | | | | |
| LEDR，LEDG,AC_Fout | Vout(H) Output High Voltage | VDD=5V, IOH=-10mA | 3.5 | 5.0 | - | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | Vout(L) Output Low Voltage | VDD=5V, IOL=10mA | - | 0 | 0.3 | V |
| Hbridge_Mode,DT0 DT1， Test_Mode, Phase_SEL, FRQSEL,Multi_INV,SST ,VZC_IN,AC_RST | Vin(H) Input High Voltage Level | VDD=5V | 3.0 | 5.0 | 5.5 | V |
| | Vin(L) Input Lo Voltage Level | VDD=5V | -0.3 | 0 | 1 | V |

# 8. Detailed Description

## 8.1 PWM Modulation

EG8025 works in center-aligned PWM modulation mode with fixed switching frequency of 20KHz. The advantage is that switching frequency on the H-bridge is 20KHz, while the switching frequency on output inductor and output capacitor is twice(40KHz) the switching frequency. Compared with traditional inverters using the unipolar or bipolar modulation, the size of capacitors and inductors can be reduced.

## 8.2 AC Output Voltage Feedback

EG8025 uses instantaneous voltage feedback SPWM control technology, and waveform of the output is instantaneously regulated(every PWM cycle 50uS) by the comparison of the instantaneous voltage feedback with a sinusoidal reference. Compared with traditional single voltage-mode SPWM control, the EG8025 has advantages of the high output voltage accuracy and the fast dynamic response, and output harmonic distortion is less than 3% at heavy load.

The sinusoidal reference voltage in the EG8025 consists of an sine wave amplitude of 1.36V and a DC offset of 1.65V.

EG8025’s voltage feedback process is through measuring AC voltage output of inverter by pins(53,54,55)VAC_FB. For such voltage sampling and feedback circuit shown in Fig 8.2a and Fig 8.2b, it calculates the error between measured output voltage and sinusoid reference voltage, and adjusts the output voltage accordingly.

EG8025 uses an external resistor network consisting of differential amplifier for output voltage feedback as shown in Fig 8.2a. Note the external resistance must be satisfied that (R39+R34) equals (R38+R35) and (R28 // R32) equals (R27 // R31). ( Notes: Here the symbol // means parallel.)

**For inverter of output voltage 230V, the application circuit is shown in Fig 8.2a.**

The following formals are a reference design for setting output voltage.

Step1、Calculates the DC offset of OPamp output

Vout_DC=$\frac{R31}{R27+R31}$ x 5V=5.1K/15.1K x 5V≈1.68V（As Fig 8.2a）.

Step2、Calculates the gain of OPamp

A=(R28//R32)/(R39+R34)

Step3、Calculates the output voltage of OPamp：Vout_AC=A*Vin

Vout_AC = $\frac{R28 // R32}{R34+R39}$ x($V_{ACL}$ -$V_{ACN}$) ≈ $\frac{1}{240}$ x($V_{ACL}$ -$V_{ACN}$) （As Fig 8.2a）

According to the above formals, it is a scaled down amplifier with a ratio of 1/240.

For 230V AC output voltage with 325V amplitude, the output voltage of OPamp is equal to VAC_FB=Vout_DC+Vout_AC=1.68V+1.35V=3.03V. it will feedback to pin 18 of VAC_FB. after calculating the error, then adjusts the output voltage accordingly.

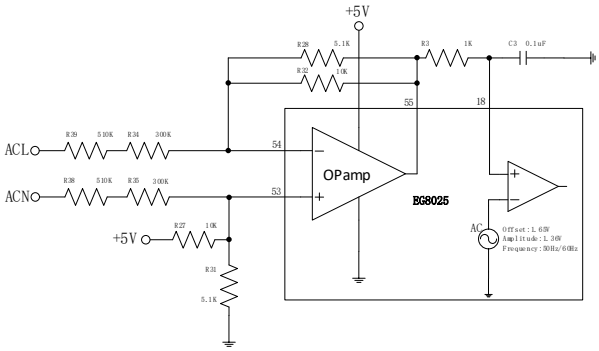



Figure 8.2a The Feedback Network of AC Output Voltage for 230V Inverter

**For inverter of output voltage 120V, the application circuit is shown in Fig 8.2b.**

The following formals are a reference design for setting output voltage.

Step1、Calculates the DC offset of OPamp output

Vout_DC= $\frac{R31}{R27+R31}$ x 5V=5.1K/15.1K x 5V≈1.68V（As Fig 8.2b）.

Step2、Calculates the gain of OPamp

A=(R28//R32)/(R39+R34)

Step3、Calculates the output voltage of OPamp：Vout_AC=A*Vin

Vout_AC = $\frac{R28 // R32}{R34+R39}$ x($V_{ACL}$ -$V_{ACN}$) ≈ $\frac{1}{118}$ x($V_{ACL}$ -$V_{ACN}$) （As Fig 8.2b）

According to the above formals, it is a scaled down amplifier with a ratio of 1/240.

For 120V AC output voltage with 170V amplitude, the output voltage of OPamp is equal to VAC_FB=Vout_DC+Vout_AC=1.68V+1.44V=3.12V. it will feedback to pin 18 of VAC_FB. after calculating the error, then adjusts the output voltage accordingly.

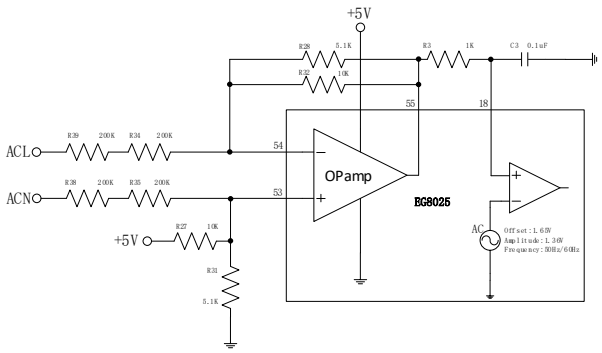



Figure 8.2b The Feedback Network of AC Output Voltage for 120V Inverter

## 8.3 AC Output Current Feedback

The EG8025’s AC current sampling and feedback circuit structure is shown in Figure 8.3a. IFB1P,IFB1N and IFB2P,IFB2N sample the currents on shunt resistors RS2 and RS4 respectively. IFB1P,IFB1N are responsible for sampling the positive half cycle current of AC output when Hbridge_Mode=0,and IFB2P,IFB2N are responsible for sampling the negative half cycle current of AC output when Hbridge_Mode=0. Through internal fixed gain 9.5 amplifiers and a current synthesizer,then feed back to internal current mode loop to calculate the error to adjust load response.

External PCB traces of IFB1P,IFB1N and IFB2P,IFB2N are required with differential pairs to rout. The recommend resistance for R97,R98,R101,R102 is 100Ω,as shown in Fig 8.3.If user needs to change the resistance,it is recommended that the maximum resistance not exceed 1KΩ,otherwise it will affect the gain of internal amplifier.

The internal current loop of EG8025 sets the maximum saturation current value. The maximum saturation current value is Imax=3000mV/9.5/Rs. For example, when Rs is 0.01Ω, maximum current Imax=3000mV/9.5/0.01Ω=31.5A can be obtained. Here 0.01Ω(Rs) is more suitable for 1.5KW inverter applications. For different power watts inverter applications, the shunt resistance can be changed according to above formula.

The pins of IFB1P, IFB1N and IFB2P,IFB2N cannot be left floating or connect to GND, and it must refer the connection of section 8.7, otherwise the output voltage will fail.

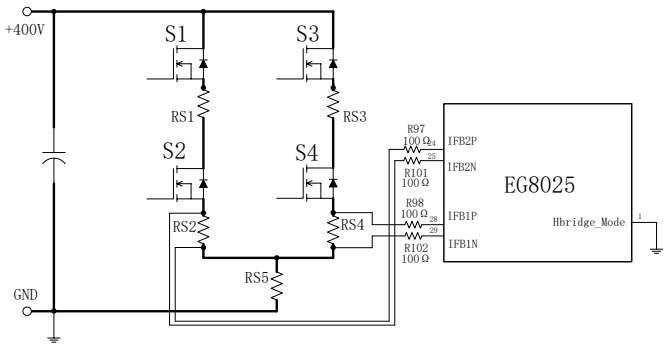



Figure 8.3a AC output current feedback

EGmicro provides a software utility of computer side that can calibrate the output voltage and output current for mass production. User can log in www.egmicro.com website to download it or contact us for it.

## 8.4 Temperature Feedback

EG8025 provides two channels temperature feedback TFB1 and TFB2, which is use for over temperature protection and detection the temperature value to report onto UART. The TFB1 is mainly used to detect temperature of PCB board, and the TFB2 is mainly used to detect IGBT temperature. The temperature detection circuit is shown in Figure 8.4a.

The temperature detection circuit of TFB1 is a simple voltage divider circuit, which consists of thermal resistor RT1 and R60 resistor, as shown in Fig 8.4a.Thermal resistor has 10K resistance at 25℃(B=3950),and the recommend resistance for R60 is 2KΩ.The TFB1’ s over temperature voltage is set to 3.3V,corresponding over temperature value is about 85℃, and hysteresis value of over temperature protection is 10℃,it will turn off the over temperature protection when temperature value is less than 75℃.

The temperature detection circuit of TFB2 is a simple voltage divider circuit, which consists of thermal resistor RT2 and R61 resistor, as shown in Fig 8.4a.Thermal resistor has 100K resistance at 25℃(B=3950),and the recommend resistance for R61 is 6.2KΩ.The TFB2’ s over temperature voltage is sets to 3.3V,corresponding over temperature value is about 130℃, and hysteresis value of over temperature protection is 10℃,it will turn off the over temperature protection when temperature value is less than 120℃.

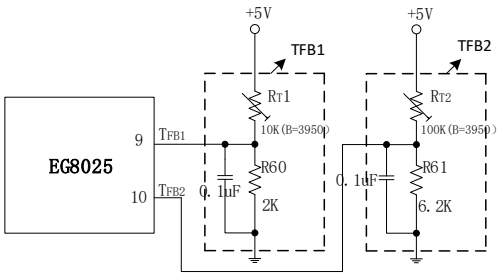



Figure 8.4a EG8025 Temperature Detection Circuit

## 8.5 DC bus Voltage Feedback

In order to prevent inverter from being damage duo to too low or too high DC bus voltage input, EG8025 has a build-in DC bus detection circuit for over voltage and under voltage protection. The DC bus voltage detection circuit shown in Figure 8.5a. The detection circuit of pin11 VDC_IN is a simple voltage divider circuit.

The over voltage value of VDC_IN is set to 2.8V with 500mS delay, corresponding over voltage value of DC bus is about 440V (as shown in circuit of Fig 8.5a), and hysteresis value of over voltage protection is 10V,it will turn off the over voltage protection when DC bus voltage value is lower than 430V.

The under voltage value of VDC_IN is set to 1.8V with 10S delay, corresponding under voltage value of DC bus is about 290V (as shown in circuit of Fig 8.5a), and hysteresis value of under voltage protection is 30V,it will turn off the under voltage protection when DC bus voltage value is higher than 320V.

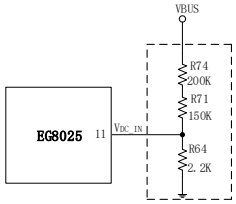



Figure 8.5a EG8025 DC Bus Detection Circuit

## 8.6 Dead Time Setting

The DT1 and DT0 pins control the dead time. Dead time is one of the important characteristics of IGBT/MOSFET. Lack of enough dead time will result in the damage of MOSFET duo to bridge shoot-through. If the dead time is too long, it will lead to distortion of waveform and overheating of MOSFET. Figure 8.6a is the four dead time settings of EG8025, “00” =300nS, “01” =500nS, “10” =1uS, “11” =1.5uS.

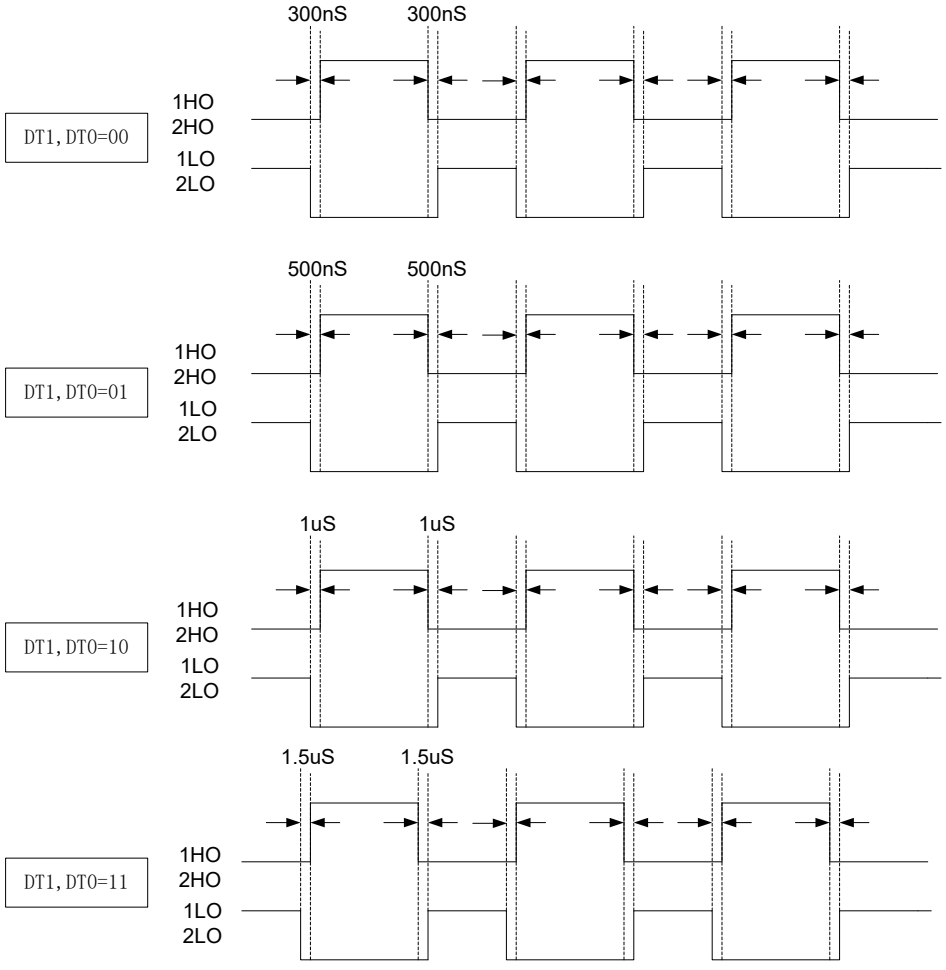



Figure 8.6a EG8025 Dead Time Control Setting

## 8.7 H-Brdige Control Signal Interchange

EG8025 supports the legs interchange function of left bridge and right bridge, the purpose is more easily to layout the PCB board after left bridge and right bridge are interchanged.

The pin 1(HBridge_Mode) of EG8025 is used for setting H-Bridge interchange.

**The application circuit with HBridge_Mode "0" is shown in Fig 8.7a.**

When HBridge_Mode is "0",the **left-bridge’ s IGBTs/MOSFETs** are controlled by output signals of HO2,VS2,LO2,SDHIN2,SDLIN2 from gate driver 2, and **right-bridge’ s IGBTs/MOSFETs** are controlled by output signals of HO1,VS1,LO1,SDHIN1,SDHLIN from gate driver 1. IFB1P,IFB1N are responsible for sampling the positive half cycle current of AC output when Hbridge_Mode=0, and it must be connected to RS4 shunt resistor. IFB2P,IFB2N are responsible for sampling the negative half cycle current of AC output when Hbridge_Mode=0, and it must be connected to RS2 shunt resistor.

The output inductor L1 on ACL must be connected to switching node of left bridge, and L2 on ACN must be connected to switching node of right bridge. The positive sensing input of differential amplifier must be connected to ACL, and the negative sensing input of differential amplifier must be connected to ACN, so that the output voltage feedback can be in phase with internal AC reference voltage.

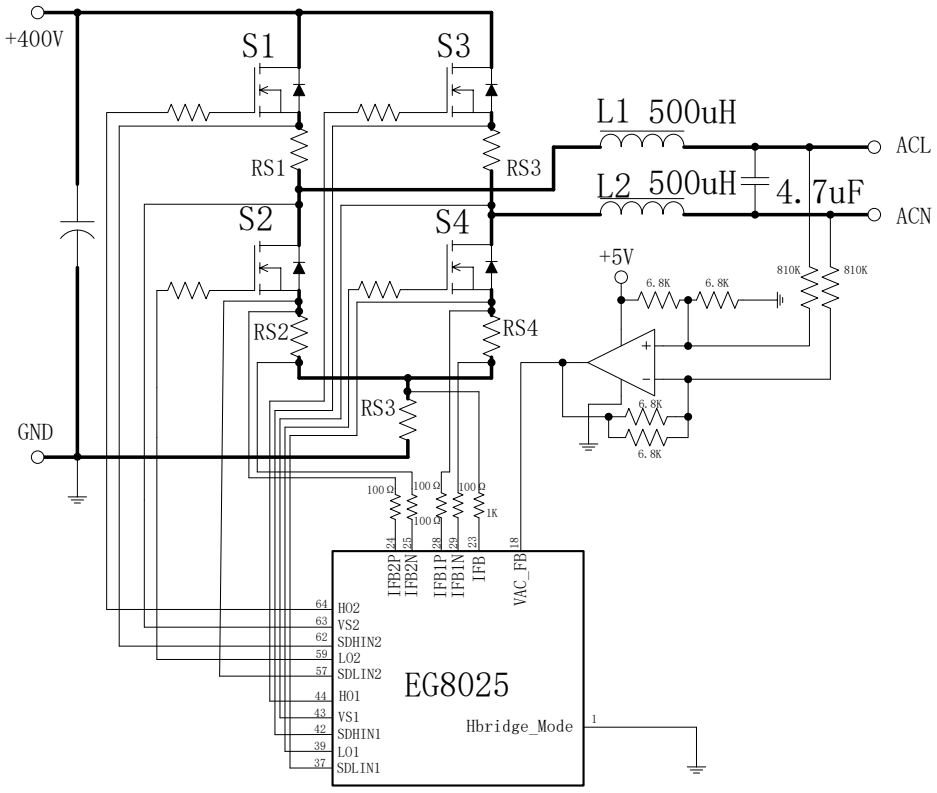



Figure 8.7a The application circuit with HBridge_Mode “0”

**The application circuit with HBridge_Mode "1" is shown in Fig 8.7b.**

When HBridge_Mode is "1",the **left-bridge’s IGBTs/MOSFETs** are controlled by output signals of HO1,VS1,LO1,SDHIN1,SDHLIN from gate driver 1, and **right-bridge’s IGBTs/MOSFETs** are controlled by output signals of HO2,VS2,LO2,SDHIN2,SDLIN2 from gate driver 2. IFB1P,IFB1N are responsible for sampling the negative half cycle current of AC output when Hbridge_Mode=1, and it must be connected to RS2 shunt resistor. IFB2P,IFB2N are responsible for sampling the positive half cycle current of AC output when Hbridge_Mode=1, and it must be connected to RS4 shunt resistor.

The output inductor L1 on ACL must be connected to switching node of left bridge, and L2 on ACN must be connected to switching node of right bridge. The positive sensing input of differential amplifier must be connected to ACL, and the negative sensing input of differential amplifier must be connected to ACN, so that the output voltage feedback can be in phase with internal AC reference voltage.

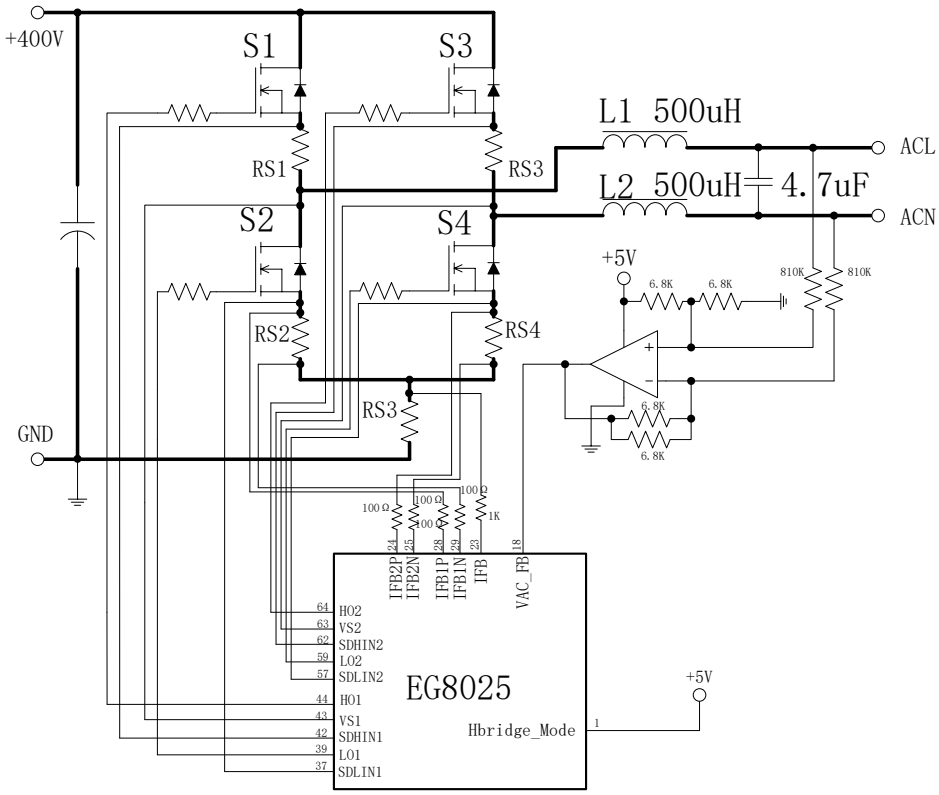



Figure 8.7b The application circuit with HBridge_Mode “1”

# 9. Protections

EG8025 features some protections against over load, over current, over voltage and under voltage for DC bus, over temperature, short circuit, and etc.

EG8025 provides two AC voltage reset modes, one is to perform a hardware reset by pulling down pin 20(AC_RST) to a low voltage, another is to perform a software reset through a UART commands.

The following protection values are based on a 1KW power inverter, and EGmicro can provide parameter modification according to user requirements.

## 9.1 Over Load Protection

EG8025 has over load protection function. When continuous output power is greater than 1100W, the red LED on pin 26(LEDR) starts to blink indicating. When continuous output power is greater than 1200W for 60 seconds or greater than 1300W for 1 second, the output will be turned off and outputs red LED indicating. User can read the over load status indication through the UART serial ports.

## 9.2 Over Load Protection

EG8025 has over current protection function. When AC continuous output current is greater than 5A, the red LED on pin 26(LEDR) starts to blink indicating. When AC continuous output current is greater than 5.5A for 60 seconds, the output will be turned off and outputs red LED indicating. User can read the over current status indication through the UART serial ports.

## 9.3 Over Voltage and Under Voltage Protection for DC Bus

EG8025 has over voltage and under voltage protection function for DC bus. When DC bus voltage is higher than 440V or lower than 290V , the output will be turned off and outputs red LED indicating. User can read the over voltage and under voltage status indication through the UART serial ports.

## 9.4 Over Temperature Protection for PCB Board

EG8025 has a over temperature protection function for PCB board. When TFB1’s temperature value is higher than 85℃, the output will be turned off and outputs red LED indicating. User can read the over temperature status indication through the UART serial ports.

## 9.5 Over Temperature Protection for IGBT/MOSFET

EG8025 has a over temperature protection function for IGBT. When TFB2’s temperature value is higher than 130℃, the output will be turned off and outputs red LED indicating. User can read the over temperature status indication through the UART serial ports.

## 9.6 Short Circuit Protection for Output

EG8025 has short circuit protection function for output. When short circuit fault is happened, after a short time 30mS delay, the output will be turned off and outputs red LED indicating. User can read the short circuit status indication through the UART serial ports.

## 9.7 Peak Current Protection for IGBT/MOS

EG8025 provides independent four channels current protection circuit for H-bridge IGBT/MOSFET, and four comparators with 200mV reference source, which are used for peak current limitation of H-bridge's IGBT/MOSFET. The peak current protection circuit of IGBT/MOSFET is shown in Figure 9.7a.

The following formals are a reference design for setting peak current value.

Peak current protection value of S1: Is1_peak=200mV*(1+R26/R25)/RS1

For example, when R26=10K,R25=10K,RS1=10m Ω

Is1_peak=200mV*(1+10K/10K)/10m Ω =40A

Peak current protection value of S2: Is2_peak=200mV*(1+R36/R30)/（RS2+RS5）

For example, when R36=10K,R30=3.3K,RS2=10m Ω ,RS5=10m Ω

Is2_peak=200mV*(1+10K/3.3K)/(10m Ω +10m Ω )=40A

Peak current protection value of S3: Is3_peak=200mV*(1+R33/R29)/RS3

For example, when R33=10K,R29=10K,RS3=10m Ω

Is3_peak=200mV*(1+10K/10K)/10m Ω =40A

Peak current protection value of S3: Is4_peak=200mV*(1+R24/R23)/（RS4+RS5）

For example, when R36=10K,R30=3.3K,RS2=10m Ω ,RS5=10m Ω

Is4_peak=200mV*(1+10K/3.3K)/(10m Ω +10m Ω )=40A

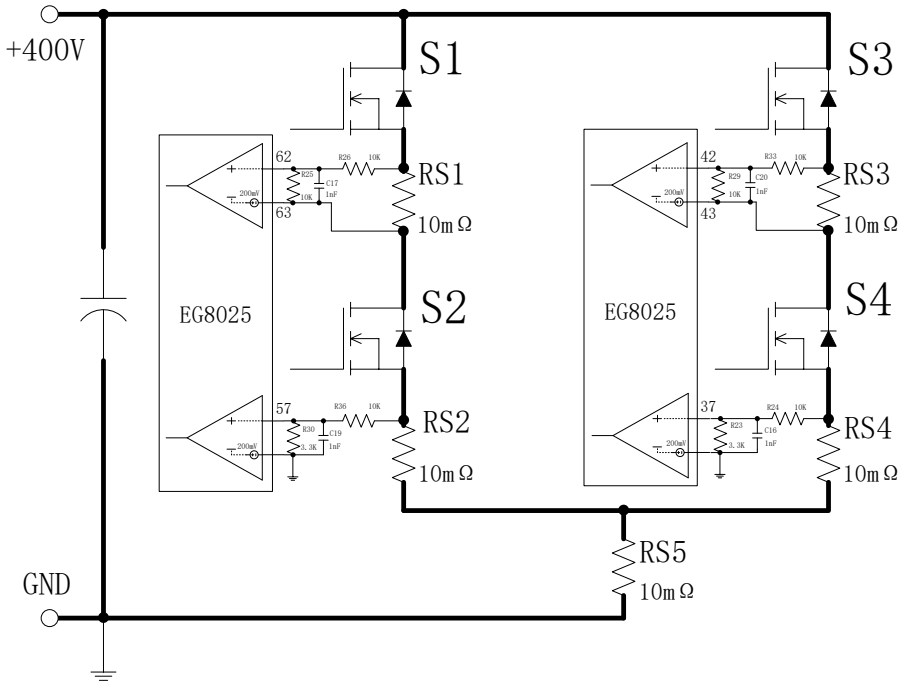



Figure 9.7a The independent four channels current protection circuit of IGBTs/MOSFETs

# 10. Multiple Inverter Applications

EG8025 supports the function of group three-phase four-wire inverter or multi-inverter in parallel applications. The following pins are used to setup multiple inverters application. The diagram of inverter in parallel is shown in Figure 10-a, and the diagram of group three-phase four-wire inverter is shown in Figure 10-b.

- Pin 15-> Multi_INV Single/Multiple Inverters select

  "0": It is applied to single inverter or the host of Multi-inverters

  "1": It is applied to inverters in parallel or group three-phase four-wire inverter through combination with the pin 12.
- Pin 12-> Phase_SEL Phase Selection input for zero-crossing synchronization or 120-degree phase delay processing.

  "0":zero-crossing synchronization, which can realize the application of parallel or the host of group three-phase inverter.

  "1":120 degree phase delay processing after zero-crossing input, which is only for group three-phase four-wire inverter.
- Pin 17-> VZC_IN Zero-crossing signal input
- Pin 13-> AC_FOUT Zero-crossing output signal

## 10.1 Diagram of Inverter in Parallel

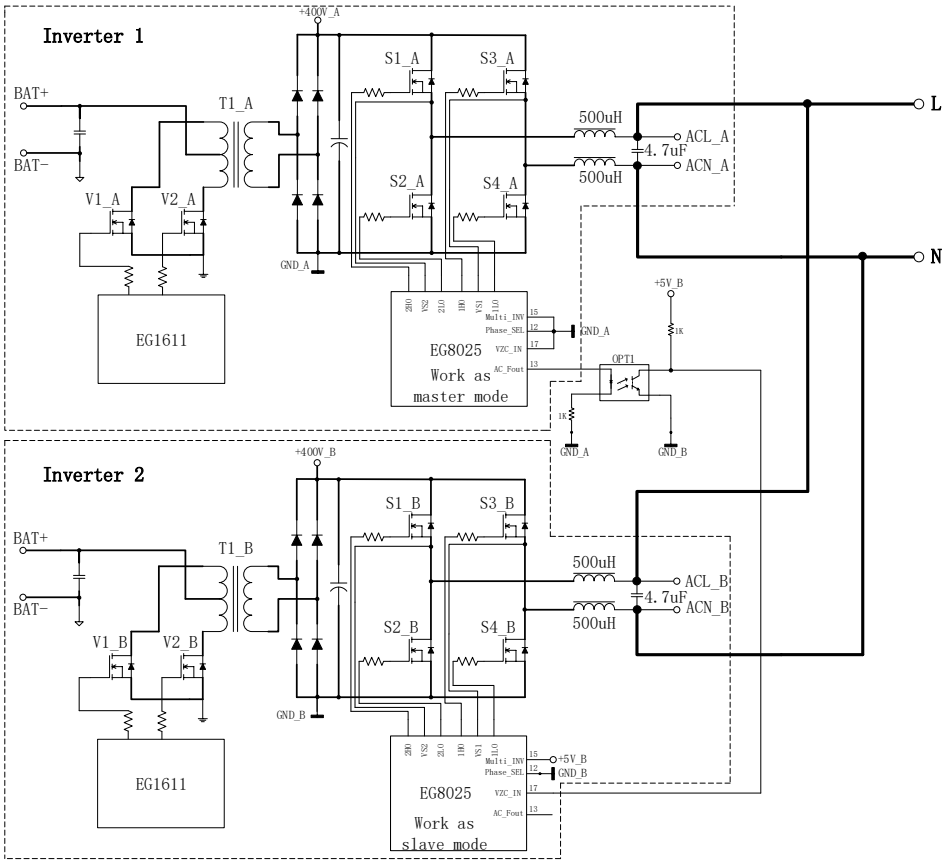



Figure 10-a. Diagram of inverter in parallel

## 10.2 Diagram of Group Three-Phase Four-Wire Inverter

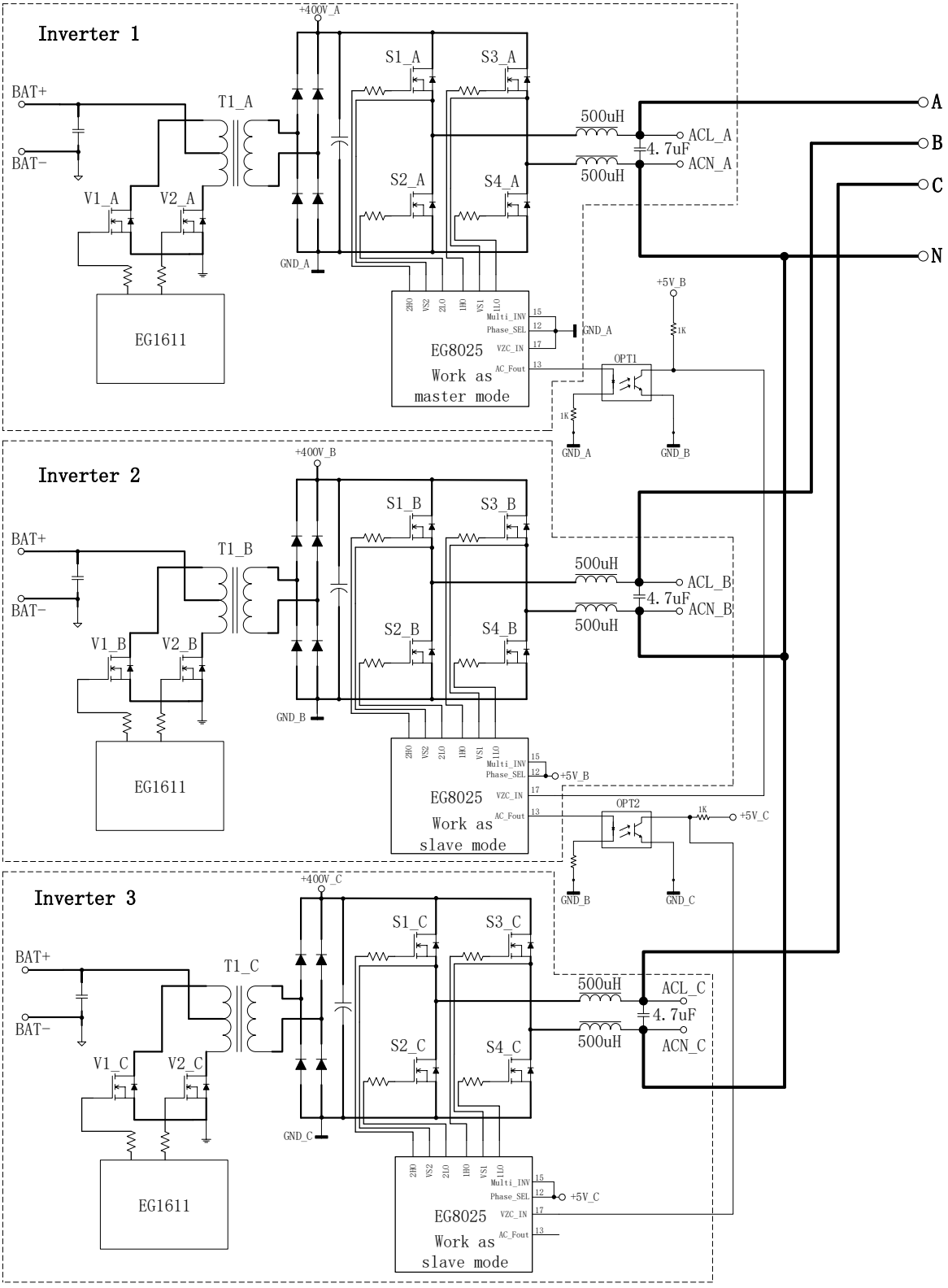



Figure 10-b. Diagram of Group Three-Phase Four-Wire Inverter

**Note:** The power supplies of 400V_A/GND_A,400V_B/GND_B,400V_C/GND_C must be isolated from each other as Figure 10-b.

# 11. Test Mode

EG8025 provides a test mode for debugging the working parameters of external circuit, such as gate drivers outputs, operational amplifier working, the rise and fall time of IGBT/MOSFET gates, output LC filter parameter, and etc.

When Test_Mode is "1",EG8025 enters test mode. In test mode,EG8025 outputs an open-loop SPWM signals, which means that there are no protection functions, and the voltage feedback and current feedback are invalid.

The following is a comparison table of pins parameter in test mode and normal mode.

| Pins Parameter | Maximum ratings in normal mode | Maximum ratings in test mode |
|---|---|---|
| VAC_FB（Pin18） | 1.65V+1.35V | 0～5V |
| IFB1P，IFB1N（Pin28，Pin29） | 320mV | 0～5V |
| IFB2P，IFB2N（Pin24，Pin25） | 320mV | 0～5V |
| IFB_IN（Pin78） | 0.5V | 0～5V |
| TFB1（Pin9） | 3.3V | 0～5V |
| TFB2（Pin10） | 3.3V | 0～5V |
| VDC-IN（Pin11） | >2.8V or <1.8V | 0～5V |

# 12. UART Serial Ports

## 12.1 UART Parameters

**Serial Communication Parameters** : (9600.8.N.1)

Baud rate:9600
Data bit length:8
Parity: None
Stop bit:1

**Serial Communication Functions:**

There are two serial communication functions on UART, one is **APP** function and other is **CFG** function. The **APP** is an **Application** register that mainly used to send status of inverter to the host and to receive control commands from the host to control unit. The **CFG** is a advanced **Configuration** register that mainly used to set working mode of inverter and to calibrate the parameters value. The **APP** works in inverter running. The **CFG** works in inverter stopping. The parameter values configured through the **CFG** will be stored in the FLASH of EG8025, and automatically load during power on.

## 12.2 APP Functions

The **APP** is an **Application** layer function, which mainly used to send status of inverter to the host and to receive control commands from the host to control unit. The **APP** works in inverter running.

### 12.2.1 APP Message for sending

EG8025 will continuously send status messages to the host at 200ms intervals with a length of 16 bytes after power up.

**Status Message:**

| Status Message（200ms intervals period） | | |
|---|---|---|
| BYTE0 | Header | 0x55 |
| BYTE1 | High Byte of output voltage | **Output Voltage:** the data of output voltage is represented by 2 bytes. The LSB is 0.1V. For example:[0x08,0xCF] The voltage is represented by two hexadecimal numbers,0x08 converted to decimal is 8 and 0xCF converted to decimal is 207.The decimal value of the data is 8*256+207=2255.The resulting voltage V=2255*0.1V=225.5V. |
| BYTE2 | Low Byte of output voltage | |
| BYTE3 | High Byte of output current | **Output Current:** the data of output current is represented by 2 bytes. The LSB is 0.01A. For example:[0x02,0xCF] The current is represented by two hexadecimal numbers,0x02 converted to decimal is 2 and 0xCF converted to decimal is 207.The decimal value of the data is 2*256+207=719.The resulting Current I=719*0.01A=7.19. |
| BYTE4 | Low Byte of output current | |

| | | |
|---|---|---|
| BYTE5 | High Byte of DC bus voltage | **DC bus Voltage:** the data of DC bus voltage is represented by 2 bytes. The LSB is 0.1V. For example:[0x0E,0x83] The voltage is represented by two hexadecimal numbers,0x0E converted to decimal is 14 and 0x83 converted to decimal is 131.The decimal value of the data is 14*256+131=3715.The resulting voltage V=3715*0.1V=3715.5V. |
| BYTE6 | Low Byte of DC bus voltage | |
| BYTE7 | Reserved | Reserved |
| BYTE8 | Reserved | Reserved |
| BYTE9 | IGBT’S Temperature | **IGBT’s Temperature：** the data of IGBT’s temperature is 1 byte with signed number, and the minimum resolution is 1℃.<br>For example:<br>[0x16] 0x16 converted to decimal is 20,the resulting temperature T=20℃<br>[0xF0] 0xF0 converted to decimal is -16,the resulting temperature T=-16℃ |
| BYTE10 | Fault Codes | Fault Codes:<br>0x00：Undefined<br>0x01：Over Load<br>0x02：Short Circuit<br>0x03：Under Voltage of AC output voltage<br>0x04：Over Voltage of DC bus<br>0x05：Under Voltage of DC bus<br>0x06：Phase Error<br>0x07：Over Temperature<br>0x08：Over Current<br>0x09：Frequency Mismatch<br>0x0A：Engine speed too low<br>0x0C：Inverter OFF |
| BYTE11 | PCB’S Temperature | **PCB’s Temperature：** the data of PCB’s temperature is 1 byte with signed number, and the minimum resolution is 1℃.<br>For example:<br>[0x16] 0x16 converted to decimal is 20,the resulting temperature T=20℃<br>[0xF0] 0xF0 converted to decimal is -16,the resulting temperature T=-16℃ |
| BYTE12 | High Byte of output power | **Output Power:** the data of output power is represented by 2 bytes, and the minimum resolution is 1W. For example:[0x06,0x40] The output power is represented by two hexadecimal numbers,0x06 converted to decimal is 6 and 0x40 converted to decimal is 64.The decimal value of the data is 6*256+64=1600.The resulting power P=1600*0.1W=1600W. |
| BYTE13 | Low Byte of output power | |
| BYTE14 | High byte of CRC check | **Cyclic Redundancy Check is CRC16=f($X^{16}+X^{15}+X^2+1$)**<br>To perform CRC16 operation on the first 14 bytes of byte0-byte13,byte14=high byte of check result,byte15=low byte of check result. |
| BYTE15 | Low byte of CRC check | |

### 12.2.2 APP Message for receiving

There are two APP messages that the inverter can receive.

**Inverter OFF:** The inverter output will be turned off once it receives a shutdown message.
**Inverter ON:** The inverter output will be turned on once it receives a turn on message and clear the fault status.

The message length is 16 bytes, and the timeout is 50mS,which means that the time interval of sending messages between bytes should be less than 50mS.To avoid receiving error frames, it is recommended that the time interval between two groups of messages is greater than 100mS.

**Inverter OFF Message：**

| **Inverter OFF**（50ms receive timeout） | | |
|---|---|---|
| BYTE0 | Command 1 | 0x0F |
| BYTE1 | Command 2 | 0xF0 |
| BYTE2 | Command 3 | 0x5A |
| BYTE3 | Command 4 | 0x36 |
| BYTE4 | Reserved | 0x00 |
| BYTE5 | Reserved | 0x00 |
| BYTE6 | Reserved | 0x00 |
| BYTE7 | Reserved | 0x00 |
| BYTE8 | Reserved | 0x00 |
| BYTE9 | Reserved | 0x00 |
| BYTE10 | Reserved | 0x00 |
| BYTE11 | Reserved | 0x00 |
| BYTE12 | Reserved | 0x00 |
| BYTE13 | Reserved | 0x00 |
| BYTE14 | High byte of CRC check | **Cyclic Redundancy Check is CRC16=f($X^{16}+X^{15}+X^2+1$)** To perform CRC16 operation on the first 14 bytes of byte0-byte13,byte14=high byte of check result,byte15=low byte of check result. |
| BYTE15 | Low byte of CRC check | |

**Inverter ON Message：**

| **Inverter ON**（50ms receive timeout） | | |
|---|---|---|
| BYTE0 | Command 1 | 0x7D |
| BYTE1 | Command 2 | 0xD7 |
| BYTE2 | Command 3 | 0xFE |
| BYTE3 | Command 4 | 0xDA |
| BYTE4 | Reserved | 0x00 |
| BYTE5 | Reserved | 0x00 |

| | | |
|---|---|---|
| BYTE6 | Reserved | 0x00 |
| BYTE7 | Reserved | 0x00 |
| BYTE8 | Reserved | 0x00 |
| BYTE9 | Reserved | 0x00 |
| BYTE10 | Reserved | 0x00 |
| BYTE11 | Reserved | 0x00 |
| BYTE12 | Reserved | 0x00 |
| BYTE13 | Reserved | 0x00 |
| BYTE14 | High byte of CRC check | **Cyclic Redundancy Check is CRC16=f($X^{16}+X^{15}+X^2+1$)** To perform CRC16 operation on the first 14 bytes of byte0-byte13,byte14=high byte of check result,byte15=low byte of check result. |
| BYTE15 | Low byte of CRC check | |

## 12.3 CFG Functions

The **CFG** is a advanced **Configuration** function, which is mainly used to set working mode of inverter and to calibrate the parameters value. The **CFG** works in inverter stopping. The parameter values configured through the **CFG** will be stored in the FLASH of EG8025, and automatically load during power on.

The **CFG** functions requires a request massage from host, and EG8025 responds to the request service and sends the response massage back to host.

Both sending data and receiving data use with a fixed length of 16 bytes. The message starts with ASCII codes ‘E’ and ‘G’, and ends with CRC16. In order to distinguish between **APP** message and **CFG** message, EG8025 uses a CRC checksum to distinguish it.

The checksum of **APP** message is f($\mathbf{X^{16}+X^{15}+X^2+1}$). The checksum of **CFG** message is f($\mathbf{X^{16}+X^{15}+X^2+1}$)+1,that is, the **CFG** message is equal to **APP**+1.

### 12.3.1 CFG Request Message

**CFG Request Message Format:**

| CFG Request Message（50ms receive timeout） | | |
|---|---|---|
| BYTE0 | Header 1 | 0x45 - ‘E’ |
| BYTE1 | Header 2 | 0x47 - ‘G’ |
| BYTE2 | Service ID(SID) | CFG service code requested by the host |
| BYTE3 | Subfunction(sfun)/ 地 址 (addr) | Subfunction or Address under the current service |
| BYTE4 | Request Data 1 | |
| BYTE5 | Request Data 2 | |
| BYTE6 | Request Data 3 | |
| BYTE7 | Request Data 4 | |
| BYTE8 | Request Data 5 | |
| BYTE9 | Request Data 6 | |

| | | |
|---|---|---|
| BYTE10 | Request Data 7 | |
| BYTE11 | Request Data 8 | |
| BYTE12 | Request Data 9 | |
| BYTE13 | Request Data 10 | |
| BYTE14 | High byte of CRC check | **Cyclic Redundancy Check is CRC16=f($X^{16}+X^{15}+X^2+1$)+1** To perform CRC16 operation on the first 14 bytes of byte0-byte13,byte14=high byte of check result,byte15=low byte of check result. |
| BYTE15 | Low byte of CRC check | |

### 12.3.2 CFG Response Message

**CFG Response Message Format:**

| CFG Response Message（50ms receive timeout） | | |
|---|---|---|
| BYTE0 | Header 1 | 0x45 - ‘E’ |
| BYTE1 | Header 2 | 0x47 - ‘G’ |
| BYTE2 | Service ID(SID) | CFG service code requested by the host |
| BYTE3 | Subfunction(sfun)/ 地 址 (addr) | Subfunction or Address under the current service |
| BYTE4 | Request Data 1 | |
| BYTE5 | Request Data 2 | |
| BYTE6 | Request Data 3 | |
| BYTE7 | Request Data 4 | |
| BYTE8 | Request Data 5 | |
| BYTE9 | Request Data 6 | |
| BYTE10 | Request Data 7 | |
| BYTE11 | Request Data 8 | |
| BYTE12 | Request Data 9 | |
| BYTE13 | Request Data 10 | |
| BYTE14 | High byte of CRC check | **Cyclic Redundancy Check is CRC16=f($X^{16}+X^{15}+X^2+1$)+1** To perform CRC16 operation on the first 14 bytes of byte0-byte13,byte14=high byte of check result,byte15=low byte of check result. |
| BYTE15 | Low byte of CRC check | |

### 12.3.3 0x22 Service -Read DID

The 0x22 is a read DID service. The system’s configuration parameters and version information are stored in the DID. The host can read it by requesting the 0x22 service.

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Byte 7 | Byte 8 | Byte 9 | Byte 10 | Byte 11 | Byte 12 | Byte 13 | Byte 14 | Byte 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x45 | 0x47 | 0x22 | addr | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | CRC16 | |

Addr is the address of the DID. The different DID address store the different DID information.

Response from slave:

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Byte 7 | Byte 8 | Byte 9 | Byte 10 | Byte 11 | Byte 12 | Byte 13 | Byte 14 | Byte 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x45 | 0x47 | 0x22 | addr | d1 | d2 | d3 | d4 | d5 | d6 | d7 | d8 | d9 | d10 | CRC16 | |

If the slave responds that D1-D10 are all 0xFF,it means that reading DID failed.

### 12.3.4 0x2E Service-Write DID

The 0x2E is a writing DID service. The host can write configuration parameters and version information into EG8025 by requesting the 0x2E service.

0x2E request message from host:

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Byte 7 | Byte 8 | Byte 9 | Byte 10 | Byte 11 | Byte 12 | Byte 13 | Byte 14 | Byte 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x45 | 0x47 | 0x2E | addr | d1 | d2 | d3 | d4 | d5 | d6 | d7 | d8 | d9 | d10 | CRC16 | |

Addr is the address of the DID. The different DID address store the different DID information.

Response from slave:

| Byte0 | Byte1 | Byte2 | Byte3 | Byte4 | Byte5 | Byte6 | Byte7 | Byte8 | Byte9 | Byte 10 | Byte 11 | Byte 12 | Byte 13 | Byte 14 | Byte 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x45 | 0x47 | 0x2E | addr | resp | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | CRC16 | |

resp = 1 : Write Succeeded

resp = 0 : Write Failed

DID information table:

| DID Information Table | | | | | |
|---|---|---|---|---|---|
| **ADDR** | **DID** | **W/R** | **LEN** | **TYPE** | **Description** |
| 0x09 | ProductDate | w/r | 4 | BCD | This DID can be written into the production date of inverter. Such as October 15,2019:<br>d1 = 0x20<br>d2 = 0x19<br>d3 = 0x10<br>d4 = 0x15 |
| 0x0A | SerialNo | w/r | 10 | ASCII | This DID can be written into the serial number of inverter. For example, the 0001 product of the 21st week of 2019 produced by the HS factory:"HS19210001"<br>d1 = ‘H’<br>d2 = ‘S’<br>d3 = ‘1’<br>d4 = ‘9’<br>d5 = ‘2’ |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | d6 = ‘1’<br>d7 = ‘0’<br>d8 = ‘0’<br>d9 = ‘0’<br>d10 = ‘1’ |
| 0x0B | PartNo | r | 10 | ASCII | This DID represents the part number of the main IC:<br>"EG8025" |
| 0x0C | ChipID | r | 10 | hex | This DID contains the chip ID, and each chip has unique ID:<br>For example：0x0123456789ABCDEF0123<br>d1 = 0x01<br>d2 = 0x23<br>d3 = 0x45<br>d4 = 0x67<br>d5 = 0x89<br>d6 = 0xAB<br>d7 = 0xCD<br>d8 = 0xEF<br>d9 = 0x01<br>d10 = 0x23 |
| 0x0D | UsartVer | r | 10 | ASCII | Serial communication protocol version number, such as V1.0 version released on October 15,2019:<br>“1.0.191015” |
| 0x0E | SoftwareVer | r | 10 | ASCII | Firmware version number, such as V2.0 version released on October 15,2019:<br>“2.1.191015” |
| 0x0F | HardwareVer | r | 10 | ASCII | Hardware version number, such as V3.2 version released on October 15,2019:<br>“3.2.191015” |

### 12.3.5 0x2F Service -IO Control

The 0x2F is an IO control service. The host can control the work mode of EG8025 by requesting the 0x2F service, such as work in test mode.

0x2F request message from host:

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Byte 7 | Byte 8 | Byte 9 | Byte 10 | Byte 11 | Byte 12 | Byte 13 | Byte 14 | Byte 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x45 | 0x47 | 0x2F | sfun | ctl | d2 | d3 | d4 | d5 | d6 | d7 | d8 | d9 | d10 | CRC16 | |

Sfun is a different IO service sub-function, and ctl is the control word under the current sub-function.

Response from slave:

| Byte 0 | Byte 1 | Byte 2 | Byte 3 | Byte 4 | Byte 5 | Byte 6 | Byte 7 | Byte 8 | Byte 9 | Byte 10 | Byte 11 | Byte 12 | Byte 13 | Byte 14 | Byte 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x45 | 0x47 | 0x2F | sfun | resp | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | CRC16 |

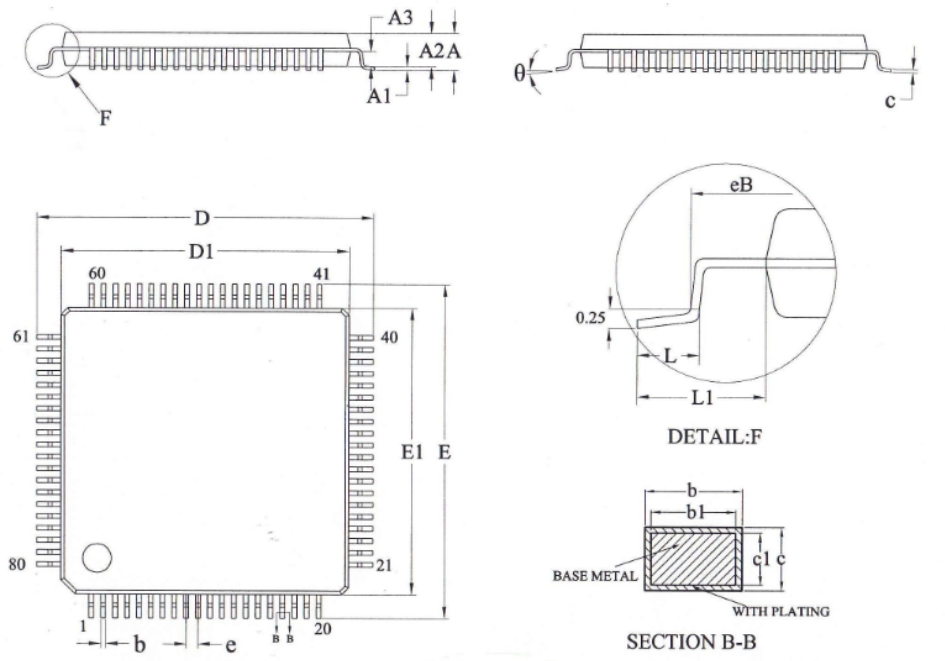
resp = ctl : Write succeeded
resp = 0xFF : Write Failed

IO Control Table:

| IO Control Table | | |
|---|---|---|
| 0x02 | 0x00 | Inverter works in closed loop mode |
| | 0x03 | Inverter works in SPWM open loop mode |

# 13. Package Dimensions

## 13.1 LQFP80




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 13.80 | 14.00 | 14.20 |
| D1 | 11.90 | 12.00 | 12.10 |
| E | 13.80 | 14.00 | 14.20 |
| E1 | 11.90 | 12.00 | 12.10 |
| eB | 13.05 | — | 13.25 |
| e | 0.50BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00REF | | |
| θ | 0 | — | 7° |